

WWW.VUTUBE.EDU.PK

CS501 Advanced Computer Architecture

Mid Term Examination - November 2004

Time Allowed: 90 Minutes

Please read the following instructions carefully before attempting any of the questions:

1. Attempt all questions. Marks are written adjacent to each question.
2. Do not ask any questions about the contents of this examination from anyone.
 - a. If you think that there is something wrong with any of the questions, attempt it to the best of your understanding.
 - b. If you believe that some essential piece of information is missing, make an appropriate assumption and use it to solve the problem.
 - c. Write all steps, missing steps may lead to deduction of marks.
3. Exam is Closed Book. No handouts or extra material is allowed in exam hall other than rough sheet which will be provided by the examiner.

****WARNING: Please note that Virtual University takes serious note of unfair means. Anyone found involved in cheating will get an `F` grade in this course.**

Total Marks: 50
Questions: 5

Total

Question No. 1

Marks : 6

Write short answers to the following questions:

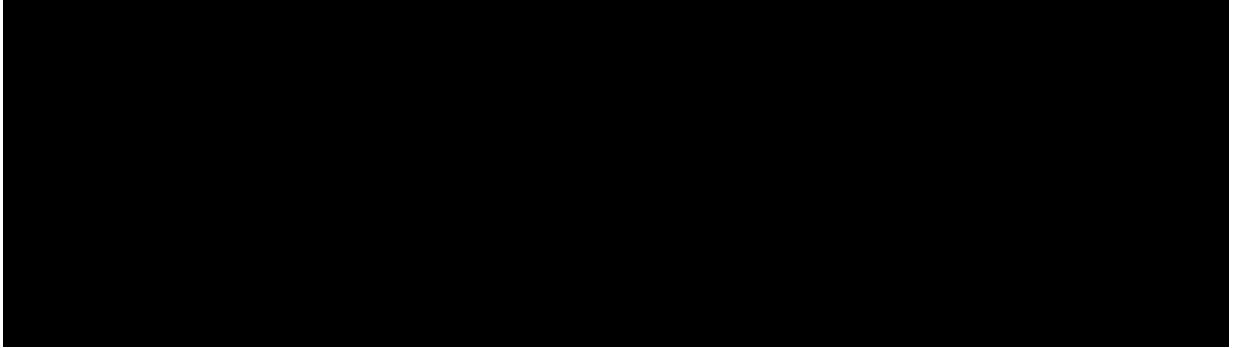
- (a) Define 'Single Stepping'.
- (b) What is meant by control signals?
- (c) What is the difference between instruction memory and data memory?

Question No. 2

Marks : 14

Complete the table given.

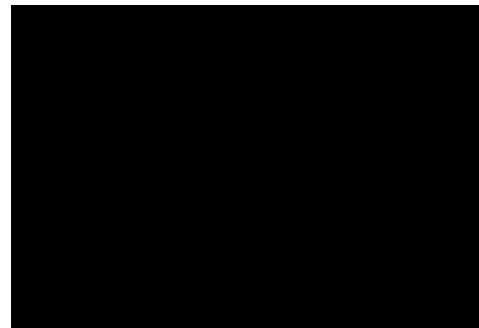
What will be the logic levels on the external FALCON-A buses when each of the following FALCON-A instruction is executing on the processor? All numbers are in the decimal number system, unless noted otherwise. Also specify memory addressing modes for each of the FALCON-A instructions given.



Assumptions:

- All memory content is aligned properly.
In other words, all the memory accesses start at addresses divisible by 2.
- Value in the PC = C348h

Memory Map with assumed values:



Question No. 3

Marks : 10

Consider two programs having three types of instructions given as follows:

Compare both the programs for the following parameters:

1. Instruction count
2. Speed of execution

Question No. 4

Marks : 10

The following diagram shows the uni-bus implementation of the FALCON-A CPU.

Write the structural RTL description for the 'sub r3, r2, r1' instruction including the instruction fetch phase. Assume that a timing generator with up to eight timing intervals is available.

Question No. 5

Marks : 10

The following table shows a partial summary of the ISA for the SRC. Write an assembly language program using the SRC assembly language to evaluate the expression:

$$Z = 8(a + 58) - b$$

Note: a, b and c are names of memory locations. Your program should not change the source operands. Do not worry about the contents of a and b. There is no need to worry about assembler directives. Comments in your code may be helpful.

