

Question No : 1 of 52

Marks: 1 (Budgeted Time 1 Min)

The hexadecimal value "FD" is equivalent to binary value _____

Answer (Please select your correct option)

VuAnswers.com

11011111

11111101

correct

11001110

00010111

Made by: Waqar Siddhu

Question No : 2 of 52

Marks: 1 (Budgeted Time 1 Min)

"A + B = B + A" is _____

Answer (Please select your correct option)

VuAnswers.com

Demorgan's Law

Distributive Law

Commutative Law

correct

Associative Law

Made by: Waqar Siddhu

Question No : 3 of 52

Marks: 1 (Budgeted Time 1 Min)

_____ is invalid number of cells in a single group formed by the adjacent cells in K-map

Answer (Please select your correct option)

VuAnswers.com

2

8

12

correct

16

Made by: Waqar Siddhu

Question No : 4 of 52

Marks: 1 (Budgeted Time 1 Min)

The _____ Encoder is used as a keypad encoder.

Answer (Please select your correct option)

VuAnswers.com

- 2-to-8 encoder
- 4-to-16 encoder
- BCD-to-Decimal
- Decimal-to-BCD Priority

correct

Made by: Waqar Siddhu

Question No : 5 of 52

Marks: 1 (Budgeted Time 1 Min)

The Programmable Array Logic (PAL) has _____ AND array and a _____ OR array

Answer (Please select your correct option)

VuAnswers.com

- Fixed, programmable
- Programmable, fixed
- Fixed, fixed
- Programmable, programmable

correct

Made by: Waqar Siddhu

Question No : 6 of 52

Marks: 1 (Budgeted Time 1 Min)

74HC163 has two enable input pins which are _____ and _____

Answer (Please select your correct option)

VuAnswers.com

- ENP, ENT
- ENI, ENC
- ENP, ENC
- ENT, ENI

correct

Made by: Waqar Siddhu

Question No : 7 of 52

Marks: 1 (Budgeted Time 1 Min)

Given the state diagram of an up/down counter, we can find _____

Answer (Please select your correct option)

VuAnswers.com

The next state of a given present state

correct

The previous state of a given present state

Both the next and previous states of a given state

The state diagram shows only the inputs/outputs of a given states

Made by: Waqar Siddhu

Question No : 8 of 52

Marks: 1 (Budgeted Time 1 Min)

A 4-bit parallel in / serial out shift register contains the value "0100", _____ clock signal(s) will be required to shift the value completely out of the register (i.e. to set the register to 0).

Answer (Please select your correct option)

VuAnswers.com

1

2

correct

3

4

Made by: Waqar Siddhu

Question No : 9 of 52

Marks: 1 (Budgeted Time 1 Min)

In Single-Precision Floating Point format, "exponent" is represented by _____ bits.

Answer (Please select your correct option)

VuAnswers.com

8-bits

16-bits

32-bits

correct

64-bits

Made by: Waqar Siddhu

Question No : 10 of 52

Marks: 1 (Budgeted Time 1 Min)

A particular Full Adder has _____ inputs and _____ output(s).

Answer (Please select your correct option)

VuAnswers.com

2, 3

2, 2

3, 2

correct

3, 3

Made by: Waqar Siddhu

Question No : 11 of 52

Marks: 1 (Budgeted Time 1 Min)

Programmable Array Logic (PAL) has _____ input(s) and _____ output(s).

Answer (Please select your correct option)

VuAnswers.com

Single, multiple

Multiple, single

Single, single

Multiple, multiple

correct

Made by: Waqar Siddhu

Question No : 12 of 52

Marks: 1 (Budgeted Time 1 Min)

At $S = 0$ and $R = 1$, an active-HIGH SR latch is in _____ condition.

Answer (Please select your correct option)

VuAnswers.com

SET

RESET

correct

not sure

Invalid

No change

Made by: Waqar Siddhu

Question No : 13 of 52

Marks: 1 (Budgeted Time 1 Min)

At $J = 1$, and $K = 1$, output of JK Flip-flop will be _____

Answer (Please select your correct option)

VuAnswers.com

Set

Reset

Toggle

Invalid

correct

Made by: Waqar Siddhu

Question No : 14 of 52

Marks: 1 (Budgeted Time 1 Min)

The negative edge triggered flip-flop changes state on _____

Answer (Please select your correct option)

VuAnswers.com

Positive half cycle of clock

Negative half of clock

Low-to-high transition of clock

High-low transition of clock

correct

Made by: Waqar Siddhu

Question No : 15 of 52

Marks: 1 (Budgeted Time 1 Min)

When four 1's are taken as a group on a Karnaugh map, the number of variables eliminated from the output expression is/are _____

Answer (Please select your correct option)

VuAnswers.com

1

2

3

4

correct

Made by: Waqar Siddhu

Question No : 16 of 52

Marks: 1 (Budgeted Time 1 Min)

The _____ output of first 74HC163 counter is connected to _____ and _____ inputs of other 74HC163 counter to form a single cascaded counter

Answer (Please select your correct option)

VuAnswers.com

RCO, ENT, ENP

correct

ENT, RCO, ENP

ENP, RCO, ENT

RCO, ENI, ENC

Made by: Waqar Siddhu

Question No : 17 of 52

Marks: 1 (Budgeted Time 1 Min)

The design and implementation of synchronous counters start from _____

Answer (Please select your correct option)

VuAnswers.com

Truth table

K-map

State table

State diagram

correct

Made by: Waqar Siddhu

Question No : 18 of 52

Marks: 1 (Budgeted Time 1 Min)

The best state assignment tends to _____.

Answer (Please select your correct option)

VuAnswers.com

Maximizes the number of state variables that don't change in a group of related states

correct

Minimizes the number of state variables that don't change in a group of related states

Minimizes the equivalent states

Maximizes the equivalent states

Made by: Waqar Siddhu

Question No : 19 of 52

Marks: 1 (Budgeted Time 1 Min)

In _____, the \bar{Q} output of the last flip-flop of the shift register is connected to the data input of the first flip-flop.

Answer (Please select your correct option)

VuAnswers.com

- Moore machine
- Mealy machine
- Johnson counter
- Ring counter

correct

Made by: Waqar Siddhu

Question No : 20 of 52

Marks: 1 (Budgeted Time 1 Min)

In _____, the Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.

Answer (Please select your correct option)

VuAnswers.com

- Moore machine
- Mealy machine
- Johnson counter
- Ring counter

correct

Made by: Waqar Siddhu

Question No : 21 of 52

Marks: 1 (Budgeted Time 1 Min)

If $S=1$ and $R=0$, then $Q(t+1) = \underline{\hspace{2cm}}$ for positive edge triggered flip-flop

Answer (Please select your correct option)

VuAnswers.com

- 0
- 1
- Invalid
- Input is invalid

correct

Made by: Waqar Siddhu

Question No : 22 of 52

Marks: 1 (Budgeted Time 1 Min)

For a gated D-Latch, if $EN=1$ and $D=1$ then $Q(t+1) =$ _____

Answer (Please select your correct option)

VuAnswers.com

0

1

$Q(t)$

Invalid

Made by: Waqar Siddhu

Question No : 23 of 52

Marks: 1 (Budgeted Time 1 Min)

Which of the following is NOT a sequential circuit?

Answer (Please select your correct option)

VuAnswers.com

SR latch

Counter

correct

Full Adder

JK Flip-flop

Made by: Waqar Siddhu

Question No : 24 of 52

Marks: 1 (Budgeted Time 1 Min)

Each stage of Master-slave flip-flop works in _____

Answer (Please select your correct option)

VuAnswers.com

One complete clock signal

One fourth of the clock signal

One third of the clock signal

One half of the clock signal

correct Made by: Waqar Siddhu

Question No : 25 of 52

Marks: 1 (Budgeted Time 1 Min)

The counter states can be determined by the formula: _____ ("n" represents the total number of flip-flops).

Answer (Please select your correct option)

VuAnswers.com

- n^2 (n raise to power 2)
- n^2-1 (n raise to power 2 and then minus 1)
- 2^n (2 raise to power n)
- 2^n-1 (2 raise to power n and then minus 1)

correct

Made by: Waqar Siddhu

Question No : 26 of 52

Marks: 1 (Budgeted Time 1 Min)

RCO Stands for _____

Answer (Please select your correct option)

VuAnswers.com

- Reconfiguration Counter Output
- Reconfiguration Clock Output
- Ripple Counter Output
- Ripple Clock Output

correct Made by: Waqar Siddhu

Question No : 27 of 52

Marks: 1 (Budgeted Time 1 Min)

A divide-by-50 counter divides the input _____ signal to a 1 Hz signal.

Answer (Please select your correct option)

VuAnswers.com

- 10 Hz
- 50 Hz
- 100 Hz
- 500 Hz

correct

Made by: Waqar Siddhu

Question No : 28 of 52

Marks: 1 (Budgeted Time 1 Min)

The alternate solution for a demultiplexer-register combination circuit is _____

Answer (Please select your correct option)

VuAnswers.com

Parallel in / Serial out shift register

Serial in / Parallel out shift register

correct

Parallel in / Parallel out shift register

Serial in / Serial Out shift register

Made by: Waqar Siddhu

Question No : 29 of 52

Marks: 1 (Budgeted Time 1 Min)

In asynchronous transmission when the transmission line is idle, _____

Answer (Please select your correct option)

VuAnswers.com

It is set to logic low

It is set to logic high

correct

Remains in previous state

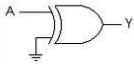
State of transmission line is not used to start transmission

Made by: Waqar Siddhu

Question No : 30 of 52

Marks: 1 (Budgeted Time 1 Min)

The output of this circuit is always _____



Answer (Please select your correct option)

VuAnswers.com

1

0

A

correct

\bar{A}

Made by: Waqar Siddhu

Question No : 31 of 52

Marks: 1 (Budgeted Time 1 Min)

Which is not characteristic of a shift register?

Serial in/parallel in

correct

Serial in/parallel out

Parallel in/serial out

Parallel in/parallel out

VuAnswers.com

Made by: Waqar Siddhu

Question No : 32 of 52

Marks: 1 (Budgeted Time 1 Min)

A Nibble consists of ____ bits

2

4

correct

8

16

VuAnswers.com

Made by: Waqar Siddhu

Question No : 33 of 52

Marks: 1 (Budgeted Time 1 Min)

The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines

Write Time

Refresh Time

Refresh Time

Access Time

correct

VuAnswers.com

Made by: Waqar Siddhu

Question No : 34 of 52

Marks: 1 (Budgeted Time 1 Min)

In _____, all the columns in the same row are either read or written.

Answer (Please select your correct option)

VuAnswers.com

Sequential Access

MOS Access

FAST Mode Page Access

correct

None of given options

Made by: Waqar Siddhu

Question No : 35 of 52

Marks: 1 (Budgeted Time 1 Min)

In order to synchronize two devices that consume and produce data at different rates, we can use _____

Answer (Please select your correct option)

VuAnswers.com

Read Only Memory

First In First Out Memory

correct

Flash Memory

Fast Page Access Mode Memory

Made by: Waqar Siddhu

Question No : 36 of 52

Marks: 1 (Budgeted Time 1 Min)

The process of converting the analogue signal into a digital representation (code) is known as _____

Answer (Please select your correct option)

VuAnswers.com

Strobing

Amplification

Quantization

correct

Digitization

Made by: Waqar Siddhu

Question No : 37 of 52

Marks: 1 (Budgeted Time 1 Min)

A hold action occurs :

Answer (Please select your correct option)

VuAnswers.com

- After the analog-to-digital conversion
- During each sample
- Immediately after a sample
- Before each sample

Made by: Waqar Siddhu

Question No : 38 of 52

Marks: 1 (Budgeted Time 1 Min)

A flash A/D converter uses :

Answer (Please select your correct option)

VuAnswers.com

- Counters
- Flip-flops
- Op-amps
- An integrator

correct

Made by: Waqar Siddhu

Question No : 39 of 52

Marks: 1 (Budgeted Time 1 Min)

_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

Answer (Please select your correct option)

VuAnswers.com

- Resolution
- Accuracy
- Quantization
- Missing Code

correct

Made by: Waqar Siddhu

Question No : 40 of 52

Marks: 1 (Budgeted Time 1 Min)

Sampling of an analog signal produces :

Answer (Please select your correct option)

VuAnswers.com

- A series of impulses those are proportional to the frequency of the signal
- A series of impulses those are proportional to the amplitude of the signal
- Digital codes that represent the analog signal amplitude
- Digital codes that represent the time of each sample

Made by: Waqar Siddhu


Question No : 41 of 52

Marks: 2 (Budgeted Time 4 Min)

How many 4-bit Parallel Adders are required to add two BCD digits?

Answer (Please [click here](#) to Add Answer)

VuAnswers.com



Made by: Waqar Siddhu


Question No : 42 of 52

Marks: 2 (Budgeted Time 4 Min)

What is meant by "excitation inputs"?

Answer (Please [click here](#) to Add Answer)

VuAnswers.com



Made by: Waqar Siddhu

Question No : 43 of 52

Marks: 2 (Budgeted Time 4 Min)

How many bytes will be there in $32\text{ K} \times 4$ memory?

Answer (Please [click here](#) to Add Answer)

VuAnswers.com

Normal Arial 12 B I U

Made by: Waqar Siddhu

Question No : 44 of 52

Marks: 2 (Budgeted Time 4 Min)

Generally two types of D/A Converters are used. Write down their names.

Answer (Please [click here](#) to Add Answer)

VuAnswers.com

Normal Arial 12 B I U

Made by: Waqar Siddhu

Question No : 45 of 52

Marks: 3 (Budgeted Time 6 Min)

Draw the function table of an Half adder circuit.

Answer (Please [click here](#) to Add Answer)

VuAnswers.com

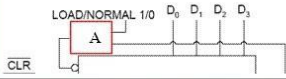
Normal Arial 12 B I U

Made by: Waqar Siddhu

Question No : 46 of 52

Marks: 3 (Budgeted Time 6 Min)

Following is an incomplete diagram. Name the gate which can be placed in red boxes A and B to configure 74HC161 as a Mod-9 counter.



Answer (Please [click here](#) to Add Answer)

VuAnswers.com

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Made by: Waqar Siddhu

Question No : 47 of 52

Marks: 3 (Budgeted Time 6 Min)

Draw a circuit diagram of flip-flop based static memory cell.

Rich text editor toolbar with icons for undo, redo, bold, italic, underline, text color, background color, bulleted list, numbered list, link, unlink, and a 100% zoom level. The text area is empty.

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Made by: Waqar Siddhu

Question No : 48 of 52

Marks: 3 (Budgeted Time 6 Min)

What is RAM Stack, which register stores the address of top of the stack?

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Made by: Waqar Siddhu

Question No : 49 of 52

Marks: 5 (Budgeted Time 10 Min)

Simplify the following Boolean expression so that it uses minimum number of gates.

$$\overline{(A + B + C + D)} + \overline{(ABC)}$$

Answer (Please [click here](#) to Add Answer)

VuAnswers.com



Made by: Waqar Siddhu

Question No : 50 of 52

Marks: 5 (Budgeted Time 10 Min)

You are given the block diagram of 74HC163 4-bit Synchronous Counter. Connect two 74HC163 4-bit Synchronous Counters to form a single Cascaded Decade Counter.



Answer (Please [click here](#) to Add Answer)

VuAnswers.com



Made by: Waqar Siddhu

