Q.1 A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

A. 64 mW

B. 25 mW

C. 1024 mW

D. 10 mW

Q.2 The 74HC163 is a 4-bit Synchronous Counter.it has.....data output pins

A. 8

B. 2

C. 6

D. 4

Q.3 In gated SR latch, what is the value of the output if EN=1, S=0 and R=0?

A. 1

B. Invalid

C. 0

D. Qt

Q.4 In 8-input multiplexer, the two outputs are connected through a/an ____ gate.

A. OR

B. AND

C. NOT

D. NOR

Q.5 In 8-input multiplexer, when ___ is set to 0, the first multiplexer is selected allowing its inputs 1C0, 1C1, 1C2 and 1C3 to be selected.

A. D

B. A

C. B

D. C

Q.6 2-Input, 8-bit Multiplexer, by setting the S input to logic ___ the _ inputs of both the multiplexers are selected.

A. Low, C

B. High, B

C. Low, B

D. Low, C

Q.7 A synchronous decade counter will have _____ flip-flops

A. 10

B. 3

C. 4

D. 7

Q.8 The OLMC can be configured to provide a feedback input signal to the AND gate array input. There are _____ possibilities.

A. two

B. three

C. four

D. five

Q.9 The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

A. Pulse Stability time (PST)

B. Set-up time

C. Pulse Interval time

D. Hold time

Q.10 A mono-stable device only has a single stable state

A. False

B. True

Q.1 The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

A. It does not show transition on change in pulse

B. Doesn't have an invalid state

C. Sets to clear when both J = 0 and K = 0

D. It does not accept asynchronous inputs

Q.2 RCO stands for _____

A. Ripple Counter Output

B. Ripple Clock Output

C. Reconfiguration Counter Output

D. Reconfiguration Clock Output

Q.3 PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.

A. PLAs

B. EPROM

C. PALs

D. PLDs

Q.4 A NOR based S-R latch is implemented using _____ gates instead of _____ gates.

A. NOR,NAND

B. XOR,NAND

C. NOR,XOR

D. OR,XOR

Q.5 ABEL is an acronym for

A. Advanced Boolean Expression Language

B. Advanced Broadband Enabled Longitude

C. Advanced Boolean Equation Language

D. None of the given options

Q.6 An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting _____

A. Q' output of all flip-flops to K input of next flip-flops

B. Q' output of all flip-flops to clock input of next flip-flops

C. Q output of all flip-flops to J input of next flip-flops

D. Q output of all flip-flops to clock input of next flip-flops

---

Q.7 On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when _____

A. The clock pulse transition from LOW to HIGH

B. The clock pulse transition from HIGH to LOW

C. The clock pulse is LOW

D. The clock pulse is HIGH

Q.8 The _____ input overrides the _____ input

A. Synchronous, asynchronous

B. Clear input (CLR), Preset input (PRE)

C. Preset input (PRE), Clear input (CLR)

D. Asynchronous, synchronous

Q.9 The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the _____

A. Set-up time

B. Pulse Stability time (PST)

C. Pulse Interval time

D. Hold time

Q.10 The n flip-flops store ____ states.

A. 2^(n+1)

B. 2^n

C. 0

D. 1

Q.1 In gated SR latch, what is the value of the output if EN=1, S=0 and R=1?

A. 0

B. Invalid

C. Qt

D. 1

Q.2 OLMC stands for _____.

A. Ordered Logic Micro Cells

B. Output Logic Macro Cells

C. Output Logic Micro Cells

D. Ordered Logic Macro Cells

Q.3 The terminal count of a 4-bit binary counter in the UP mode is_____

A. 1111

B. 0011

C. 0000

D. 1100

Q.4 In sequential circuits memory elements are connected with_____.

A. Feedback path

B. Clock

C. External Event

D. Logic circuit

Q.5 When the number 29 is represented on 7-segment display, which BCD input is represented on LSD display unit?

A. 1000

B. 1001

C. 1010

D. 1100

Q.6 All ABEL statements must end with ____.

A. "

B. '

C. ;

D. :

Q.7 If a circuit suffers “Clock Skew “ problem, the output of circuit can’t be guarantied.

A. False

B. True

Q.8 In 8-input multiplexer, the two outputs are connected through a/an ____ gate.

A. NOR

B. NOT

C. OR

D. AND

Q.9 _____ have Buffers at the inputs which produce the actual variable and its complement.

A. EPROM

B. PLA

C. GAL

D. PAL

Q.1 _____ is one of the examples of asynchronous inputs.

A. S-R input
B. D input
C. Clear Input (CLR)
D. J-K input

Q.2 OLMC stands for _____.

A. Ordered Logic Micro Cells
B. Output Logic Micro Cells
C. Ordered Logic Macro Cells
D. Output Logic Macro Cells

Q.3 A source file that is created in ABEL has _____ sections.

A. five
B. two
C. four
D. three

Q.4 The primary use of multiplexers is _____.

A. Logic function generator
B. Parallel to serial convertor
C. Operation sequencing
D. Data Router

Q.5 PALs tend to execute _____ logic.

A. SAP
B. SAC
C. SOP
D. SPD

Q.6 In asynchronous digital systems all the circuits change their state with respect to a common clock

A. True
B. False

Q.7 Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a ___ multiplexer.

A. 2-input, 8-bit
B. 2-input, 4-bit
C. 4-input, 16-bit
D. 4-input, 8-bit

Q.8 Each stage of Master-slave flip-flop works at ___ of the clock signal

A. Each stage works on complete clock signal

B. One fourth

C. One third

D. One half

Q.9 When the both inputs of edge-triggered J-K flop-flop are set to logic zero _____

A. Q=0 and Q'=1

B. Q=1 and Q'=0

C. The flop-flop is triggered

D. The output of flip-flop remains unchanged

Q.10 We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), to supply the required frequency to each part of circuit, we can get help by using _____

A. T-Flip-Flop

B. D-flipflop

C. Using S-R Flop-Flop

D. J-K flip-flop

Q.1 The absence of a _____ element in sequential circuit restricts the use of digital combinational circuits to certain application areas.

A. memory

B. cell

C. device

D. clock

Q.2 A NOR based S-R latch is implemented using _____ gates instead of _____ gates.

A. XOR,NAND

B. OR,XOR

C. NOR,XOR

D. NOR,NAND

Q.3 Why demultiplexer is called a data distributor?

A. The output will be distributed to one of the inputs

B. Single input to Single Output

C. One of the inputs will be selected for the output

D. The input will be distributed to one of the outputs

Q.4 Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state

A. Ten

B. Two

C. Eight

D. Three

Q.5 In a Digital System, Binary data is used and represented in_____.

A. Serial

B. Static

C. Parallel

D. Variable

Q.6 Design of state diagram is one of many steps used to design

A. an UP/DOWN counter

B. a clock

C. any counter

D. a truncated counter

Q.7 _____are implemented by combining combinational circuits with memory elements.

A. PLDs

B. PLA

C. system

D. Sequential circuits

Q.8 The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

A. Set-up time

B. Pulse Stability time (PST)

C. Hold time

D. Pulse Interval time

Q.9 An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting _____

A. Q' output of all flip-flops to clock input of next flip-flops

B. Q output of all flip-flops to clock input of next flip-flops

C. Q' output of all flip-flops to K input of next flip-flops

D. Q output of all flip-flops to J input of next flip-flops

Q.10 In case of cascading Integrated Circuit counters, the enable inputs and RCOof the Integrated Circuit counters allow cascading of multiple counters together

A. False

B. True

Q.1 Which of the following can be used to declare objects in Ada language?

A. Array

B. Tagged type

C. Stack

D. Function

Q.2 In LISP, an empty list represented by nil is the same as _____.

A. 0

B. ()

C. {}

D. <>

Q.3 Ada language supports function overloading based on their:

A. return type

B. characteristics

C. running time

D. parameters

Q.4 Which of the following is the Range Operator in ADA programming language?

A. ,,

B. ..

C. #

D. %

Q.5 _____ is not a discrete type in Ada.

A. Integer type

B. String Type

C. Character type

D. Modular type

Q.6 Which of the following function of LISP assigns value 5 to symbol y?

A. >(setq,5,y)

B. >(setq y 5)

C. >(setq,y,5)

D. >(setq 5 y)

Q.7 In Ada programming language, _____ operator is used to access individual fields of a record type.

A. Dot

B. Exclamation

C. Space

D. Colon

Q.8 Which of the following post-test loop is not supported in Ada language?

A. 'for' loop

B. 'do while' loop

C. 'while' loop

D. Infinite loop

Q.9 The structure that is used to group data and subprograms in Ada language is called:

A. Package

B. Class

C. Array

D. Function

Q.10 All of the following were main design goals of Ada language EXCEPT:

A. Design language for the Department of Defence (USA)

B. Designing a portable language

C. Program reliability and maintenance

D. Avoid unintentional mistakes during programming

Q.11 RCO stands for _____

A. Ripple Counter Output

B. Ripple Clock Output

C. Reconfiguration Clock Output

D. Reconfiguration Counter Output

Q.12 A NOR based S-R latches maintain the output state when both the set and reset inputs are _____.

A. active

B. inactive

C. consistent

D. invalid

Q.13 If S=1 and R=1, for negative edge triggered flip-flop then

Q(t+1) Input is invalid

B. 0

C. 1

D. Invalid

Q.14 PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.

A. PLDs

B. EPROM

C. PLAs

D. PALs

Q.15 The S-R latch has two inputs, therefore _____ different combinations of inputs can be applied to control the operation of the S-R latch.

A. sixteen

B. four

C. two

D. eight

Q.16 In gated SR latch, what is the value of the output if EN=1, S=1 and R=0?

A. 1

B. Invalid

C. 0

D. Qt

Q.17 The OLMC of the GAL16V8 is similar to the OLMC of the _____ with some enhancements.

A. GAL12V10

B. GAL14V10

C. GAL16V10

D. GAL22V10

Q.18 In case of cascading Integrated Circuit counters, the enable inputs and RCOof the Integrated Circuit counters allow cascading of multiple counters together

A. False

B. True

Q.19 In sequential circuits memory elements are connected with_____.

A. Feedback path

B. Clock

C. Logic circuit

D. External Event

Q.20 In designing any synchronous counter a modulus number is used which determine the number of..... used in a counter

A. Latches

B. Counters

C. Flip Flops

D. Registers

Q.21 We use tagged type in Ada for _____.

A. Encapsulation

B. Polymorphism

C. Abstraction

D. Inheritance

Q.22 Consider the following two statements written in Ada: type Months is (January, February, March, April, May, June, July); type Monthly_Sales is array(Months) of Float; What is size of array named 'Monthly_Sales'?

A. 2

B. 8

C. 7

D. 3

Q.23 Which of the following statement of Ada language is similar to 'throw' statement of C++?

A. exception

B. exit

C. raise

D. disaster

Q.24 Extensible types in Ada language are created through:

A. Tagged types

B. Packages

C. Dynamic programming

D. Operator Overloading

Q.25 Concurrency in Ada language is achieved through _____.

A. Controls
B. Packages
C. Tasking
D. Classes

Q.26 A 'switch' statement is C-language is used for decision making. Its alternative in Ada language is:

A. 'record' statement
B. 'case' statement
C. 'for' statement
D. 'while' statement

Q.27 A 'break' statement in C-language is used to exit from loop structure. It's alternative in Ada language is:

A. terminate
B. exit
C. kill
D. breakif

Q.28 We may create our own exceptions in _____.

A. Ada
B. SNOBOL
C. C
D. C++

Q.29 Which of the following is not type of inheritance in C++?

A. restricted
B. protected
C. private
D. public

Q.30 What is function overriding in C++?

A. Using global functions inside a class
B. Defining multiple functions with the same name in one class
C. Redefining a base class function in a derived class
D. Calling a function multiple times

Q.31 A post-fix unary operator is implemented in C++ using non-member function with _____ argument(s).

A. Three

B. One

C. Two

D. Zero

Q.32 Suppose Person is a user defined class. In statement "Person * pPtr", static type of pPtr is _____.

A. Object

B. Person

C. Person*

D. pPtr

Q.33 Which of the following access specifier ensures that base class member is accessible in derived class of this base class and NOT outside of this class?

A. public

B. protected

C. private

D. Static

**Q.34 Consider the code below: class class1 { public: int i; }; class class2 : private class1 { }; Then int member i of class1 is _____ in class2. **

**A. private/hidden **

B. public

C. static

D. protected

**Q.35 Consider the code below: class class1 { protected: void func1(); }; class class2 : private class1 { }; Function func1 of class1 is _____ in class2. **

A. static

B. public

**C. private/hidden **

D. protected

**Q.36 Consider the code below: class class1 {   private: int i; }; class class2 : protected class1 { }; Then int member i of class1 is _____ in class2. **

A. public

**B. private **

C. static

D. protected

Q.37 In case of protected inheritance, public members of base class will be _____ in derived class.

A. protected

B. hidden

C. private

D. public

**Q.38 Consider the code below: class class1 {   private: void func1(); }; class class2 : public class1 { }; Function func1 of class1 is _____ in class2. **

A. static

B. public

C. protected

**D. private **

Q.39 A 4-bit binary UP/DOWN counter is in the binary state zero. the next state in the DOWN mode is_____

A. 1000

B. 1111

C. 0001

D. 1110

Q.40 _____ flip-flops are obsolete now.

A. Master-Slave

B. Edge-triggered

C. T-Flipflop

D. D-Flipflop

Q.41 Karnaugh map is used in designing

A. All of the above

B. a clock

C. an UP/DOWN counter

D. a counter

Q.42 The power consumed by a flip-flop is defined by _____

A. P = Vcc x Icc

B. P = Icc x Rcc

C. P = Vcc x Rcc

D. P = Mcc x Vcc

Q.43 In Complex mode of GAL16V8, OLMCs can be configured in _____ ways.

A. three

B. four

C. two

D. five

Q.44 8-bit parallel data can be converted into serial data by using _____ multiplexer

A. 4-to-4

B. 4-to-2

C. 8-to-4

D. 8-to-1

Q.45 We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), to supply the required frequency to each part of circuit, we can get help by using _____

A. D-flipflop

B. J-K flip-flop

C. Using S-R Flop-Flop

D. T-Flip-Flop

Q.46 For a gated D-Latch if EN=1 and D=1 then Q(t+1) = _____

A. 1

B. Q(t)

C. 0

D. Invalid

Q.1 _____ is one of the examples of synchronous inputs.

A. Preset input (PRE)

B. Clear Input (CLR)

C. EN input

D. J-K input

Q.2 Three cascaded modulus-10 counters have an overall modulus of

A. 1000

B. 30

C. 10000

D. 100

Q.3 A one-shot mono-stable device contains _____

A. AND gate, Resistor, Capacitor and NOT Gate

B. XNOR gate, Resistor, Capacitor and NOT Gate

C. NAND gate, Resistor, Capacitor and NOT Gate

D. NOR gate, Resistor, Capacitor and NOT Gate

Q.4 A latch is a temporary storage device that has _____ stable states.

A. three

B. four

C. two

D. five

Q.5 In 8-input multiplexer, when __ is set to 0, the first multiplexer is selected allowing its inputs 1C0, 1C1, 1C2 and 1C3 to be selected.

A. C

B. B

C. A

D. D

Q.6 The _____ input overrides the _____ input

A. Clear input (CLR), Preset input (PRE)

B. Synchronous, asynchronous

C. Preset input (PRE), Clear input (CLR)

D. Asynchronous, synchronous

Q.7 If S=1 and R=0, then for positive edge triggered flip-flop

Q(t+1) Input is invalid

B. 1

C. Invalid

D. 0

Q.8 _____ Counters as the name indicates are not triggered simultaneously

A. Negative-Edge triggered

B. Positive-Edge triggered

C. Synchronous

D. Asynchronous

Q.9 A positive edge-triggered flip-flop changes its state when _____

A. Low-to-high transition of clock

B. Enable input (EN) is set

C. Preset input (PRE) is set

D. High-to-low transition of clock

Q.10 The combinational digital circuits have _____ storage element; therefore combinational circuits handle only instantaneous inputs.

A. one

B. three

C. no

D. two

Q.1 The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

A. Pulse Interval time

B. Hold time

C. Set-up time

D. Pulse Stability time (PST)

Q.2 A standard interface for programming the In-System PLD consists of

A. 4-wire

B. 8-wire

C. 16-wire

D. 2-wire

Q.3 To display the number ___ the BCD number 0010 representing the MSD is applied at the inputs of the BCD to 7-Segment display circuit connected to the MSD 7-Segment Display Digit.

A. 49

B. 29

C. 39

D. 19

Q.4 A decade counter is _____

A. Mod-8 counter

B. Mod-3 counter

C. Mod-5 counter

D. Mod-10 counter

Q.5 _____are implemented by combining combinational circuits with memory elements.

A. system

B. PLA

C. PLDs

D. Sequential circuits

Q.6 The primary use of multiplexers is _____.

A. Operation sequencing

B. Parallel to serial convertor

C. Logic function generator

D. Data Router

Q.7 A NOR based S-R latch is implemented using _____ gates instead of _____ gates.

A. OR,XOR

B. NOR,XOR

C. NOR,NAND

D. XOR,NAND

Q.8 The OLMC of the GAL16V8 is similar to the OLMC of the _____ with some enhancements.

A. GAL16V10

B. GAL12V10

C. GAL22V10

D. GAL14V10

Q.9 For a gated D-Latch if EN=1 and D=1 then Q(t+1) = _____

A. 1

B. 0

C. Q(t)

D. Invalid

Q.10 Tri-State Buffer is a _____ gate with a control line that disconnects the output from the input.

A. AND

B. NOT

C. OR

D. NAND

Q.1 In 16-input multiplexer, the decoder inputs ___ and ___ enable one out of the four multiplexers.

A. A, B
B. A, D
C. C, D
D. B, C

Q.2 Why demultiplexer is called a data distributor?

A. Single input to Single Output
B. One of the inputs will be selected for the output
C. The input will be distributed to one of the outputs
D. The output will be distributed to one of the inputs

Q.3 the terminal count of a modulus-13 binary counter is

A. 1100
B. 1111
C. 1101
D. 0000

Q.4 The_____ output has the output of the OR gate connected through an XOR gate to the tri-state buffer.

A. PLA
B. Programmed Polarity
C. Combinational input/
D. Combinational

Q.5 In sequential circuits memory elements are connected with_____.

A. Clock
B. Logic circuit
C. External Event
D. Feedback path

Q.6 The primary use of multiplexers is _____.

A. Operation sequencing
B. Data Router
C. Logic function generator
D. Parallel to serial convertor

Q.7 PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.

A. PLAs

B. PALs

C. PLDs

D. EPROM

Q.8 The counter states or the range of numbers of a counter is determined by the formula. ("n" represents the total number of flip-flops)

A. (n raise to power 2)

B. (2 raise to power n and then minus 1)

C. (n raise to power 2 and then minus 1)

D. (2 raise to power n)

Q.9 The power consumed by a flip-flop is defined by _____

A. P = Vcc x Rcc

B. P = Icc x Rcc

C. P = Vcc x Icc

D. P = Mcc x Vcc

Q.10 The Synchronous counters are also known as Ripple Counters:

A. False

B. True

Q.1 In 8-input multiplexer, when ___ is set to 0, the first multiplexer is selected allowing its inputs 1C0, 1C1, 1C2 and 1C3 to be selected.

A. D

B. C

C. A

D. B

Q.2 Demultiplexer can also be used as

A. Decoder

B. Encoder

C. Deselector

D. Inverse multiplexer

Q.3 A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

A. 10 mW

B. 25 mW

C. 1024 mW

D. 64 mW

Q.4 PALs tend to execute _____ logic.

A. SAC

B. SAP

C. SOP

D. SPD

Q.5 _____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.

A. Combinational Input/Output

B. Combinational Input

C. Programmable polarity

D. Combinational Output

Q.6 When the number 29 is represented on 7-segment display, which BCD input is represented on LSD display unit?

A. 1001

B. 1000

C. 1010

D. 1100

Q.7 Design of state diagram is one of many steps used to design

A. a clock

B. an UP/DOWN counter

C. any counter

D. a truncated counter

Q.8 OLMC stands for _____.

A. Ordered Logic Macro Cells

B. Output Logic Micro Cells

C. Output Logic Macro Cells

D. Ordered Logic Micro Cells

Q.9 Why demultiplexer is called a data distributor?

A. Single input to Single Output

B. One of the inputs will be selected for the output

C. The output will be distributed to one of the inputs

D. The input will be distributed to one of the outputs

Q.10 In 1-to-4 demultiplexer, how many select lines are required

A. 4

B. 5

C. 3

D. 2

Q.1 A binary tree will not be considered an AVL tree if the difference between left and right subtree of each node is not more than :

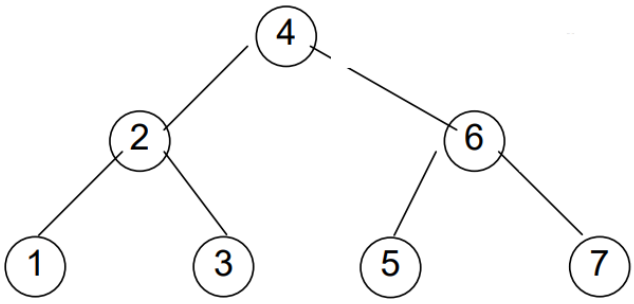
A. 0

B. 2

C. 3

D. 1

Q.2 What will be the balance factor of node 6 if node 5 is deleted from the given tree ?



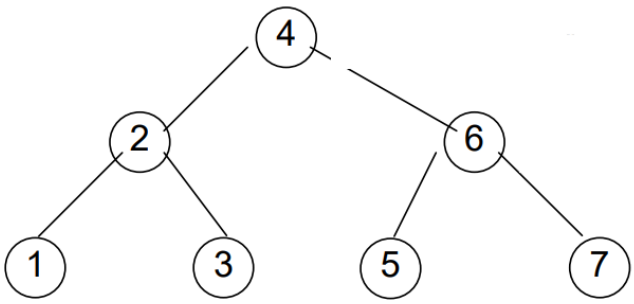
A. -1

B. 2

C. 0

D. 1

Q.3 What will be the balance factor of node 2 if node 1 is deleted from the given tree ?



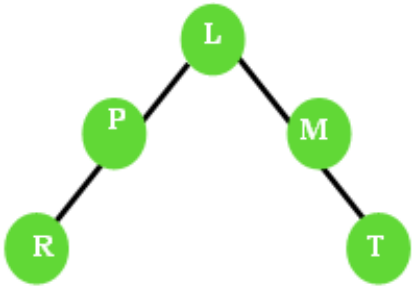
A. 1

B. 0

C. 2

D. -1

Q.4 Which node will become unbalanced if a node is inserted as child of the node R in the given tree?



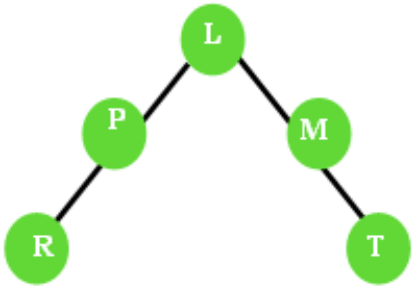
A. L

B. R

C. P

D. M

Q.5 How many rotations will be made if a node is inserted as left child of the node R in the given tree?



A. 3

B. 1

C. 4

D. 2

Q.6 Within an expert system, the _____ contains facts about a specific subject area and rules that express the reasoning procedures of an expert on the subject.

A. Knowledge base

B. Knowledge engineer

C. inference logic

D. Inference engine

Q.7 In CLIPS, _____ command is used to remove facts.

A. retract

B. erase

C. facts

D. delete

Q.8 Backward chaining is more focused and tries to avoid exploring _____ paths of reasoning.

A. different

B. searching

C. unnecessary

D. necessary

Q.9 Identify correct statement for the given rule.
score of Ali is 66

Then
IF
He is eligible to take admission in any of the University abroad
IELTS score of Ali is 6 and
CGPA of Ali is 3.7 and
GRE

A. (defrule Alichance (Ali (attribute “IELTS score”)(value “6”))
(Ali (attribute “GRE”)(value “66”))
(Ali (attribute “CGPA”)(value “3.7”))
=>
(printout t “He is eligible to take admission in any of the University abroad”))

B. (deftamplate Ali (slot attribute)(slot value))
(attribute “CGPA”)(value “3.7”))
(Ali (attribute “GRE”)(value “66”))
(Ali
<=
(Ali (attribute “IELTS score”)(value “6”))

C. (deftamplate Ali (slot attribute)(slot value))
(defrule Alichance (Ali (attribute “IELTS score”)(value “6”))
(Ali (attribute “CGPA”)(value “3.7”))
(Ali (attribute “GRE”)(value “66”))
=>
(printout t “He is eligible

D. (deftamplate Ali (slot attribute)(slot value))
(attribute “CGPA”)(value “3.7”))
(Ali (attribute “GRE”)(value “66”))
(Ali
=>
(printout t “He is eligible to take

Q.10 Which of the following window is not present in CLIPS tool.

A. Facts window

B. Rule window

C. Focus window

D. Agenda window

Q.11 An alternative method is the longest-matching strategy. This method involves firing the conclusion that was derived from the _____.

A. Longest rule

B. Shortest rule

C. Complex rule

D. Forward chain rule

Q.12 Forward chaining is known as

A. Data-driven reasoning

B. Intelligence-driven reasoning

C. Goal-driven reasoning

D. Rule-driven reasoning

Q.13 Reasoning in fuzzy logic is just a matter of generalizing the familiar _____ logic.

A. Complex

B. Boolean

C. Supervised

D. Coagnitive

Q.14 Backward chaining, however, starts with the _____ and tries to reach down to all primitive nodes (marked by '?'), where information is sought from the user.

A. goal state

B. last state

C. intermediate state

D. transition state

Q.15 In CLIPS, the _____ command is used for debugging programs.

A. WATCH

B. FACT

C. CLEAR

D. DEBUG

Q.16 If you want to convert a list into a string in CLIPS, which function would you use?

A. include$

B. explode$

C. exclude$

D. implode$

Q.17 What does the exit command do in CLIPS?

A. Defines a template for structured facts.

B. Initializes the system with facts.

C. Adds a new fact to the working memory.

D. Shuts down the CLIPS environment.

Q.18 If you want to compare two String values for equality in CLIPS, which function would you use?

A. equal

B. equ

C. equa

D. eq

Q.19 What is the purpose of the length$ function in CLIPS?

A. To find the length of a string

B. To convert a string to a list

C. To concatenate two strings

D. To get the number of elements in a list

Q.20 The correct way to call the following function in CLIPS is _____. (deffunction add (?num1 ?num2) (return (+ ?num1 ?num2)))

A. (call add 5 10)

B. (add 5 10)

C. (invoke add 5 10)

D. (execute add(5, 10))

Q.21 In CLIPS, which data type is used for a sequence of characters enclosed in double quotes?

A. Boolean

B. String

C. Symbol

D. List

Q.22 Which of the following is NOT a valid data type in CLIPS?

A. Tuple

B. String

C. Void

D. Integer

Q.23 What does the mod function in CLIPS return?

A. The result of division

B. The absolute value of a number

C. The square root of a number

D. The remainder when dividing two numbers

Q.24 What data type does the value 3.14 represent in CLIPS?

A. Float

B. String

C. List

D. Integer

Q.25 Which of the following CLIPS functions is used to find the square root of a number?

A. length

B. abs

C. mod

D. sqrt

Q.26 In a straight rebuy, the buyer wants to alter product specifications, prices, terms, or suppliers.

A. True

B. False

Q.27 At a recent marketing seminar, the featured speaker stated that a target market consists of a set of buyers who share common needs or characteristics that the company decides to serve. You believe this is a correct definition.

A. False

B. True

Q.28 Decision of a single participant is enough in the business buying process.

A. True

B. False

Q.29 Karachi Gifts divides its markets into units of nations, regions, and cities. Bombay uses geographic segmentation.

A. True

B. False

Q.30 Many marketers believe that behavior variables are the best starting point for building market segments.

A. False

B. True

Q.31 The demand for many business goods tends to change more slowly than the demand for consumer goods.

A. True

B. False

Q.32 Ideally in the modified rebuy situation, the buyer does not think of changing the product specifications, price or a supplier.

A. True

B. False

Q.33 There are less participants involved in modified rebuy as compared to straight rebuy.

A. False

B. True

Q.34 Asif regularly purchasing dairy products from his nearest milk shop is an example of a straight rebuy situation.

A. True

B. False

Q.35 Shopping For The Rich and Famous is a buying service that helps wealthy clients find the best buys in exclusive clothing, high-end cars, travel, and financial services. This firm would use income segmentation.

A. True

B. False

**Q.36 Consider the code below: class class1 {   private: int i; }; class class2 : public class1 { }; Then int member i of class1 is _____ in class2. **

A. protected

B. public

**C. private **

D. static

Q.37 In case of public inheritance, protected members of base class will be _____ in derived class.

A. protected

B. private

C. hidden

D. public

Q.38 Suppose you have following C++ statements: int oldValue=10; int newValue = ++ oldValue; What will be the value of oldValue and newValue after executing above statements?

A. oldValue= 10 , newValue=10

B. oldValue= 11 , newValue=11

C. oldValue= 10 , newValue=11

D. oldValue= 11 , newValue=10

**Q.39 Consider the code below: class class1 { public: int i; }; class class2 : private class1 { }; Then int member i of class1 is _____ in class2. **

A. protected

**B. private/hidden **

C. public

D. static

Q.40 Which of the following is/are casting operator(s) in C++?

A. dynamic_cast

B. static_cast

C. All of the given options

D. const_cast

Q.41 In which of the following way(s), we can inherit a class from another class in C++?

A. Private

B. All of the given options

C. Protected

D. Public

Q.42 _____ represents "IS A" relationship.

A. Simple Association

B. Composition

C. Aggregation

D. Inheritance

Q.43 If you have three classes in a C++ program A, B, and C where class A inherits from class B, then class _____ contains all the characteristics of class _____.

A. A, C

B. A, B

C. B, C

D. B, A

**Q.44 Consider the code below: class class1 { protected: int i; }; class class2 : private class1 { }; Then int member i of class1 is _____ in class2. **

A. public

**B. private/hidden **

C. static

D. protected

Q.45 If we have not given any constructor for the class, compiler generates which of the following constructors?

A. Explicit Default Constructor

B. Explicit Parameterized Constructor

C. Implicit Default Constructor

D. Implicit Parameterized Constructor

Q.46 A Quad 1-of-4 MUX has four Multiplexers, each multiplexer has____ inputs and a single output.

A. Five

B. Four

C. Six

D. Eight

Q.47 _____ is one of the examples of asynchronous inputs.

A. Clear Input (CLR)

B. D input

C. J-K input

D. S-R input

Q.48 A _____ can not operate without a memory element.

A. counter

B. clock

C. cell

D. unit

Q.49 The latch is said to be in logic _____ state when
and Q'=1.
Q=1 and Q'=0 and it is in the logic low state when Q=0

A. high

B. constant

C. low

D. zero

Q.50 In Complex mode of GAL16V8, OLMCs can be configured in _____ ways.

A. four

B. two

C. five

D. three

Q.51 When the control line in tri-state buffer is high, the buffer operates like a _____ gate

A. XOR

B. NOT

C. AND

D. OR

Q.52 _____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.

A. Combinational Input/Output

B. Combinational Input

C. Programmable polarity

D. Combinational Output

Q.53 In gated SR latch, what is the value of the output if EN=1, S=0 and R=1?

A. Invalid

B. 0

C. Qt

D. 1

Q.54 GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a _____ with a _____.

A. column,column

B. row,column

C. column,row

D. row,row

Q.55 A mono-stable device only has a single stable state

A. True

B. False

Q.1 A 4-bit binary up/down counter is in the binary state of zero. The next state in the UP mode is

A. 0001

B. 1111

C. 1110

D. 1000

Q.2 Divide-by-32 counter can be acheived by using

A. DIV 16 and DIV 32

B. Flip-Flop and DIV 16

C. Flip-Flop and DIV 10

D. Flip-Flop and DIV 32

Q.3 In the keyboard encoder, how many times per second does the ring counter scan the key board?

A. 625 scans/second

B. 700 scans/second

C. 600 scans/second

D. 650 scans/second

Q.4 Which mechanism allocate the binary values to the states in order to reduce the cost of the combinational circuits?

A. State Evaluation

B. State Assignment

C. State Minimization

D. State Reduction

Q.5 The Test Vector definition defines the test vectors for all the three counter inputs and _____counter output/outputs.

A. Two

B. One

C. Four

D. Three

Q.6 Design of state diagram is one of many steps used to design

A. a clock

B. an UP/DOWN counter

C. a truncated counter

D. any counter

Q.7 In moore machine the output depends on

A. the current state and the output of previous flip flop

B. the current state

C. only inputs

D. the current state and inputs

Q.8 The term hold always means _____.

A. Q=0, $\bar{Q}$=0

B. Q=1, $\bar{Q}$=0

C. Q=0, $\bar{Q}$=1

D. No change

Q.9 State of flip-flop can be switched by changing its_____.

A. Momentary Signal

B. Input Signal

C. Contemporary Signal

D. Output Signal

Q.10 A 4- bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?

A. 1001

B. 1100

C. 1011

D. 0011

Q.1 A divide-by-10 Johnson counter requires

A. five flip-flops

B. twelve flip-flops

C. four flip-flops

D. ten flip-flops

Q.2 According to Moore circuit, the output of synchronous sequential circuit depend/s on _____ of flip flop.

A. External Inputs

B. Present State

C. Previous State

D. Next State

Q.3 Which mechanism allocate the binary values to the states in order to reduce the cost of the combinational circuits?

A. State Assignment

B. State Minimization

C. State Reduction

D. State Evaluation

Q.4 Once the state diagram is drawn for any sequential circuit the next step is to draw

A. Transiation table

B. Next-state table

C. Karnaugh map

D. Logic expression

Q.5 To implement the counter using S-R flip-flops instead of J-K flip-flops, the ____ transition table is used.

A. J-K

B. S-R

C. Next State

D. None of above

Q.6 Divide-by-160 counter is acheived by using

A. DIV 16 and DIV 10

B. DIV 16 and DIV 32

C. Flip-Flop and DIV 10

D. Flip-Flop and DIV 16

Q.7 Karnaugh map is used in designing

A. All of the above

B. an UP/DOWN counter

C. a counter

D. a clock

Q.8 A 4-bit binary up/down counter is in the binary state of zero. The next state in the UP mode is

A. 1111

B. 1000

C. 1110

D. 0001

Q.9 The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.

A. Combinational

B. Sequential

C. Synchronous

D. Asynchronous

Q.10 The characteristic equation of D-flip-flop implies that ____.

A. The next state is dependent on previous state

B. The next state is independent of inputs

C. The next state is independent of present state

D. The next state is dependent on present state

Q.1 When the ____ Hz sampling interval is selected, the signal at the output of the J-K flip-flop has a time period of ____ seconds.

A. 1,1

B. 0,2

C. 2,5

D. 1,2

Q.2 A divide-by-10 ring counter requires a minimum of

A. five flip-flops

B. four flip-flops

C. twelve flip-flops

D. ten flip-flops

Q.3 The 3-bit up counter can be implemented using _____ flip-flop(s).

A. S-R Flip-flops or D-Flip-flops

B. S-R Flip-flops Only

C. S-R Flip-flips and D-Flip-flops

D. D-Flip-flop Only

Q.4 A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:

A. 1000

B. 1110

C. 1111

D. 0001

Q.5 If data is brought into the J terminal and its complement to the K terminal, a J-K flip-flop operates as a(n) _____.

A. S-C flip-flop

B. D flip-flop

C. S-R flip-flop

D. N flip-flop

Q.6 To serially shift a byte of data into a shift register, there must be

A. one load pulse

B. one clock pulse for each 1 in the data

C. eight clock pulses

D. one clock pulse

Q.7 In designing any counter the transition from a current state to the next sate is determined by

A. Current state and inputs

B. Only current state

C. Only inputs

D. current state and outputs

Q.8 Three cascaded modulus-10 counters have an overall modulus of

A. 30

B. 100

C. 1000

D. 10000

Q.9 The duration for which the elevator doors are opened, and remain open, and time it takes for the elevator to move from one floor to the next can be determined by a/an_____.

A. None of the given options

B. Input Signal

C. Output Signal

D. Clock Signal

Q.10 Divide-by-32 counter can be acheived by using

A. Flip-Flop and DIV 10

B. Flip-Flop and DIV 32

C. Flip-Flop and DIV 16

D. DIV 16 and DIV 32

Q.1 The ABEL Input file can use a_____ instead of the equation to specify the Boolean expressions.

A. Truth Table

B. State Diagram

C. Logic Circuit

D. Karnaugh Map

Q.2 A divide-by-10 Johnson counter requires

A. twelve flip-flops

B. five flip-flops

C. ten flip-flops

D. four flip-flops

Q.3 Divide-by-32 counter can be acheived by using

A. Flip-Flop and DIV 16

B. Flip-Flop and DIV 10

C. Flip-Flop and DIV 32

D. DIV 16 and DIV 32

Q.4 Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause the output to _____.

A. Toggle

B. Latch

C. Reset

D. Set

Q.5 A 4- bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?

A. 1011

B. 0011

C. 1001

D. 1100

Q.6 Design of state diagram is one of many steps used to design

A. any counter

B. a truncated counter

C. an UP/DOWN counter

D. a clock

Q.7 With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in

A. 80 micro seconds

B. 10 micro seconds

C. 80 mili seconds

D. 8 micro seconds

Q.8 If data is brought into the J terminal and its complement to the K terminal, a J-K flip-flop operates as a(n) _____.

A. S-C flip-flop

B. D flip-flop

C. S-R flip-flop

D. N flip-flop

Q.9 In designing any counter the transition from a current state to the next sate is determined by

A. Current state and inputs

B. current state and outputs

C. Only inputs

D. Only current state

Q.10 A stage in the shift register consists of

A. a byte of storage

B. a latch

C. a flip flop

D. four bits of storage

Q.1 Two states are said to be equal if they have exactly same_____.

A. Next state

B. None of the given options

C. Inputs

D. Outputs

Q.2 The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.

A. Combinational

B. Sequential

C. Synchronous

D. Asynchronous

Q.3 A 4-bit binary up/down counter is in the binary state of zero. The next state in the UP mode is

A. 0001

B. 1111

C. 1000

D. 1110

Q.4 The Test Vector definition defines the test vectors for all the three counter inputs and _____counter output/outputs.

A. Four

B. One

C. Two

D. Three

Q.5 A flip-flop is presently in SET state and must remain SET on the next clock pulse. What must j and K be?

A. J = 0, K = X(Don't care)

B. J = 1, K = 0

C. J = X(Don't care), K = 0

D. J = 1, K = X(Don't care)

Q.6 When an eight bit serial in/out shift register is used for a 24 micro seconds time delay, the clock frequency must be

A. 41.67 KHz

B. 8 MHz

C. 333 KHz

D. 125 KHz

Q.7 The _____ inputs can be directly mapped to Karnaugh maps.

A. External

B. J-K

C. Flip-flop

D. S-R

Q.8 To implement the counter using S-R flip-flops instead of J-K flip-flops, the _____ transition table is used.

A. Next State

B. J-K

C. None of above

D. S-R

Q.9 Design of state diagram is one of many steps used to design

A. a truncated counter

B. an UP/DOWN counter

C. a clock

D. any counter

Q.10 Choose the best possible answer of following question:

The D flip-flop is only activated by __________.

A. Both positive & negative edge trigger

B. a positive edge trigger

C. None of the given options

D. a negative edge trigger

Q.1 The Test Vector definition defines the test vectors for all the three counter inputs and _____counter output/outputs.

A. Four

B. One

C. Two

D. Three

Q.2 In mealy machine the output depends on

A. current state and the inputs

B. None of the above

C. the current state

D. the inputs

Q.3 Three cascaded modulus-10 counters have an overall modulus of

A. 10000

B. 1000

C. 100

D. 30

Q.4 Number of states in an 8-bit Johnson counter sequence are:

A. 8

B. 16

C. 14

D. 12

Q.5 The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.

A. Combinational

B. Asynchronous

C. Synchronous

D. Sequential

Q.6 Divide-by-32 counter can be acheived by using

A. DIV 16 and DIV 32

B. Flip-Flop and DIV 32

C. Flip-Flop and DIV 10

D. Flip-Flop and DIV 16

Q.7 The 3-bit up counter can be implemented using _____ flip-flop(s).

A. S-R Flip-flips and D-Flip-flops

B. S-R Flip-flops or D-Flip-flops

C. S-R Flip-flops Only

D. D-Flip-flop Only

Q.8 The duration for which the elevator doors are opened, and remain open, and time it takes for the elevator to move from one floor to the next can be determined by a/an_____.

A. Output Signal

B. Input Signal

C. None of the given options

D. Clock Signal

Q.9 A 4- bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?

A. 1001

B. 1011

C. 1100

D. 0011

Q.10 With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in

A. 10 micro seconds

B. 80 micro seconds

C. 80 mili seconds

D. 8 micro seconds

Q.1 The Test Vector definition defines the test vectors for all the three counter inputs and _____counter output/outputs.

A. Four

B. One

C. Three

D. Two

Q.2 In the keyboard encoder, how many times per second does the ring counter scan the key board?

A. 700 scans/second

B. 625 scans/second

C. 650 scans/second

D. 600 scans/second

Q.3 A divide-by-10 Johnson counter requires

A. five flip-flops

B. four flip-flops

C. ten flip-flops

D. twelve flip-flops

Q.4 With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in

A. 8 micro seconds

B. 80 micro seconds

C. 10 micro seconds

D. 80 mili seconds

Q.5 The 3-bit up counter can be implemented using _____ flip-flop(s).

A. S-R Flip-flops or D-Flip-flops

B. D-Flip-flop Only

C. S-R Flip-flips and D-Flip-flops

D. S-R Flip-flops Only

Q.6 To parallel load a byte of data into a shift register, there must be

A. eight clock pulse

B. one clock pulse

C. one clock pulse for each 1 in the data

D. one clock pulse for each 0 in the data

Q.7 The term hold always means _____.

A. Q=1, $\bar{Q}$=0

B. Q=0, $\bar{Q}$=0

C. No change

D. Q=0, $\bar{Q}$=1

Q.8 State of flip-flop can be switched by changing its_____.

A. Output Signal

B. Input Signal

C. Contemporary Signal

D. Momentary Signal

Q.9 The ____ inputs can be directly mapped to Karnaugh maps.

A. External

B. Flip-flop

C. J-K

D. S-R

Q.10 when the transmission line is idle in an asynchronous transmission

A. It is set to logic low

B. It is set to logic high

C. State of transmission line is not used to start transmission

D. It remains in previous state

Q.1 Divide-by-32 counter can be acheived by using

A. Flip-Flop and DIV 16

B. DIV 16 and DIV 32

C. Flip-Flop and DIV 32

D. Flip-Flop and DIV 10

Q.2 The duration for which the elevator doors are opened, and remain open, and time it takes for the elevator to move from one floor to the next can be determined by a/an_____.

A. None of the given options

B. Input Signal

C. Output Signal

D. Clock Signal

Q.3 when the transmission line is idle in an asynchronous transmission

A. State of transmission line is not used to start transmission

B. It is set to logic low

C. It remains in previous state

D. It is set to logic high

Q.4 To implement the counter using S-R flip-flops instead of J-K flip-flops, the ____ transition table is used.

A. J-K

B. Next State

C. None of above

D. S-R

Q.5 A divide-by-10 Johnson counter requires

A. five flip-flops

B. four flip-flops

C. twelve flip-flops

D. ten flip-flops

Q.6 Which mechanism allocate the binary values to the states in order to reduce the cost of the combinational circuits?

A. State Assignment

B. State Minimization

C. State Reduction

D. State Evaluation

Q.7 In designing any counter the transition from a current state to the next sate is determined by

A. current state and outputs

B. Only inputs

C. Only current state

D. Current state and inputs

Q.8 The characteristic equation of D-flip-flop implies that ____.

A. The next state is independent of present state

B. The next state is dependent on previous state

C. The next state is independent of inputs

D. The next state is dependent on present state

Q.9 The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.

A. Combinational

B. Synchronous

C. Asynchronous

D. Sequential

Q.10 With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in

A. 8 micro seconds

B. 10 micro seconds

C. 80 micro seconds

D. 80 mili seconds

CS302 - Quiz No.04

Date: 07 January 2026

Q.1 Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause the output to _____.

A. Latch

B. Reset

C. Set

D. Toggle

Q.2 Design of state diagram is one of many steps used to design

A. an UP/DOWN counter

B. a clock

C. any counter

D. a truncated counter

Q.3 In moore machine the output depends on

A. only inputs

B. the current state

C. the current state and the output of previous flip flop

D. the current state and inputs

Q.4 A 4-bit binary up/down counter is in the binary state of zero. The next state in the UP mode is

A. 1111

B. 1000

C. 1110

D. 0001

Q.5 To implement the counter using S-R flip-flops instead of J-K flip-flops, the ____ transition table is used.

A. Next State

B. None of above

C. J-K

D. S-R

Q.6 The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.

A. Asynchronous

B. Synchronous

C. Combinational

D. Sequential

Q.7 Karnaugh map is used in designing

A. a counter
B. a clock
C. an UP/DOWN counter
D. All of the above

Q.8 The characteristic equation of D-flip-flop implies that ____.

A. The next state is dependent on present state
B. The next state is independent of present state
C. The next state is independent of inputs
D. The next state is dependent on previous state

Q.9 A divide-by-10 Johnson counter requires

A. five flip-flops
B. ten flip-flops
C. four flip-flops
D. twelve flip-flops

Q.10 State of flip-flop can be switched by changing its_____.

A. Input Signal
B. Momentary Signal
C. Output Signal
D. Contemporary Signal

Q.1 When an eight bit serial in/out shift register is used for a 24 micro seconds time delay, the clock frequency must be

A. 125 KHz

B. 333 KHz

C. 8 MHz

D. 41.67 KHz

Q.2 The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.

A. Asynchronous

B. Combinational

C. Synchronous

D. Sequential

Q.3 According to Moore circuit, the output of synchronous sequential circuit depend/s on _____ of flip flop.

A. Previous State

B. Present State

C. External Inputs

D. Next State

Q.4 Design of state diagram is one of many steps used to design

A. a clock

B. an UP/DOWN counter

C. a truncated counter

D. any counter

Q.5 In the keyboard encoder, how many times per second does the ring counter scan the key board?

A. 700 scans/second

B. 650 scans/second

C. 600 scans/second

D. 625 scans/second

Q.6 The ____ inputs can be directly mapped to Karnaugh maps.

A. J-K

B. S-R

C. External

D. Flip-flop

Q.7 A stage in the shift register consists of

A. a byte of storage

B. a latch

C. four bits of storage

D. a flip flop

Q.8 In mealy machine the output depends on

A. the current state

B. None of the above

C. current state and the inputs

D. the inputs

Q.9 A 4-bit binary up/down counter is in the binary state of zero. The next state in the UP mode is

A. 1110

B. 1111

C. 0001

D. 1000

Q.10 If data is brought into the J terminal and its complement to the K terminal, a J-K flip-flop operates as a(n) _____.

A. N flip-flop

B. D flip-flop

C. S-R flip-flop

D. S-C flip-flop
