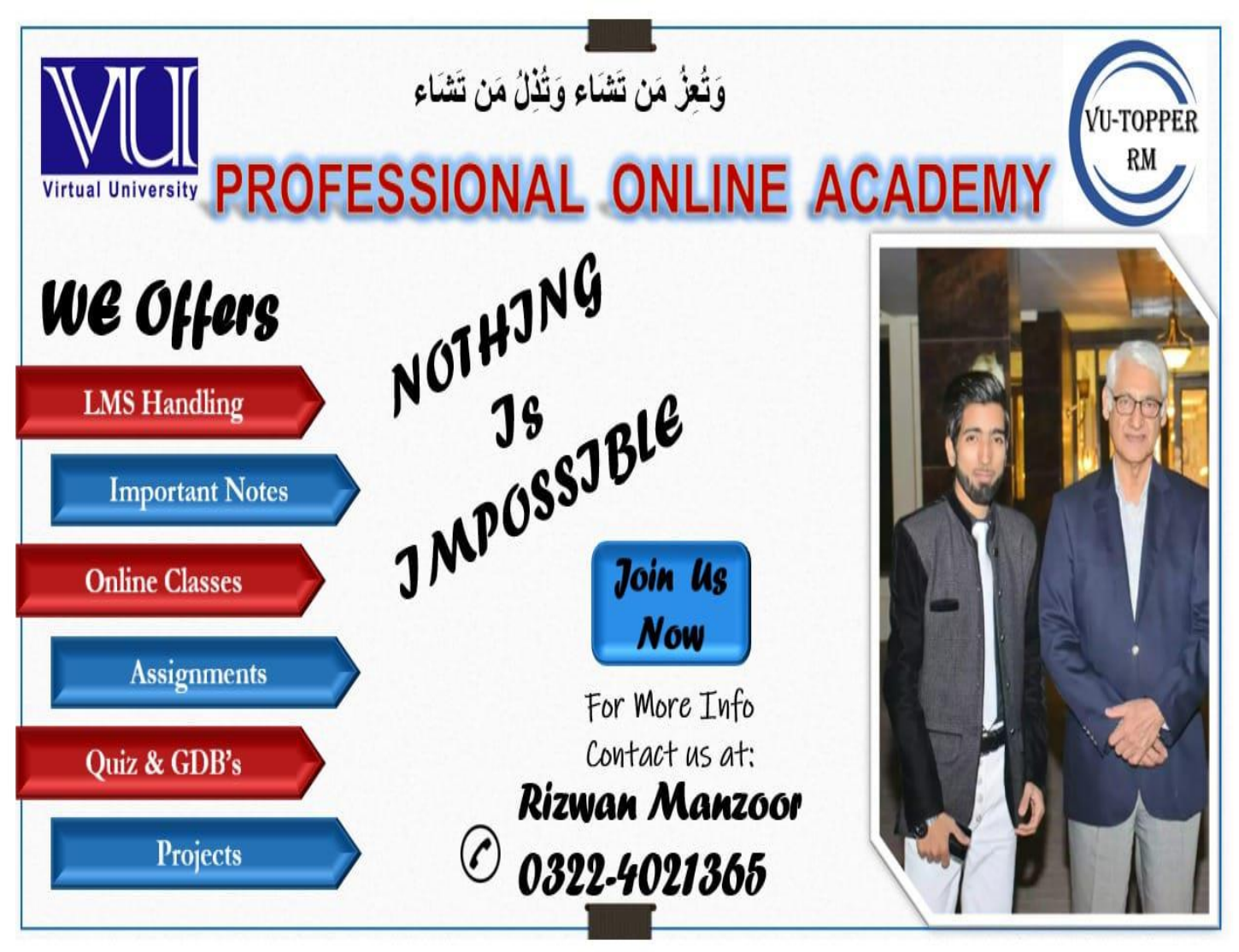
CS-501 Advanced Computer Architecture

Update MCQS For Quiz-4 File

Solve By Vu Topper RM

85% To 100% Marks



بری صحبت سے تنہائی بہتر ہے اور تنہائی سے نیک صحبت بہتر ہے

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Adding a data pin to a chip with 2^m words of s bits increases the number of bits it can store by only a factor of _____

A. s/(s+1)
B. s^2/s
C. (s+1)/s Page 320
D. (s+2)/s

The_____is m-bits wide and contains memory address generated by the CPU directly connected to the m-bit wide address bus Booth Recording

A. Program counter (PC)
B. Instruction Register(IR)
C. memory Buffer Register(MBR)
D. memory address register (MAR) Page 316

_____ is a read-mostly memory that can be written into at any time without erasing prior contents

A. PROM
B. EPROM
C. EEPROM Page 321
D. Main memory

By which file extension does the FALCON-A Assembler loads a FALCON-A assembly file?

A. .src
B. .exe
C. .org
D. .asmfa Page 08

The conversion of numbers from a representation in one base to another is known as_____

A. Radix Conversion Page 301
B. Number Representation
C. Decimal representation

D. Hexadecimal Representation

In Single-Precision Binary Floating Point Representation the exponent is _____

A. 1 bit
B. 8 bits **Page 313**
C. 11 bits
D. 23 bits

In 1x8 memory cell arrangement, each block is connected through a bi-directional data bus implemented with _____ tri-state buffer(s).

A. 1
B. 2 **Page 317**
C. 4
D. 8

Taking control of the system bus for a few bus cycles is known as _____.

A. Bus Stealing
B. None of given
C. Cycle Stealing **Page 288**
D. Cycle Transfering

_____ is nonvolatile and may be written into only once.

E. PROM **Page 321**
F. EPROM
G. EEPROM
H. Main memory

human works with base 10 and computers work with base _____.

A. 2 **Page 316**
B. 8
C. 10
D. 16

The main issue/s in error control is/are_____.

A. Correction of Error
B. Avoidance of Error
C. Detection of Error
D. Both Detection of Error and Correction of Error
Google

Adding an address pin to a memory chip increases the capacity of memory by a factor of _____.

A. 2 **Page 320**
B. 3
C. 1.5
D. 2.5

_____ is much faster than EPROM.

A. Rom
B. Hard disk
C. Flash Memory **Page 321**
D. Main memory

The _____ is w-bit wide and contains a data word, directly connected to the data bus which is b-bit wide memory address register (MAR) .

A. Program counter (PC)
B. Instruction Register(IR)
C. memory Buffer Register(MBR) **Page 316**
D. memory address register (MAR)

The information about interrupt vector is given in 8-bits, from bit 0 to 7, which is translated to bit _____ on the data bus.

A. 0 to 7
B. 8 to 15

C. 16 to 23 **Page 260**

D. 11 to 18

For _____ of an error we just need to know that there exists an error.

A. Detection **Page 297**

B. Correction

C. None of the given

D. Both Correction and Detection

Which is a status bit that indicates whether the block in cache has been modified or not modified?

A. End bit

B. Dirty bit **Page 327**

C. Access bit

D. Presence bit

Which I/O technique will be used by a sound card that may need to access data stored in the computer's RAM?

A. Polling

B. Programmed I/O

C. Interrupt driven I/O

D. Direct memory access(DMA) **Page 271**

A 16k×4 Static RAM Chip is arranged in the form of four _____ memory cells.

A. 4×16

B. 16×4

C. 64×256 **Page 318**

D. 256×256

A typical one level decoder has _____ input(s) and _____ output(s).

n, n

n, 2^n Page 318

2^n, n

n, n^2

When a particular sector is found, the data is transferred to _____.

A. RAM

B. I/O module Page 293

C. Cache memory

D. Instruction register

_____ is the concept in which a process is copied into the main memory from the secondary memory according to the requirement.

A. Paging

B. Segmentation

C. Logical Partition

D. Demand Paging Page 329

What is the basic idea of “carry look ahead”?

A. To reduce congestion

B. To solve the redundancy

C. To speed up the ripple carry Page 308

D. To synchronize with CPU clock

Given an m-digit base b number x, the _____ of x is xc=(bm−x)modbm

A. Radix Compliment Page 304

B. Biased Representation

C. Signed Magnitude Form

D. Diminished Radix Compliment

_____ is the simplest form for representing a signed number

A. None of the given

B. Sign Magnitude Form Page 304

C. Biased Representation
D. Diminished Radix Compliment Form

Each memory reference issued by the CPU is translated from the logical address space to _____.
A. Virtual Address
B. Cache Address
C. Physical Address Page 328
D. Effective Address

When an I/O module has a capability of executing a specific set of instructions for specific I/O devices in the memory without the involvement of CPU is called _____.
A. I/O Channel Page 291
B. Cycle Stealing
C. I/O processors
D. Selector Channel

_____refers to the fact when a given address has been referenced, the next address is highly probable to be accessed within a short period of time
A. Full Locality
B. Half Locality
C. Spatial Locality Page 322
D. Temporal Locality

_____ depends upon the present position of the head and the position of the required sector.
A. Seek time Page 293
B. Throughput
C. Execution time
D. Direct memory Access

The Memory Management unit (MMU) is located between _____ and _____.

A. ROM and RAM
B. The CPU and the physical memory Page 328
C. Main memory and secondary memory
D. Secondary memory and Virtual memory

_____ is non volatile i-e it retains the information in it when power is removed from it

A. ROM Page 230
B. RAM
C. Cache
D. Hard disc

Along with the information bits, we add up another bit, which is called?

A. Start bit
B. Stop bit
C. Parity bit Page 297
D. Header bit

_____chips have quartz windows and by applying ultraviolet light data can be erased from them.

A. PROM
B. EPROM Page 321
c. EEPROM
D. Flash Memory

For write to complete in Write through, the CPU has to wait. This wait stateis called _____.

A. Write Stalls Page 327
B. Cache Miss
C. Write Buffer
D. Write Allocate

CRC has ---------- overhead as compared to Hamming code.

A. Equal
B. Lesser **Page 298**
C. Greater
D. None of the given

A component connected to the _____ and with which the master component can communicate during a particular bus cycle. Normally the CPU with its bus control logic is the master component.

A. System bus **Page 288**
B. Bus component
C. Slave component
D. Master component

The _____ can be determined from the number of platters and the number of tracks.

A. Latency
B. execution time
C. storage capacity **Page 293**
D. Speed of processing

_____ is a combination of arithmetic, logic and shifter unit along with some multiplexers and control unit.

A. ALU **Page 313**
B. Flip Flop
C. Control Unit
D. Barrel Rotator

---------- allows a peripheral to read and write memory without intervention by the CPU.

A. Polling
B. Programmed I/O
C. Interrupt driven I/O

D. Direct memory access(DMA) **Page 287**

What should be the behavior of interrupts during critical sections?

A. Must remain Enable
B. Must remain Disable **Page 197**
C. Depends on current situation
D. Only important interrupts be enable.

The Direct memory access (DMA) scheme results in direct link between _____ and _____,

A. Cache memory and Registers
B. the CPU and the physical memory
C. Secondary memory and Virtual memory
D. main memory and secondary memory **Page 331**

The register file is a collection of _____bit wide registers used for data transfer between memory and the CPU .

A. 16
B. 64
C. 32 **Page 316**
D. 8

Dirty bit is a status bit which is used to indicate whether _____.

A. The block is valid or not
B. The block is accessible or not
C. The block has been modified or not **Page 327**
D. The block has been accessed frequently or not

In computers,floating-point representation uses _____to encode significand,exponent and their sign in a single word

A. Octal Number
B. Binary Numbers **Page 313**
C. Decimal Numbers

D. Hexa decimal Numbers

Shifting of the radix point towards left or right is called _____

A. Scaling **Page 302**
B. Shifting
C. Right Shift
D. Logical Shift

_____ is said to occur when a 0 is received instead of a stop bit.

A. Parity Error
B. Block Error
C. Framing Error **Page 221**
D. Over-run Error

_____ hazard occurs when attempting to access the same resource in different ways at the same time

A. Data
B. Branch
C. Structural **Page 198**
D. Instruction

_____ controls the sequence of the flow of microinstructions.

A. Multiplexer
B. DMA Controller
C. Virtual Memory
D. Micro program controller **Page 208**

The multiplexer_____ is used to decide which value is transferred to be written back to the register file.

A. MP2
B. MP3
C. MP4

D. MP5 Page 195

Pipeline hazard occurs when an instruction depends on the result of _____ instruction that is not yet complete.

A. First
B. Next
C. Previous Page 198
D. Ongoing

Connection to a CPU that provides a data path between the CPU and external devices, such as a keyboard, display, or reader is called----------

A. I/O port
B. Buffer
C. Processor
D. Memory mapping

Why DMA is faster than Programmer I/O technique because?

A. DMA uses buffers with CPU
B. DMA uses interrupted driven I/O
C. DMA transfers data directly using CPU.
D. DMA transfers data directly without using CPU Google

_____ signal is used in printer with DB-25 interface to reset its controller.

A. #PE
B. #INIT
C. #SLCT
D. #STROB

How can you define an interrupt?

A. A process where input devices can takeover the working of the microprocessor
B. A process where memory can speed up programs execution speed

C. A process where an external device can speedup the working of the microprocessor

D. A process where an external device can get the attention of the microprocessor

Below given RTL description belongs to which stage of pipe-lining?
IR2 ← M [PC];
PC2 ← PC+4;

A. Memory Access
B. Instruction Fetch
C. ALU Operation
D. Instruction Decode

Identify the following type of serial communication error condition:
"The prior character that was received was not still read by the CPU and is over written by a new received character."

A. Parity error
B. Framing error
C. Overrun error **Page 240**
D. Under-run error

Super-scalar processor divides the instructions into _____ classes.

A. 4
B. 3
C. 2
D. 5

The _____ instruction is completed once memory access has been made and the memory location has been written to.

A. Store **Page 192**
B. Link
C. Branch
D. Control

_____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.

A. Pipelining
B. Partial decoding Page 235
C. Microprogramming
D. Instruction pre-fetching

_____ form the control signal field in the micro instruction.

A. A bits
B. B bits
C. C bits Page 206
D. D bits

A combination of parallel and sequential hardware used to build a multiplier is known as _____

A. Booth Recording
B. Parallel Array Multiplier
C. Series Parallel Multiplier Page 379
D. None of the these

The cache contains a copy of portions of the _____.

A. ROM
B. EPROM
C. Flash Memory
D. Main memory Page 321

When _____ signal is high, this would correspond to a read operation equivalent to having an input data to the CPU and output from the memory.

A. R/W Page 316
B. REQUEST
C. COMPLETE
D. None of the given

Every interrupt handler has an interrupt return (IRET) instruction, this instruction is an example of _____ return.

A. FAR
B. NEAR
C. SHORT
D. RELATIVE

In which one of the following methods, does the CPU poll to identify the interrupting module and branches to an interrupt service routine on detecting an interrupt?

A. Daisy chain
B. Software poll
C. Multiple interrupt lines
D. All of given option

_____ are computed by the ALU and stored in processor status register.

A. Condition codes Page 311
B. Fraction Division
C. Conditional Branches
D. None of the given

Raid Level ____ is not a true member of the RAID family.

A. 0 Page 365
B. 1
C. 2
D. 3

A very large page size results in increased_____.

A. Delay
B. Through put
C. Access time Page 330
D. Execution time

Every time you press a key, an interrupt is generated.

A. Software interrupt
B. Hardware interrupt **Page 275**
C. None of the given
D. All of the given

What is the status of the ACKNLG# signal when a character is completely received by the printer?

A. It toggles its state
B. It remains unaffected
C. It goes from low to high
D. It goes from high to low **Page 239**

A _____signal decides whether the input word should be shifted or bypassed.

A. Shift/bypass **Page 384**
B. Control Read
C. Control Write
D. None of the given

In virtual memory mechanism, pages are formulated in the _____ memory and brought into the _____ memory.

A. Main, cache
B. Main, secondary
C. Secondary, main **Page 328**
D. Secondary, cache

Along with information bits we add up another bit which is called the_____bit.

A. CRC
B. Parity **Page 328**
C. Hamming
D. Error Detection

Select the parts of a hard disk.

A. Header only
B. Data section only
C. Data section and a trailer
D. Header, data section and a trailer

If a character is not available at the beginning of an interval, an _____ is said to occur.

A. Parity Error
B. Framing Error
C. Overrun Error
D. Under-run Error Page 262

In which technique does the hardware directly access host memory for reading or writing independent of CPU?

A. Polling
B. Programmed I/O
C. Interrupt driven I/O
D. Direct Memory Access (DMA)

Most parallel I/O ports used with peripheral devices are mapped on a range of_____.

A. Cache
B. Bus addresses
C. Contiguous addresses Page 287
D. Direct memory access

How does DMA saves CPU time?

A. By periodically polling
B. By issuing a interrupt request to the CPU to request attention
C. By storing all data in a buffer to be later transferred to the CPU
D. By controlling transfer between I/O devices and memory directly

_____ form the branch control field in the micro instruction.

A. A bits
B. B bits Page 206
C. M bits
D. D bits

A parallel port can be considered to be a big _____ gate.

A. OR
B. AND ok
C. NOR
D. NOT

_____ lets the user execute the program, one instruction at a time.

A. Execute
B. List File
C. Change PC
D. Single Step Page 7

For input ports, the incoming data should be placed on the data bus only during the I/O read bus cycle. For this purpose, _____ are used.

A. Flip Flops
B. Registers
C. AND Gates
D. Tri-state Buffers ok

At the start of the transfer operation in synchronous communication, the master activates the _____ signal.

A. Data
B. Read
C. Enable
D. Acknowledge

The directive _____ is used to define variables.

A. .db
B. .exe
C. .org
D. .equ

---------- is the time needed by the CPU to recognize (not service) an interrupt request.

A. Throughput
B. Timer delay
C. Interrupt Latency Page 256
D. Response Deadline

_____hazard occurs when an instruction attempts to access some data value that has not yet been updated by the previous instruction.

A. Data Page 198
B. Branch
C. Structural
D. Instruction

In _____, a separate address space of the CPU is reserved for I/O operations.

A. All of above
B. Isolated I/O Page 217
C. None of above
D. Memory Mapped I/O

The Pentium does allow the use of some part of its _____ accumulator register EAX

A. 8 bits
B. 16 bits
C. 32 bits Page 230
D. 64 bits

A collection of ----------is called a micro program.

A. DMA
B. Registers
C. Microinstructions Page 205
D. large scale operations

_____ is an electrical pathway through which the processor communicates with the internal and external devices attached to the computer.

A. DISK
B. Hazard
C. Memory
D. Computer Bus

Where does the processor store the address of the first instruction of the ISR?

A. Interrupt handler
B. Interrupt request
C. Interrupt vector Page 277 ok
D. All of the given options

_____ signal has input direction with respect to printer

A. PE#
B. BUSY
C. ACKNLG#
D. STROBE#

Identify the following type of serial communication error condition in which no character is available at the beginning of an interval.

A. Parity error
B. Overrun error
C. Framing error
D. Under-run error Page 240

_____ form the branch address field in the micro instruction.

A. A bits
B. B bits
C. M bits Page 206 ok
D. D bits

_____ is/are example(s) of synchronous communication.

A. All of the given
B. Register to Memory
C. Memory to Memory
D. Register to Register

ET = _____.

A. CPI x IC/T
B. CPI / IC x T
C. CP x IC x T
D. CPI x IC x T Page 118

To set the value of micro-PC from external address, the value of 4 to 1 multiplexer is _____.

A. 00
B. 01
C. 10
D. 11

Tri-state buffers are used for removing _____.

A. bus collision
B. bus contention
C. Instruction collision
D. Instruction contention

Which of the following pins of processor is designated for maskable interrupts?

A. MI

B. NMI
C. RINT
D. INTR

Which one of the following is NOT a technique used when the CPU wants to exchange data with a peripheral device?

A. Virtual Memory Page 268
B. Programmed I/O
C. Interrupt driven I/O
D. Direct Memory Access (DMA)

Which is the last instruction of the ISR that is to be executed when the ISR terminates?

A. INT
B. IRQ
C. NMI
D. IRET Page 255

In the little-endian format exchanging data between computers, the data transmitted by one will be received in a “swapped” form by the other.

A. Signals
B. Swapped Google
C. Arranged
D. Organized

Identify the type of serial communication error condition in which "0" is received instead of a stop bit (which is always a "1")?

A. Parity error
B. Overrun error
C. Framing error Page 240
D. Under-run error

_____ means that the CPU should input data from an input device only when the device is ready to provide data and send data to an output device only when it is ready to receive data.

A. Data transfer
B. Data location
C. Data synchronization Page 218
D. Asynchronous transmission

The third stage of the Pipelined version of SRC is;

A. Register write
B. ALU operation Page 190
C. Memory access
D. Instruction Fetch

A _____ processor is based on a very long instruction word.

A. SRC
B. VLIW Page 202
C. FALCON-E
D. FALCON-A

In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?

A. Parallel
B. Asynchronous
C. Semi-synchronous
D. Daisy-Chaining Priority

_____ signal has Output direction with respect to printer

A. INIT#
B. D<7..0>
C. STROBE#

D. ACKNLG#

Interrupt driven I/O is better than _____.

A. Stall
B. Polling Page 259
C. First In First Out
D. Data Forwarding

From an n bit control word we may have _____ bit signal values.

A. Nxn
B. n^2
C. 2^n Page 210
D. 2xn

The source file of FALSIM should contain _____ text only.

A. UFT
B. ANSI
C. ASCII Google
D. Unicode

_____ usually involves calculating the target address and evaluating a condition.

A. Pipelined SRC
B. ALU instructions
C. Branch Instructions Page 193
D. Load/Store instructions

The SRC uses a hazard detection unit. The hazard can be resolved using either pipeline stalls or by _____.

A. Data forwarding Page 199
B. Data compressing
C. Instruction handling
D. Instruction forwarding

Connection to a CPU that provides a data path between the CPU and external devices, such as a keyboard, display, or reader is called----------

A. Buses
B. Program
C. Processor
D. Memory address

Which temporary register is loaded with either a register value from the register file or a constant from the instruction?

A. Z4
B. X3
C. Y3 Page 191 ok
D. Z5

Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?

A. Parallel Priority
B. Asynchronous Priority
C. Daisy-Chaining Priority
D. Semi-synchronous Priority

VLIW stands for _____.

A. Very Long Instruction Word
B. Very Long Instruction Width
C. Variable Length Instruction Width
D. Variable Length Instruction Word Page 202

Which of the following is not True regarding serial communication?

A. Slow
B. High cost
C. Inefficient
D. Easy to implement.

In a printer with DB-25 interface, _____ signal is is better for edge triggered systems.

A. PE#
B. BUSY#
C. STROB#
D. ACKNLG# Page 242

Which of the followings is not an example of super-scalar processors?

A. Intel P6
B. IAPX88
C. PowerPC 601
D. DEC Alpha 21164

A software routine performed when an interrupt is received by the computer is called as ---------

A. Trap
B. Interrupt
C. Exception
D. Interrupt handler

An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.

A. Memory
B. Flip Flops
C. Multiplexers
D. Peripheral devices Page 216

For More Important Notes
Channel Name = #VuTopperRM

بری صحبت سے تنہائی بہتر ہے اور تنہائی سے نیک صحبت بہتر ہے