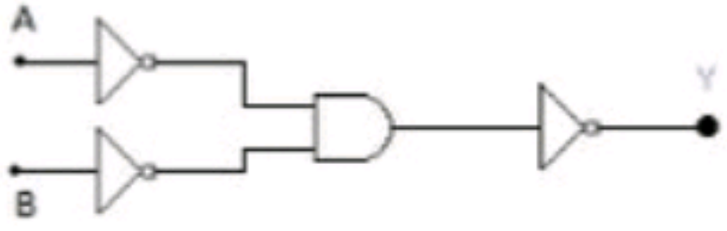
CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 01)

Question # 1 of 5 (Start time: 08:13:57 PM, 26 April 2024)

What will be the Boolean Equation for (Y) for the given Gate Level Diagram.



Select the correct option

○	$A'B'$
○	$A'B$
○	$A + B$
●	$A' + B$

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 02)

Question # 4 of 5 (Start time: 03:50:49 PM, 03 May 2024)

DE Morgan's Theory is used to convert _____ gates to _____ones.

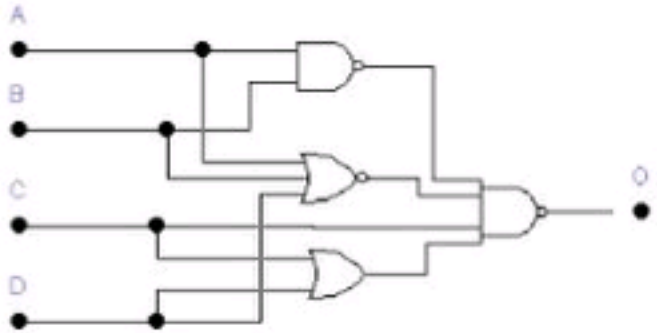
Select the correct option

○	AND/XOR, XOR/AND
○	AND/OR, NOR/NAND
○	AND/NAND, OR/NOR ✓
○	OR/NOT, NOT/OR

CS302P - Digital Logic Design (Practical) (Semester Quiz # 01 (Graded))

Question # 10 of 10 (Start time: 10:12:16 AM, 07 May 2024)

What will be the simplified Boolean Expression of the stated Gate Level Diagram.



Select the correct option

- ○ A + B + C' + D
- ○ A + B' + C' + D
- ◉ A' + B' + C' + D

CS302P - Digital Logic Design (Practical) (Semester Quiz # 02 (Graded))

Question # 3 of 10 (Start time: 10:01:14 AM, 23 May 2024)

In EWB, logic 1 is represented by using the _____ line

Select the correct option

- (●) V_{CC}
- ( ) -V
- ( ) Ground
- ( ) V_{DD}

CS302P - Digital Logic Design (Practical) (Semester Quiz # 01 (Graded))

Question # 8 of 10 (Start time: 10:10:34 AM, 07 May 2024)

To draw a logic circuit for boolean expression **AB'+C**, how many gates are used?

Select the correct option

○	4
○	2
○	3 ✓
○	1

CS302P - Digital Logic Design (Practical) (Semester Quiz # 02 (Graded))

Question # 10 of 10 (Start time: 10:09:27 AM, 23 May 2024)

_____ gate with a bubble at the output is know as NOR gate.

Select the correct option

- ○ NOT
- ○ AND
- ○ NAND
- ◉ OR

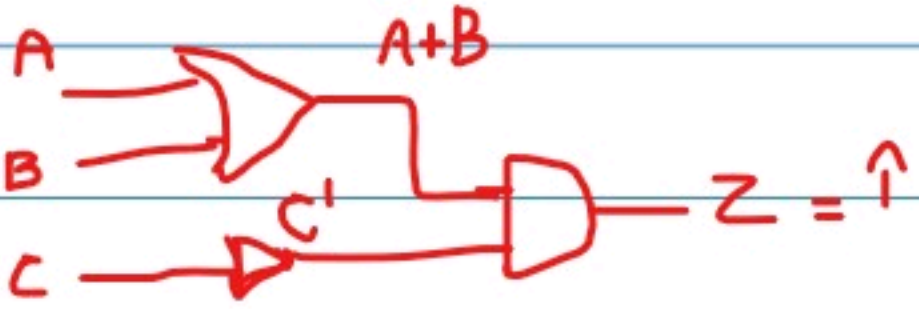
CS302P - Digital Logic Design (Practical) (Semester Quiz # 02 (Graded))

Question # 5 of 10 (Start time: 10:04:21 AM, 23 May 2024)

The Boolean function **Z = A + B . C'** can be implemented in digital logic circuit by connecting _____ gates together.

Select the correct option

○	1
○	3 ✓
○	4
○	2



CS302P - Digital Logic Design (Practical) (Semester Quiz # 02 (Graded))

Question # 4 of 10 (Start time: 10:02:47 AM, 23 May 2024)

According to De-Morgan's law, which of the following is **TRUE**?

Select the correct option

- $A \cdot B = (A' \cdot B')'$
- $(A + B)' = (A' + B')'$
- $A + B = (A' \cdot B')'$
- $A + B = (A + B)'$

CS302P - Digital Logic Design (Practical) (Semester Quiz # 02 (Graded))

Question # 2 of 10 (Start time: 09:59:41 AM, 23 May 2024)

According to the commutative law of Boolean algebra, which of the following expression is **TRUE**?

Select the correct option

- ○ $A.B = A+B$
- ● $A.B = B.A$
- ○ $A.B' = A'.B$
- ○ $A'.B' = A.B$

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 9)

Question # 2 of 5 (Start time: 10:35:27 AM, 05 July 2024)

An identify comparator is defined as a digital comparator which has _____

Select the correct option

○	Three output terminals
○	Only one output terminal
○	No output terminals
◉	Two output terminals

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 9)

Question # 4 of 5 (Start time: 10:36:54 AM, 05 July 2024)

Which of the following is an invalid BCD code?

Select the correct option

- 1001
- 1101 , 1010 , 1011 , 1100 , 1110 , 1111
- 0011
- 0101

The Gray Code

The Gray code does not have any weights assigned to its bit positions. The Gray Code is not a positional code. The Gray code is different from the unsigned binary code as successive values of Gray code differ by only one bit. Table 4.5 shows the Gray Code representation of Decimal numbers 0 to 9.

Decimal	Gray	Binary
0	0000	0000
1	000**1**	0001
2	00**1**1	0010
3	001**0**	0011
4	0**1**10	0100
5	011**1**	0101
6	01**0**1	0110
7	010**0**	0111
8	**1**100	1000
9	110**1**	1001

Table 4.5 Gray Code representation of Decimal values

The bits in **bold** change in successive values of Gray code representation

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 9)

Question # 1 of 5 (Start time: 10:34:45 AM, 05 July 2024)

Convert the binary number 1100 to Gray code.

Select the correct option

○	1010
◉	1000
○	0111
○	0101

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 8)

Question # 3 of 5 (Start time: 11:24:02 AM, 28 June 2024)

A decimal counter has _____ states.

Select the correct option

○	7
◉	10
○	2
○	9

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 8)

Question # 2 of 5 (Start time: 11:22:30 AM, 28 June 2024)

Why do we use Gray Code?

Select the correct option

- ○ Error Detection
- ◉ Error Correction
- ○ To count the number or bit changes
- ○ Invert the code

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 8)

Question # 1 of 5 (Start time: 11:21:58 AM, 28 June 2024)

Comparators are used in _____

Select the correct option

○	Memory
◉	CPU
○	Motherboard
○	Hard Drive

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04 (Graded))

Question # 8 of 10 (Start time: 11:56:58 PM, 03 July 2024)

A full adder circuit takes _____ bit(s) as input and returns _____ bit(s) as output.

Select the correct option

○	2, 1
◉	3, 2
○	2, 2
○	3, 1

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04 (Graded))

Question # 7 of 10 (Start time: 11:56:39 PM, 03 July 2024)

Which of the following is the modified code of Excess-3 code?

Select the correct option

- (●) Gray Code
- ( ) ASCII
- ( ) EBDIC
- ( ) BCD

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04 (Graded))

Question # 7 of 10 (Start time: 11:56:39 PM, 03 July 2024)

Which of the following is the modified code of Excess-3 code?

Select the correct option

- (●) Gray Code
- ( ) ASCII
- ( ) EBDIC
- ( ) BCD

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04 (Graded))

Question # 6 of 10 (Start time: 11:55:51 PM, 03 July 2024)

To create a Johnson Counter by using D-flip flops, how flip flops should be connected together?

Select the correct option

○	Q output of previous flip flop should be connected to D input of second flip flop
○	Q output of previous flip flop should be connected to clock input of second flip flop
◉	Q' output of previous flip flop should be connected to D input of second flip flop
○	Q' output of previous flip flop should be connected to clock input of second flip flop

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04 (Graded))

Question # 5 of 10 (Start time: 11:55:32 PM, 03 July 2024)

How many flop flops are required to create a counter circuit which can count from 0 to 7?

Select the correct option

○	2
○	4
○	1
◉	3

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04 (Graded))

Question # 4 of 10 (Start time: 11:55:08 PM, 03 July 2024)

Which of the following symbols is used to represent XOR operation?

Select the correct option

○	^
○	x
○	+
◉	⊕

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04 (Graded))

Question # 1 of 10 (Start time: 11:53:57 PM, 03 July 2024)

The parallel outputs of a counter circuit represent the _____

Select the correct option

- ○ Clock frequency
- ○ Parallel data word
- ◉ Clock count
- ○ Counter modulus

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04 (Graded))

Question # 2 of 10 (Start time: 11:54:12 PM, 03 July 2024)

Ripple counters are also called _____

Select the correct option

- ○ SSI counters
- ○ Synchronous counters
- ○ VLSI counters
- ● Asynchronous counters

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04 (Graded))

Question # 8 of 10 (Start time: 11:56:58 PM, 03 July 2024)

A full adder circuit takes _____ bit(s) as input and returns _____ bit(s) as output.

Select the correct option

○	2, 1
◉	3, 2
○	2, 2
○	3, 1

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 (Graded))

Question # 1 of 10 (Start time: 10:11:50 AM, 26 June 2024)

The K-map based Boolean reduction is based on the following Unifying Theorem: A + A' = 1.

Select the correct option

- (●) Non Impact
- ( ) Impact
- ( ) Complementarity
- ( ) Force

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 (Graded))

Question # 5 of 10 (Start time: 10:14:27 AM, 26 June 2024)

In order to build an XOR gate using NAND gates only, _____ gate(s) are required.

Select the correct option

○	4
◉	2
○	3
○	1

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 (Graded))

Question # 4 of 10 (Start time: 10:14:12 AM, 26 June 2024)

There are _____ cells in a 4-variable K-map.

Select the correct option

○	24
◉	16
○	8
○	20

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 (Graded))

Question # 3 of 10 (Start time: 10:13:51 AM, 26 June 2024)

A Karnaugh map (K-map) is an abstract form of _____ diagram organized as a matrix of squares.

Select the correct option

○	Triangular Diagram
◉	Venn Diagram
○	Block diagram
○	Cycle Diagram

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 (Graded))

Question # 2 of 10 (Start time: 10:13:05 AM, 26 June 2024)

In a full adder circuit having inputs **A = 1, B =1, Cin = 0**, the outputs **S** and **Cout** will be _____.

Select the correct option

○	S = 1, Cout = 1
○	S = 0, Cout = 0
○	S = 1, Cout = 0
◉	S = 0, Cout = 1

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 (Graded))

Question # 8 of 10 (Start time: 10:15:59 AM, 26 June 2024)

In 8x1 multiplexer, which one of the following lines must always be connected to ground in order to activate the mutiplexer?

Select the correct option

○	Y
○	W
◉	G`
○	Vcc

Half-Adder Sum & Carry Out Boolean Expressions

The Sum and Carry Out expressions of the Half-Adder can be determined from the function table. The Half-Adder Sum and Carry Out outputs are defined by the expressions

$$Sum = \overline{A}B + A\overline{B} = A \oplus B$$
$$CarryOut = AB$$

Half-Adder Logic Circuit

The Half-Adder Logic Circuit can be directly implemented from the Sum and Carry Out Boolean expressions. Figure 14.6

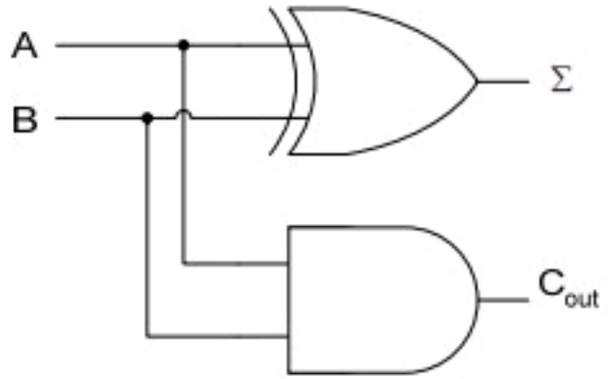


Figure 14.6 Half-Adder Logic Circuit

2. Full-Adder

A Full-Adder can be fully described in terms of its Function table, its Sum and Carry Out Boolean Expressions and the circuit Implementation.

Full-Adder Function Table

The Full-Adder has a 3-bit input and a 2-bit output. The function table of the Full-Adder

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 (Graded))

Question # 6 of 10 (Start time: 10:14:45 AM, 26 June 2024)

When implementing a half adder by using gates, which of the following gates is used to return carry bit as an output?

Select the correct option

○	OR
○	XOR
○	NAND
○	AND

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 (Graded))

Question # 9 of 10 (Start time: 10:16:58 AM, 26 June 2024)

When implementing a half adder by using gates, which of the following gates is used to give Sum (S) as an output?

Select the correct option

○	OR
○	AND
◉	XOR
○	NOR

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 (Graded))

Question # 10 of 10 (Start time: 10:17:16 AM, 26 June 2024)

There are _____ cells in a 5-variable K-map.

Select the correct option

- ○ 32
- ○ 24
- ○ 64
- ○ 16

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 (Graded))

Question # 7 of 10 (Start time: 10:15:24 AM, 26 June 2024)

A half adder can be built by using the combination of _____ and _____ gates.

Select the correct option

○	AND, NOT
○	OR, XOR
◉	AND, XOR
○	AND, OR

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 03)

Question # 5 of 5 (Start time: 06:06:02 AM, 10 May 2024)

According to the distributive law of Boolean algebra, which of the following statements is **TRUE**?

Select the correct option

○	$X + (Y\,Z) = X+Y+Z$
◉	$X + (Y\,Z) = (X + Y)\,(X + Z)$
○	$X + (Y\,Z) = XYZ$
○	$X + (Y\,Z) = XY+XZ$

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 03)

Question # 1 of 5 (Start time: 06:01:57 AM, 10 May 2024)

According to De-Morgan's Law, the expression **(A+BC)'** is equivalent to _____.

Select the correct option

- A'B'+BC
- A'B'+A'C'
- A'B+AC'
- A' + B' + C'

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 03)

Question # 2 of 5 (Start time: 06:03:17 AM, 10 May 2024)

A commutative law of boolean algebra involves _____ boolean variable(s).

Select the correct option

○	4
○	1
○	3
◉	2

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 04)

Question # 5 of 5 (Start time: 09:26:08 AM, 17 May 2024)

A Karnaugh map (K-map) is an abstract form of _____ diagram organized as a matrix of squares.

Select the correct option

○	Triangular Diagram
○	Cycle Diagram
○	Block diagram
◉	Venn Diagram

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 04)

Question # 4 of 5 (Start time: 09:24:54 AM, 17 May 2024)

Which of the following is not a valid number for grouping of terms in K-Map?

Select the correct option

- ○ 1
- ◉ 3
- ○ 4
- ○ 2

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 04)

Question # 3 of 5 (Start time: 09:24:05 AM, 17 May 2024)

A K-Map of size 2x2 can be used to map a _____ input boolean expression.

Select the correct option

◉	2
○	1
○	3
○	4

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 04)

Question # 2 of 5 (Start time: 09:23:26 AM, 17 May 2024)

_____ is known as a universal gate.

Select the correct option

○	OR
○	XNOR
◉	NAND
○	AND

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 04)

Question # 1 of 5 (Start time: 09:22:44 AM, 17 May 2024)

_____ gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families.

Select the correct option

○	Inverse
○	Boolean
◉	Universal
○	Logic

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 06)

Question # 5 of 5 (Start time: 03:41:35 PM, 14 June 2024)

When implementing a half adder by using gates, which of the following gates is used to return carry bit as an output?

Select the correct option

○	OR
○	NAND
◉	AND
○	XOR

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 06)

Question # 4 of 5 (Start time: 03:40:45 PM, 14 June 2024)

Which of the following symbols is used to represent XOR operation?

Select the correct option

- ^
- ⊕
- +
- x

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 06)

Question # 3 of 5 (Start time: 03:39:13 PM, 14 June 2024)

Which of the following gates is used for parity generation for a binary data string?

Select the correct option

○	NOR
○	AND
○	OR
◉	XOR

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 06)

Question # 2 of 5 (Start time: 03:38:08 PM, 14 June 2024)

In a full adder circuit having inputs **A = 1, B =1, Cin = 0**, the outputs **S** and **Cout** will be _____.

Select the correct option

○	S = 1, Cout = 0
○	S = 1, Cout = 1
◉	S = 0, Cout = 1
○	S = 0, Cout = 0

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 06)

Question # 1 of 5 (Start time: 03:37:18 PM, 14 June 2024)

How many select lines would be required for an 8x1 multiplexer?

Select the correct option

○	2
○	1
○	8
◉	3

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 05)

Question # 5 of 5 (Start time: 09:39:24 AM, 24 May 2024)

It should be kept in mind that don't care terms should be used along with the terms that are present in _____.

Select the correct option

○	K-Map
○	Latches
◉	Minterms
○	Expressions

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 05)

Question # 4 of 5 (Start time: 09:38:34 AM, 24 May 2024)

To build a full adder using gates, how many gates are required?

Select the correct option

- ○ 2 AND gates, 3 OR gates, 1 XOR gates
- ○ 2 AND gates, 2 OR gates, 2 XOR gates
- ◉ 2 AND gates, 2 XOR gates, 1 OR gate
- ○ 1 AND gate, 2 OR gates, 1 XOR gate

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 05)

Question # 3 of 5 (Start time: 09:38:14 AM, 24 May 2024)

Each product term of a group, w'xy' and wy, represents the _____ in that group.

Select the correct option

○	Input
○	Sum of Maxterms
○	POS
◉	Sum of Minterms

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 05)

Question # 2 of 5 (Start time: 09:37:46 AM, 24 May 2024)

Which of the following gates is used for parity generation for a binary data string?

Select the correct option

- (●) XOR
- ( ) AND
- ( ) NOR
- ( ) OR

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 05)

Question # 1 of 5 (Start time: 09:37:11 AM, 24 May 2024)

A Karnaugh map (K-map) is an abstract form of _____ diagram organized as a matrix of squares.

Select the correct option

○	Cycle Diagram
◉	Venn Diagram
○	Block diagram
○	Triangular Diagram

CS302P - Digital Logic Design (Practical) (Semester Quiz # 01 (Graded))

Question # 1 of 10 (Start time: 10:03:12 AM, 07 May 2024)

We can change the number of inputs for a gate by using _____.

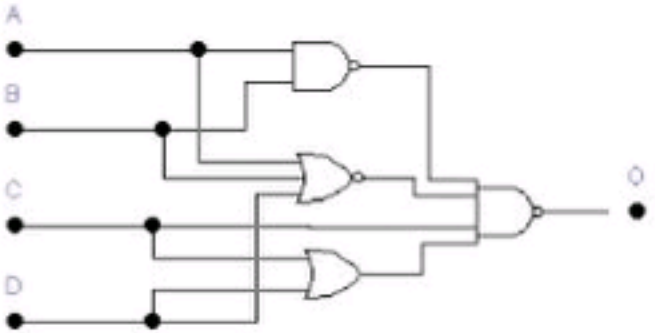
Select the correct option

- ○ Gate Structure
- ○ Truth Table
- ○ Gate Diagram
- ◉ Gate Properties

CS302P - Digital Logic Design (Practical) (Semester Quiz # 01 (Graded))

Question # 10 of 10 (Start time: 10:12:16 AM, 07 May 2024)

What will be the simplified Boolean Expression of the stated Gate Level Diagram.



Select the correct option

- ○ A + B + C' + D
- ○ A + B' + C' + D
- ◉ A' + B' + C' + D

CS302P - Digital Logic Design (Practical) (Semester Quiz # 01 (Graded))

Question # 4 of 10 (Start time: 10:05:35 AM, 07 May 2024)

Which version of Electronics Workbench is being used in this course for creating and simulating digital circuits?

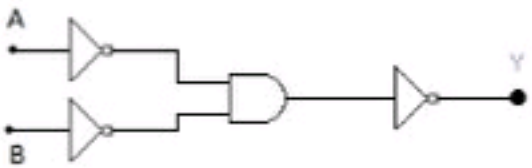
Select the correct option

- ○ version 6
- ○ version 10
- ○ version 12.5
- ○ version 5.12 ✓

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 01)

Question # 1 of 5 (Start time: 08:13:57 PM, 26 April 2024)

What will be the Boolean Equation for (Y) for the given Gate Level Diagram.



Select the correct option

○	$A'B'$
○	$A'B$
○	$A + B$
◉	$A' + B$

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 01)

Question # 2 of 5 (Start time: 08:15:05 PM, 26 April 2024)

In Electronics Workbench, the default value for the frequency of the clock source is _____.

Select the correct option

○	2 Hz
○	5 Hz
○	2 KHz
◉	50 Hz

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 01)

Question # 3 of 5 (Start time: 08:15:58 PM, 26 April 2024)

_____ is used to generate a square wave/pulse.

Select the correct option

○	Time Interval
◉	NAND Gate
○	Clock
○	Frequency

Quiz

https://vulms.vu.edu.pk/Quiz/QuizQuestion.aspx?ver=975047c7-a051-49f6-83b5-7d0d4b395c23

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 - (Graded)) **Quiz Start Time: 09:56 AM, 29 August 2022**

Question # 10 of 10 (Start time: 10:11:22 AM, 29 August 2022) **Total Marks:** 1

How many select lines would be required for an 8x1 multiplexer?

Select the correct option

Reload Math Equations

- 3
- 2
- 1
- 8

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 04)

Question # 1 of 5 (Start time: 09:22:44 AM, 17 May 2024)

_____ gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families.

Select the correct option

- ○ Inverse
- ○ Boolean
- ○ Universal
- ○ Logic

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 04)

Question # 2 of 5 (Start time: 09:23:26 AM, 17 May 2024)

_____ is known as a universal gate.

Select the correct option

○	OR
○	XNOR
◉	NAND
○	AND

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 04)

Question # 4 of 5 (Start time: 09:24:54 AM, 17 May 2024)

Which of the following is not a valid number for grouping of terms in K-Map?

Select the correct option

○	1
○	3
○	4
○	2

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 04)

Question # 5 of 5 (Start time: 09:26:08 AM, 17 May 2024)

A Karnaugh map (K-map) is an abstract form of _____ diagram organized as a matrix of squares.

Select the correct option

- ○ Triangular Diagram
- ○ Cycle Diagram
- ○ Block diagram
- ○ Venn Diagram

Question # 2 of 10 (Start time: 07:28:06 AM, 05 June 2023)

_____ is also known as a Universal gate.

Select the correct option

- OR
- XNOR
- NOR
- AND

CS302P - Digital Logic Design (Practical) (Semester Quiz # 02 – (Graded))

Question # 3 of 10 (Start time: 07:28:41 AM, 05 June 2023)

There are _____ cells in a 5-variable K-map.

Select the correct option

- 24
- 32
- 16
- 64

Question # 4 of 10 (Start time: 07:29:17 AM, 05 June 2023)

The K-map based Boolean reduction is based on the following Unifying Theorem: A + A' = 1.

Select the correct option

- Impact
- Force
- Complementarity
- Non Impact

Question # 5 of 10 (Start time: 07:31:14 AM, 05 June 2023)

_____ is known as a universal gate.

Select the correct option

- NAND
- XNOR
- OR
- AND

Question # 6 of 10 (Start time: 07:31:44 AM, 05 June 2023)

It should be kept in mind that don't care terms should be used along with the terms that are present in _____.

Select the correct option

- (●) Minterms
- ( ) K-Map
- ( ) Latches
- ( ) Expressions

Question # 7 of 10 (Start time: 07:32:45 AM, 05 June 2023)

Consider a 3-variable Karnuagh Map. How many groups of 1's can be made from the below given Karnaugh Map?

A/BC	00	01	11	10
0	0	1	1	0
1	1	1	1	1

6 & Cell = $(2)^3 = 8$

Select the correct option

1

Question # 8 of 10 (Start time: 07:33:52 AM, 05 June 2023)

Don't care conditions can be used for simplifying Boolean expressions in _____.

Select the correct option

- Registers
- K-maps
- Terms
- Latches

Question # 9 of 10 (Start time: 07:34:59 AM, 05 June 2023)

There are _____ cells in a 4-variable K-map.

Select the correct option

- ○ 20
- ○ 8
- ○ 16
- ○ 24

$(2)^4$

CS302P - Digital Logic Design (Practical) (Semester Quiz # 02 – (Graded)) Quiz Star

Question # 10 of 10 (Start time: 07:35:31 AM, 05 June 2023)

_____ gate with a bubble at the output is know as NAND gate.

Select the correct option

- NOR
- OR
- NOT
- AND

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 02)

Question # 5 of 5 (Start time: 03:51:53 PM, 03 May 2024)

A commutative law of boolean algebra involves _____ boolean variable(s).

Select the correct option

○	3
○	2
○	1
○	4

uestion # 9 of 10 (Start time: 11:50:29 PM, 08 May 2024)

Cin is part of _____ Adder.

Select the correct option

- Full
- Single
- Half
- Double

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 03)

Question # 1 of 5 (Start time: 06:01:57 AM, 10 May 2024)

According to De-Morgan's Law, the expression **(A+BC)'** is equivalent to _____.

Select the correct option

○	A'B'+BC
○	A'B'+A'C'
●	A'B+AC'
○	A' + B' + C'

Figure 14.5 Block diagrams of Half-Adder and Full-Adder

Half-Adder Function Table

The Half-Adder has a 2-bit input and a 2-bit output. The function table of the Half-Adder has two input columns representing the two single bit numbers A and B. The function table also has two output columns representing the Sum bit and Carry Out bit. Table 14.3

Input		Output	
A	B	Sum	Carry Out
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 14.3 Half-Adder Function Table

sec(s)

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 - (Graded))

Quiz Start Time: 02:54 PM, 30 January 2023

Question # 2 of 15 (Start time: 02:56:23 PM, 30 January 2023)

Total Marks: 1

Total number of inputs in a half adder is _____

Select the correct option

Reload Math Equations

- 3
- 2
- 1
- 4

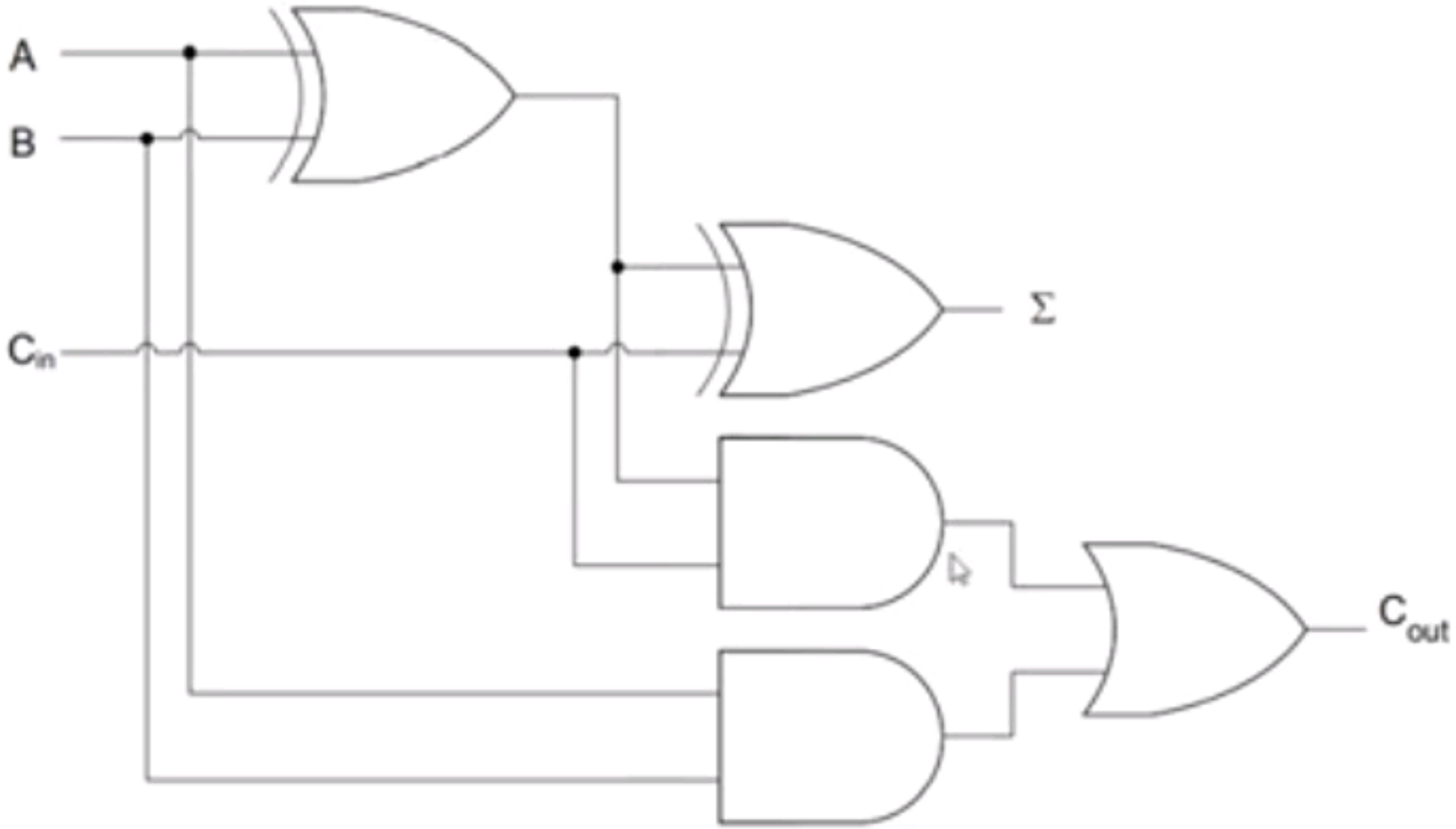


Figure 14.7 Full-Adder Logic Circuit

sec(s)

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 – (Graded))

Quiz Start Time: 02:54 PM, 30 January 2023

Question # 3 of 15 (Start time: 02:57:02 PM, 30 January 2023)

Total Marks: 1

To build a full adder using gates, how many gates are required?

Select the correct option

Reload Math Equations

- 1 AND gate, 2 OR gates, 1 XOR gate
- 2 AND gates, 3 OR gates, 1 XOR gates
- 2 AND gates, 2 OR gates, 2 XOR gates
- 2 AND gates, 2 XOR gates, 1 OR gate

Click to Save Answer & Move to Next Question

sec(s)

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 – (Graded))

Quiz Start Time: 02:54 PM, 30 January 2023

Question # 4 of 15 (Start time: 02:57:58 PM, 30 January 2023)

Total Marks: 1

Which of the following symbols is used to represent XOR operation?

Select the correct option

Reload Math Equations

- *
- ⊕
- ^
- x

10 states

اردو میں | In English

Explanation: Decimal counter is also known as 10 stage counter. So, it has **10 states**. It is also known as Decade Counter counting from 0 to 9.

https://www.sanfoundry.com › digital-circuits-questions-a...

Digital Circuits Questions and Answers – Counters - Sanfoundry

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CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 - (Graded))

Quiz Start Time: 02:54 PM, 30 January 2023

Question # 6 of 15 (Start time: 03:00:16 PM, 30 January 2023)

Total Marks: 1

A decimal counter has _____ states.

Select the correct option

Reload Math Equations

- 7
- 9
- 10
- 2

Click to Save Answer & Move to Next Question

rotate right operations. When data is rotated through a register counter a specific sequence of states is repeated. Two commonly used register counters in digital logic are the Johnson Counter and the Ring Counter.

1. Johnson Counter

In a Johnson counter, the $\overline{Q}$ output of the last flip-flop of the shift register is connected to the data input of the first flip-flop. The circuit of a 4-bit, D flip-flop based Johnson Counter is shown in figure 34.16. The sequence of states that are implemented by a n-bit Johnson counter are 2n. Thus a 4-bit Johnson counter sequences through 8 states and a 5-bit Johnson counter sequences through 10 states. Table 34.1

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 – (Graded))

Quiz Start Time: 02:54 PM, 30 January 2023

Question # 7 of 15 (Start time: 03:01:23 PM, 30 January 2023)

Total Marks: 1

To create a Johnson Counter by using D-flip flops, how flip flops should be connected together?

Select the correct option

Reload Math Equations

- Q output of previous flip flop should be connected to D input of second flip flop
- Q output of previous flip flop should be connected to clock input of second flip flop
- Q' output of previous flip flop should be connected to clock input of second flip flop
- Q' output of previous flip flop should be connected to D input of second flip flop

Click to Save Answer & Move to Next Question

اردو میں In English

Explanation: The maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops is **0 to 2^n-1**. For say, there is a 2-bit counter, then it will count till 2^2-1 = 3. Thus, it will count from 0 to 3.

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CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 – (Graded))

Quiz Start Time: 02:54 PM, 30 January 2023

Question # 9 of 15 (Start time: 03:02:57 PM, 30 January 2023)

Total Marks: 1

What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?

Select the correct option

Reload Math Equations

- 0 to 2^{n+1}
- 0 to $2^n - 1$
- 0 to 2^n
- 0 to $2^n + 1$

Click to Save Answer & Move to Next Question

sec(s)

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 – (Graded))

Quiz Start Time: 02:54 PM, 30 January 2023

Question # 8 of 15 (Start time: 03:01:50 PM, 30 January 2023)

Total Marks: 1

Which of the following gates is used for parity generation for a binary data string?

Select the correct option

Reload Math Equations

- OR
- XOR
- AND
- NOR

Click to Save Answer & Move to Next Question

the clock count

اردو میں In English

Explanation: The parallel outputs of a counter circuit represent **the clock count**. A counter counts number of times an event takes place in accordance to the clock pulse.

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CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 – (Graded))

Quiz Start Time: 02:54 PM, 30 January 2023

Question # 10 of 15 (Start time: 03:07:26 PM, 30 January 2023)

Total Marks: 1

The parallel outputs of a counter circuit represent the _____

Select the correct option

Reload Math Equations

- Parallel data word
- Counter modulus
- Clock frequency
- Clock count

How many flip-flops are required to design a mod 7 counter?

3 flip flops are required to design a mod-7 counter.

https://www.quora.com › How-many-flip-flops-will-be-re...

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sec(s)

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 – (Graded))

Quiz Start Time: 02:54 PM, 30 January 2023

Question # 11 of 15 (Start time: 03:09:09 PM, 30 January 2023)

Total Marks: 1

How many flop flops are required to create a counter circuit which can count from 0 to 7?

Select the correct option

Reload Math Equations

- 4
- 3
- 1
- 2

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

sec(s)

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 – (Graded))

Quiz Start Time: 02:54 PM, 30 January 2023

Question # 12 of 15 (Start time: 03:13:42 PM, 30 January 2023)

Total Marks: 1

In a full adder circuit having inputs **A = 1, B =1, Cin = 0**, the outputs **S** and **Cout** will be _____.

Select the correct option

Reload Math Equations

- S = 0, Cout = 1
- S = 1, Cout = 0
- S = 0, Cout = 0
- S = 1, Cout = 1

Click to Save Answer & Move to Next Question

About 1,010,000 results (0.55 seconds)

اردو میں | In English

The half adder can be built from an **XOR gate and an AND gate**. In a multi-bit adder, C_{ou} is added or carried in to the next most significant bit.

https://www.sciencedirect.com › topics › computer-science

Half Adder - an overview | ScienceDirect Topics

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Time Left sec(s)

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 – (Graded))

Quiz Start Time: 02:54 PM, 30 January 2023

Question # 13 of 15 (Start time: 03:15:42 PM, 30 January 2023)

Total Marks: 1

A half adder can be built by using the combination of _____ and _____ gates.

Select the correct option

Reload Math Equations

- AND, XOR
- OR, XOR
- AND, NOT
- AND, OR

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 – (Graded))

Quiz Start Time: 02:54 PM, 30 January 2023

Question # 14 of 15 (Start time: 03:17:13 PM, 30 January 2023)

Total Marks: 1

A counter circuit is usually constructed of _____

Select the correct option

Reload Math Equations

- A number of NOR gates connected in cascade form
- A number of NAND gates connected in cascade form
- A number of latches connected in cascade form
- A number of flip-flops connected in cascade

Click to Save Answer & Move to Next Question

اردو میں In English

A full adder can be viewed as a 3:2 lossy compressor: **it sums three one-bit inputs and returns the result as a single two-bit number**; that is, it maps 8 input values to 4 output values. Thus, for example, a binary input of 101 results in an output of 1 + 0 + 1 = 10 (decimal number 2).

https://encyclopedia.pub › entry

Binary Adder - Scholarly Community Encyclopedia

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sec(s)

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 – (Graded)) **Quiz Start Time: 02:54 PM, 30 January 2023**

Question # 5 of 15 (Start time: 02:58:42 PM, 30 January 2023) **Total Marks:** 1

A full adder circuit takes _____ bit(s) as input and returns _____ bit(s) as output.

Select the correct option

Reload Math Equations

- 2, 1
- 3, 2
- 2, 2
- 3, 1

A decimal counter has _____ states.

Select the correct option

- [ ] 7
- [ ] 2
- [x] 10
- [ ] 9

Question # 1 of 10 (Start time: 02:04:04 PM, 18 July 2023)

TTL 74LS85 is a _ _ _ _ _ _ _ _ _ _ _ _ _

Select the correct option

○	8-bit magnitude comparator
●	4-bit magnitude comparator
○	8-bit word comparator
○	1-bit digital comparator

2. A counter circuit is usually constructed of _____

a) A number of latches connected in cascade form

b) A number of NAND gates connected in cascade form

c) A number of flip-flops connected in cascade

d) A number of NOR gates connected in cascade form

View Answer

Answer: c

About 163,000,000 results (0.48 seconds)

اردو میں | In English

Explanation: Three decade counter has **30 states** and a BCD counter has 10 states. So would require 3 BCD counters. Thus, a three decade counter will count from 0 to 29.

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Question # 2 of 5 (Start time: 03:45:56 PM, 27 January 2023) Total Marks:

Three decade counter would have _____

Select the correct option

Reload Math Equations

- 5 BCD counters
- 4 BCD counters
- 3 BCD counters
- 2 BCD counters

Click to Save Answer & Move to Next Question

Question # 5 of 10 (Start time: 02:06:38 PM, 18 July 2023)

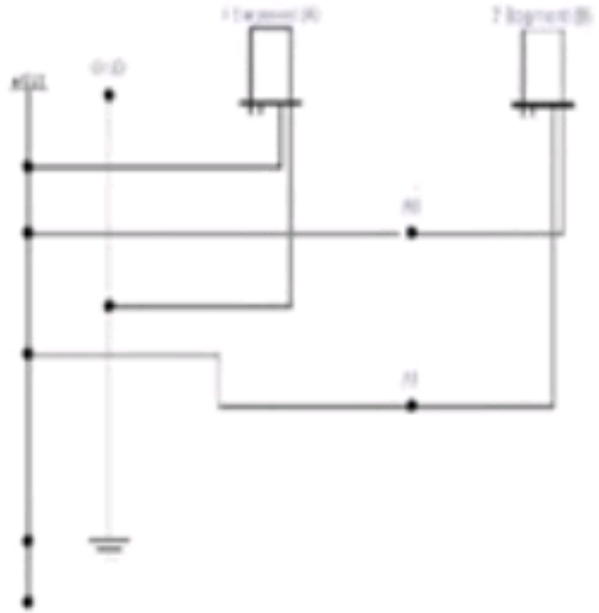
Which of the following gates is used for parity generation for a binary data string?

Select the correct option

◉	XOR
○	AND
○	NOR
○	OR

Question # 7 of 10 (Start time: 02:08:10 PM, 18 July 2023)

Consider the below given EWB circuit, what values will be displayed on 7-segment displays A and B when the circuit simulation is activated in EWB?



2, 3

Select the correct option

Question # 5 of 10 (Start time: 10:02:25 AM, 29 August 2022) **Total Marks:** 1

In order to build an XOR gate using NAND gates only, _____ gate(s) are required.

Select the correct option

Reload Math Equations

- 2
- 1
- 4
- 3

Click to Save Answer & Move to Next Question

Lesson No. 35

APPLICATIONS OF SHIFT REGISTERS

The major application of a shift register is to convert between parallel and serial data. Shift registers are also used as keyboard encoders. The two applications of the shift registers are discussed.

1. Serial-to-Parallel Converter

Earlier, Multiplexer and Demultiplexer based Parallel to Serial and Serial to Parallel converters were discussed. The Multiplexer and Demultiplexer require registers to store the parallel data that is converted into serial data and parallel data which is obtained after converting the incoming serial data. A Parallel In/Serial Out shift register offers a better solution instead of using a Multiplexer-Register combination to convert parallel data into serial data. Similarly, a Serial In/Parallel Out shift register replaces a Demultiplexer-Register combination.

In Asynchronous ... er which is constitute ... of 8-bits (which can includ ... acter from anot ... and to indicate when d ... line is idle (... ata is being transmit ... ends of t ... -bit character. A cha ... dle it is set ... gic high, when a ch ... e to logic lo ... the

imp topic

Integrated Circuit Up/Down Decade Counter

Quiz

Implementing a 4-bit Up/Down counter by connecting flip-flops and logic gate increases the circuit size and requires many connections. The 74HC190 is a 4-bit Up/Dow Synchronous Counter available in an Integrated Circuit form. Figure 29.3. The counter has th following pins. Quiz + Short

Imp

1. Parallel data inputs D_0, D_1, D_2 and D_3
2. Data outputs Q_0, Q_1, Q_2 and Q_3
3. Positive edge-triggered CLOCK signal
4. Active-low LOAD input which loads the 4-bit data applied at the counter inputs
5. Active-low CTEN counter enable input
6. $D/\overline{U}$ the count down/up input. When the input is set to logic 1, the counter counts dow and when the input is set to logic 0, the counter counts up
7. The MAX/MIN output that is set to high when the terminal count 1001 is reached whe counting up or when the terminal count 0000 is reached when counting down. Th MAX/MIN output is logic high for one complete cycle when a terminal count is reached.
8. The Ripple Clock Output RCO goes low when the Counter reaches the terminal cou 1001 or 0000 when counting up or down respectively. The RCO output remains low durin e negative half of the clock cycle. The RCO, the MAX/MIN output along with CTEN inpu used to cascade multiple counter ICs for implementing larger counters.

Quiz

Inputs D_0 D_1 D_2 D_3