IMP MCQS for Final Paper (cs302)

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A 8-bit serial in / parallel out shift register contains the value “8”, _____ clock signal(s) will be required to shift the value completely out of the register. ► 8 (Page 356)

In a sequential circuit the next state is determined by _____ and _____ ► Current state and external input (Page 318)

The divide-by-60 counter in digital clock is implemented by using two cascading counters: ► Mod-6, Mod-10 (Page 299)

The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop. ► Hold time (Page 242)

74HC163 has two enable input pins which are _____ and _____► ENP, ENT (Page 285)

_____ is said to occur when multiple internal variables change due to change in one input variable. ► Race condition (Page 267)

The _____ input overrides the _____ input. ► Asynchronous, synchronous (Page 369)

A decade counter is _____.► Mod-10 counter (Page 274)

In asynchronous transmission when the transmission line is idle, _____► It is set to logic high (Page 356)

A Nibble consists of _____ bits. ► 4 (Page 394)

The voltage gain of the Inverting Amplifier is given by the relation _____.► Vout / Vin = - Rf / Ri (Page 446)

LUT is acronym for _____► Look Up Table (Page 439)

The total amount of memory that is supported by any digital system depends upon _____.► The size of the address bus of the microprocessor (Page 430)

Stack is an acronym for _____► LIFO memory (Page 429)

Addition of two octal numbers “36” and “71” results in _____► 127

_____ is one of the examples of synchronous inputs. ► J-K input (Page 235)

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay. ► Clock Skew (Page 226)

In a state diagram, the transition from a current state to the next state is determined by► Current state and the inputs (Page 332)

_____ is used to simplify the circuit that determines the next state. ► State assignment (Page 335)

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.) ► 0000

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____► Doesn’t have an invalid state (Page 232)

A multiplexer with a register circuit converts _____► Parallel data to serial (Page 356) rep

in _____, all the columns in the same row are either read or written. ► FAST Mode Page Access (Page 413)

In order to synchronize two devices that consume and produce data at different rates, we can use _____ ► Fist In First Out Memory (Page 425)

A positive edge-triggered flip-flop changes its state when _____► Low-to-high transition of clock (Page 228)

A frequency counters _____► Counts no. of clock pulses in 1 second (Page 301)

In a sequential circuit the next state is determined by _____ and _____► Input and clock signal applied (Page 305)

The divide-by-60 counter in digital clock is implemented by using two cascading counters: ► Mod-6, Mod-10 (Page 229) rep

In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained. ► True (Page 221) rep

Flip flops are also called _____► Bi-stable multivibrators (Page 228)

A decade counter is _____.► Mod-10 counter (Page 274)

In asynchronous transmission when the transmission line is idle, _____► It is set to logic high (Page 356) rep

A Nibble consists of _____ bits. ► 4 (Page 394)

DRAM stands for _____► Dynamic RAM (Page 407)

The total amount of memory that is supported by any digital system depends upon _____► The size of the address bus of the microprocessor (Page 430)

_____ is one of the examples of asynchronous inputs. ► Clear Input (CLR)

_____ is used to minimize the possible no. of states of a circuit. ► State assignment (Page 341)

_____ is used to simplify the circuit that determines the next state ► State assignment (Page 335)

The best state assignment tends to _____.► Maximizes the number of state variables that don't change in a group of related states (Page 337)

5-bit Johnson counter sequences through ____ states. ► 10 (Page 354)

The address from which the data is read, is provided by _____. ► Microprocessor (Page 397)

_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output. ► Accuracy (Page 460)

The sequence of states that are implemented by a n-bit Johnson counter is ► 2n (n multiplied by 2)

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is ► 25 mW (Page 242)

_____ counters as the name indicates are not triggered simultaneously. ► Asynchronous (Page 269)

A synchronous decade counter will have _____ flip-flops. ► 4 (Page 281)

The alternate solution for a demultiplexer-register combination circuit is _____.► Serial in / Parallel out shift register (Page 356

The storage cell in SRAM is ► a capacitor (Page 407)

What is the difference between a D latch and a D flip-flop? ►The D flip-flop has a clock input.

For a positive edge-triggered J-K flip-flop with both J and K HIGH, the outputs will_____ if the clock goes HIGH. ► toggle

If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be ► set (Page 219)

A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value. ►True

Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer. ►A parallel to serial converter circuit (Page 244)

WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO ►Q=1 AND Q'=0 (Page 233)

If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop. ►1 (Page 230)

If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop. ► Invalid (Page 233)

We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by ►J-K flip-flop (Page 252)

A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status. ►8 (Page 272)

In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register. ►Ring counter (Page 355)

The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines. ►Access Time (Page 417)

Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state. ►Two (Page 262)

THE GLITCHES DUE TO RACE CONDITION CAN BE AVOIDED BY USING A _____►NEGATIVE-EDGE TRIGGERED FLIP-FLOPS (Page 267)

The design and implementation of synchronous counters start from _____► state diagram (Page 319)

THE HOURS COUNTER IS IMPLEMENTED USING _____►A SINGLE DECADE COUNTER AND A FLIP-FLOP

The high density FLASH memory cell is implemented using _____►1 floating-gate MOS transistor

Demultiplexer converts _____ data to _____ data. ► Serial data, parallel data (Page 356)

If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop. ► 1 (Page 230)

If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop ► Invalid (Page 230)

In asynchronous digital systems all the circuits change their state with respect to a common clock. ► False (Page 245)

A positive edge-triggered flip-flop changes its state when _____positive edge-triggered flip-flop changes its state when _____ ► Low-to-high transition of clock (Page 228)

A negative edge-triggered flip-flop changes its state when _____High-to-low transition of clock (Page 228)

A divide-by-50 counter divides the input _____ signal to a 1 Hz signal. ► 50 Hz

A synchronous decade counter will have _____ flip-flops. ► 4 (Page 281)

In _____ the Q^{---} output of the last flip-flop of the shift register is connected to the data input of the first flipflop. ► Johnson counter (Page 354)

In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register. ► Ring counter (Page 355)

Which is not characteristic of a shift register? ► Serial in/parallel in (Page 346)

In _____ outputs depend only on the combination of current state and inputs. ► Mealy machine (Page 332)

If the FIFO Memory output is already filled with data then _____► None of given options

The process of converting the analogue signal into a digital representation (code) is known as _____► Quantization (Page 445)

If the S and R inputs of the gated S-R latch are connected together using a _____gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch). ► NOT

The low to high or high to low transition of the clock is considered to be a(n) _____► Edge (Page 228)

RCO Stands for _____► Ripple Clock Output

A transparent mode means _____► The changes in the data at the inputs of the latch are seen at the output (Page 245)

In _____ outputs depend only on the current state. ► Moore Machine

Smallest unit of binary data is a _____► Bit (Page 394)

At J=1 and K=1, output of JK Flip-flop will be _____.►Toggle

Which of the following is NOT a sequential circuit? Counter

Each stage of Master-slave flip-flop works at of the clock signal One half

A Flash A/D converter uses____►Counters

When one 1 is taken as a group on a karnaugh map, the number of varaiables eliminted from the output exression is/are_____

The Sequential circuit whose output depends on the current state and the input is known as Mealy Machine.

Sequential circuits whose output is determined by the current state only is known as Moore Machine.

_____Flip-flops are obsolete now. Master-Slave

The counter states can be determined by the formula _____ (“n” represent the total number of flip-flop). ►2n (2 raise to power n)

If the FIFO Memory output is already filled with data then _____None of given options

Stack is a_____ ►LIFO Memory

According to the sampling theorem, the sampling frequency should be; Greater than twice the highest signal frequency

GAL is an acronym for _____.►Generic Array Logic

Which of the following statement is true? Power consumption of TTl is higher than CMOS

The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the_____ Set-up time (page 234)

State Machine is a generic name given to Sequential circuits_____ Sequential circuits (page 311

A bidirectional 4-bit shift register is storing nibble 1110. Is Right/LEFT input is Low. The nibble 0111 is waiting be entered on the serial data-input line. After two clock pulses, the shift register is storing_____1001

In a binary-weight D/A converter, the resistors on the inputs; Determine the weights of the digital inputs

A feature that distinguishes JK flip-flop SR flip-flop is _____ Toggle condition