CS302 By Sparrow

Final Term

Fall 2021-2022

1. **The Static Ram (SRAM) is non-volatile and is not a _____ density memory as a latch is required to store a single bit of information.**
   A. Low
   B. High
   C. Medium
   D. Hot

2. **A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.**
   A. 1
   B. 2
   C. 4
   D. 8

3. **74HC163 has two enable input pins which are _____ and _____**
   A. ENP, ENT
   B. ENI, ENC
   C. ENP, ENC
   D. ENT, ENI

4. **A decade counter is _____.**
   A. Mod-3 counter
   B. Mod-5 counter
   C. Mod-8 counter

D. Mod-10 counter

5. **The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.**
   A. Set-up time
   B. Hold time
   C. Pulse Interval time
   D. Pulse Stability time (PST)

6. **In a sequential circuit the next state is determined by _____ and _____**
   A. State variable, current state
   B. Current state, flip-flop output
   C. Current state and external input
   D. Input and clock signal applied

7. **_____ is used to minimize the possible no. of states of a circuit.**
   A. State assignment
   B. State reduction
   C. Next state table

8. **FIFO is an acronym for _____**
   A. First In, First Out
   B. Fly in, Fly Out

9. **"A + B = B + A" is _____**
   A. Demorgan's Law
   B. Distributive Law
   C. Commutative Law

10. **The sequence of states that are implemented by a n-bit Johnson counter is**
    A. n+2 (n plus 2)
    B. 2n (n multiplied by 2)

11. **_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected**
    A. Output.
    B. Resolution
    C. Accuracy

12. The address from which the data is read, is provided by _____

A. Depends on circuitry
B. None of given options
C. RAM
D. Microprocessor

13. The best state assignment tends to _____.

A. Maximizes the number of state variables that don't change in a group of related states
B. Minimizes the number of state variables that don't change in a group of related states

14. Above is the circuit diagram of _____.

A. Asynchronous up-counter
B. Asynchronous down-counter
C. Synchronous up-counter

15. 5-bit Johnson counter sequences through ____ states

A. 7
B. 10
C. 32

16. The divide-by-60 counter in digital clock is implemented by using two cascading counters:

A. Mod-6, Mod-10
B. Mod-50, Mod-10
C. Mod-10, Mod-50

17. _____ is said to occur when multiple internal variables change due to change in one input variable

A. Clock Skew
B. Race condition
C. Hold delay
D. Hold and Wait

18. A Nibble consists of _____ bits

A. 2
B. 4

19. Addition of two octal numbers "36" and "71" results in _____

A. 213
B. 123
C. 127

20. _____occurs when the same clock signal arrives at different times at different clock inputs due to

A. Propagation delay.
B. Race condition
C. Clock Skew

21. The voltage gain of the Inverting Amplifier is given by the relation _____

A. Vout / Vin = - Rf / Ri
B. Vout / Rf = - Vin / Ri

22. LUT is acronym for _____

A. Look Up Table
B. Local User Terminal

23. _____ is one of the examples of synchronous inputs.

A. J-K input
B. EN input

24. Stack is an acronym for _____

A. FIFO memory
B. LIFO memory

25. The three fundamental gates are _____

A. AND, NAND, XOR
B. OR, AND, NAND
C. NOT, NOR, XOR
D. NOT, OR, AND

26. In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

A. True
B. False

27. The 7HC163 is a 4-bit synchronous counter. It has ---------- data outputs pins.

A. 4

B. 3
C. 2

28. The ABEL Input file can use a _____ instead of the equation to specify the Boolean expressions.

A. Truth Table
B. State Diagram
C. Karnaugh Map
D. Logic Circuit

29. Counters as the name indicates are not triggered simultaneously.

A. Asynchronous
B. Synchronize
C. None Of Above

30. In memory write cycle, the time for which the WE signal remains active is known as the _____.

A. Write address setup
B. Write pulse width

31. Adding two octal numbers "36" and "71" result in _____.

A. 213
B. 123
C. 127

32. Select the mode of programming in which GAL16V8 can be programmed:

A. Simple Mode
B. Complex Mode
C. Registered Mode
D. All of the given

33. The Transition table is very similar to the _____ table.

A. Truth
B. State
C. Transition
D. None of the given

34. A SOP expression can be implemented by a _____ combination of gates.

A. OR-XOR

B. AND-NAND
C. AND-OR
D. XOR-NOR

35. Divide by-32 counter can be achieved by using:
A. Flip-flop and DIV 16
B. DIV 16
C. None

36. The _____ input overrides the _____ input.
A. Asynchronous, synchronous
B. Synchronous, asynchronous

37. The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the _____.
A. Set-up time

38. The low to high or high to low transition of the clock is considered to be a (n) _____.
A. Edge
B. Corner
C. Circle

39. Two signals _____ and _____ provide the timing inputs to the State Machine.
A. NSSR and EWSR
B. LTIME and STIME
C. PTIME and QTIME
D. NSGrn and NSYel

40. The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to _____ location(s) using a single address.
A. One
B. Two
C. Three
D. Four

41. The decimal "17" in BCD will be represented as _____
A. 11101
B. 11011
C. 10111

42. _____ is one of the examples of asynchronous inputs.

A. J-K input
B. S-R input
C. D input
D. Clear Input (CLR)

43. The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.

A. AND
B. OR

44. _____ is invalid number of cells in a single group formed by the adjacent cells in K-map

A. 2
B. 8
C. 12

45. Flip flops are also called _____

A. Bi-stable dualvibrators
B. Bi-stable transformer
C. Bi-stable multivibrators

46. The output of the expression F=A.B.C will be Logic _____ when A=1, B=0, C=1.

A. Undefined
B. One
C. Zero

47. The ANSI/IEEE Standard 754 defines a _____Single-Precision Floating Point format for binary

A. numbers.
B. 8-bit
C. 16-bit
D. 32-bit

48. The basic building block for a logical circuit is _____

A. A Flip-Flop
B. A Logical Gate

49. The total amount of memory that is supported by any digital system depends upon

_____.

A. The organization of memory
B. The structure of memory
C. The size of decoding unit
D. The size of the address bus of the microprocessor

50. Given the state diagram of an up/down counter, we can find _____

A. The next state of a given present state
B. The previous state of a given present state

51. DRAM stands for _____

A. Dynamic RAM
B. Data RAM

52. 8-bit parallel data can be converted into serial data by using _____ multiplexer.

A. 4-to-2
B. 8-to-1

53. A NOR based S-R latch is implemented using _____ gates instead of _____ gates.

A. XOR, NAND
B. NOR, XOR
C. NOR, NAND

54. The output of a NAND gate is _____ when all the inputs are one.

A. Zero
B. One

55. Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration tWD?

A. -CS
B. -WE
C. W

56. If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result.

A. 1001
B. 0110
C. 1111

57. A 3-variable Karnaugh map has

A. eight cells
B. three cells

58. In the keyboard encoder, how many times per second does the ring counter scan the key board?

A. 600 scans/second
B. 625 scans/second
C. 650 scans/second
D. 700 scans/second

59. In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in _____ when Distributed refresh is used.

A. 4.8 microsec
B. 5.9 microsec
C. 7.8 microsec
D. 5.5 microsec

60. Implementation of Latch is required almost _____ transistor.

A. Two
B. Four
C. Six
D. Eight

61. When the _____ Hz sampling interval is selected, the signal at the output of the j-k flip-flop has a time period of ____ seconds.

A. 1, 2

62. The FAST Model Page Access allows _____ memory read and access times when reading successive data values stored in consecutive locations on the same row.

A. Slow
B. Faster
C. Medium

63. Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.

A. Negative-OR, Negative-AND
B. Negative-AND, Positive-OR

C. Positive-OR, Negative-AND
D. Positive-OR, Positive-AND

64. The AND Gate performs a logical _____ function.

A. Addition
B. Subtraction
C. Multiplication
D. Division

65. The maximum value, represented by a single hexadecimal digit is _____.

A. "E"
B. "F"
C. "G"
D. "H"

66. A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

A. True
B. False

67. Cin is part of _____ Adder.

A. Half
B. Full
C. Single
D. Double

68. The domain of the expression AB'CD + AB' + C'D + B is

A. A and D
B. B only
C. A, B, C and D
D. None of the given

69. Memory is arranged in _____.

A. linear fashion
B. two-dimensional manner
C. three-dimensional manner
D. random fashion

70. The terminal count of a 4-bit binary counter in the UP mode is _____.

A. 1100

B. 0011

71. The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____ can be pressed at any time either on the first floor or the second floor in elevator.

A. REQ0
B. OPEN
C. REQ1
D. FLOOR1

72. Sub tractors also have output to check if 1 has been _____.

A. Primed
B. Shifted
C. Complemented
D. Borrowed

73. An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting _____.

A. Q output of all flip-flops to clock input of next flip-flops
B. Q' output of all flip-flops to clock input of next flip-flops

74. The ROM used by a computer is relatively _____ as it stores few bytes of code used to Boot the Computer system on power up.

A. Small
B. Large
C. Heavy
D. High

75. Flash memory Operation is classified into _____ different operation.

A. Two
B. Three
C. Four
D. Five

76. You have to choose suitable option when your timer will reset by considering this given code:
TRSTATE.CLK = clk;
TMRST: = (TRSTATE = = NSY2) # (TRSTATE = = EWY2);

A. NSY2 or EWY2
B. NSSR or TMRST

77. The 64-cell array organized as 8 x 8 cell array is considered

A. as an 64 byte memory
B. as a 16 byte memory
C. as an 8 byte memory

78. To implement the counter using S-R flip-flops instead of J-K flip-flops, the _____ transition table is used.

A. S-R

79. The Test Vector definition defines the test vectors for all the three counter inputs and _____ counter output/outputs.

A. One
B. Two
C. Three

80. Consider A=1, B=0, C=1. A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be _____.

A. Zero
B. One
C. Undefined
D. No output as input is invalid

81. In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.

A. True
B. False

82. _____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.

A. Combinational Input/output
B. Combinational Output
C. Combinational Input
D. Programmable polarity

83. PALs tend to execute _____ logic.

A. SPD

B. SOP
C. SAC

84. The 3-bit up counter can be implemented using _____ flip-flop(s).
A. S-R Flip-flips and D-Flip-flops

85. Design of state diagram is one of many steps used to design
A. Any counter

86. Which of the following is a volatile memory?
A. PROM
B. DRAM
C. EPROM
D. EEPROM

87. The outputs of SR latches in elevator state machine are feed back to the _____ gate array for connection to the D-flip-flops.
A. NOT
B. AND

88. A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:
A. 0001
B. 1000
C. 1110
D. 1111

89. When the transmission line is idle in an asynchronous transmission
A. It is set to logic low
B. It is set to logic high

90. The _____ inputs can be directly mapped to Karnaugh maps.
A. J-K

91. GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be

programmed to connect a _____ with a _____.

A. column, row
B. row, column
C. column, column
D. row, row

92. An Actable multi-vibrator is known as a (n) _____

A. Oscillator

93. A multiplexer with a register circuit converts

A. Serial data to parallel
B. Parallel data to serial
C. Serial data to serial
D. Parallel data to parallel

94. In DRAM read cycle R /W- signal is activated to read data which is made available on the _____ data line.

A. D(IN)
B. D(OUT)
C. D(AB)
D. D(INT)

95. As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack _____.

A. Bottom
B. Top
C. Down
D. Vertex

96. Canonical form is a unique way of representing _____.

A. SOP
B. Minterm

97. The _____ gate and _____ gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be

connected to the Adder input.

A. AND, NOR
B. AND, NOT
C. AND, OR
D. XOR, NAND

98. Assume a J-K flip-flop has 1s on the j and k inputs. The next clock pulse will cause the output to _____.

A. Toggle

99. UVERPROM is stands for

A. Ultra-Variant
B. Ultra-Vibrant
C. Ultra-Violet

100. Why Demultiplexer is called a data distributor?

A. The input will be distributed to one of the outputs
B. The input will be selected for the output
C. The output will be distributed to one of the inputs
D. Single input to Single Output

101. The n flip-flops store _____ states.

A. 1
B. 2^n

102. Implementation of the FIFO buffer in _____ is usually takes the form of a circular buffer.

A. RAM
B. ROM
C. PROM
D. Flash Memory

103. PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.

A. PLAs

B. PALs
C. PLDs

104. Which of the following Output Equations determines the output of the State Machine?

A. MIN = Q0Q1
B. MAX = Q0Q1EN

105. For a down counter that counts from (111 to 000), if current state is "101" the next state will be _____.

A. 111
B. 110
C. 010
D. None of the given

106. In Master-Slave flip-flop setup, the master flip flop operates at _____
A. Both Master-Slave operate simultaneously

107. The S-R latch has two inputs, therefore _____ different combinations of inputs can be applied to control the operation of the S-R latch.

A. two
B. four

108. The 3-bit up counter can be implemented using _____.
A. S-R flip-flops and D flip-flops

109. The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.
A. Sequential
B. Asynchronous
C. Synchronous

110. Which one flip-flop has an invalid output state?
A. T
B. JK

C. SR

111. The NOR logic gate is the same as the operation of the _____ gate with an inverter connected to the output.

A. AND
B. NAND
C. OR
D. NOT

112. If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a _____.

A. 0
B. 1

113. An alternate method of implementing Comparators which allows the Comparators to be easily cascaded

A. without the need for extra logic gates is _____
B. Using a single comparator
C. Using Iterative Circuit based Comparators

114. If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be

A. set
B. reset

115. A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.

A. 3
B. 7
C. 8

116. Sum term (Max term) is implemented using _____ gates

A. OR
B. AND
C. NOT

117. NOR Gate can be used to perform the operation of AND, OR and NOT Gate

A. True

B. False

118. Demultiplexer is also called

A. Data selector

B. Data router

C. Data distributor

119. The OR gate performs Boolean _____.

A. multiplication

B. subtraction

C. division

D. addition

120. In designing any counter the transition from a current state to the next sate is determined by

A. Current state and inputs

B. Only inputs

121. The storage cell in SRAM is

A. a flip –flop

B. a capacitor

122. The 4-bit 2"s complement representation of "+5" is _____

A. 1010

B. 1110

C. 1011

D. 0101

123. The alternate solution for a DE multiplexer-register combination circuit is _____

A. Parallel in / Serial out shift register

B. Serial in / parallel out shift register

124. A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

A. 10 mW

B. 25 mW

125. A synchronous decade counter will have _____ flip-flops

A. 3
B. 4
C. 7

126. Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer

A. A parallel to serial converter circuit
B. A counter circuit

127. In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.

A. Moore machine
B. Mealy machine
C. Johnson counter
D. Ring counter

128. In _____ Q bar output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.

A. Moore machine
B. Mealy machine
C. Johnson counter
D. Ring counter

129. The alternate solution for a multiplexer and a register circuit is _____

A. Parallel in / Serial out shift register
B. Serial in / Parallel out shift register

130. The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines

A. Write Time
B. Recycle Time
C. Refresh Time
D. Access Time

131. When the control line in tristate buffer is high the buffer operates like a _____ gate.

A. AND
B. OR

C. NOT

132. 3.3 v CMOS series is characterized by _____ and _____as compared to the 5 v CMOS series.

A. Low switching speeds, high power dissipation
B. Fast switching speeds, high power dissipation
C. Fast switching speeds, very low power dissipation

133. Demultiplexer converts _____ data to _____ data

A. Parallel data, serial data
B. Serial data, parallel data

134. The design and implementation of synchronous counters start from _____.

A. Truth table
B. k-map
C. state table
D. state diagram

135. The high density FLASH memory cell is implemented using _____

A. 1 floating-gate MOS transistor
B. 2 floating-gate MOS transistors

136. Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state

A. Ten
B. Eight
C. Three
D. Two

137. Generally, the Power dissipation of _____ devices remains constant throughout their operation.

A. TTL
B. CMOS 3.5 series

138. The output of an AND gate is one when _____

A. All of the inputs are one

B. Any of the input is one

139. The diagram above shows the general implementation of _____ form

A. Boolean

B. arbitrary

C. POS

140. In NAND based S-R latch, output of each _____ gate is connected to the input of the other _____ gate.

A. NOR, NAND

B. NAND, NOR

C. NOR, NOR

D. NAND, NAND

141. If S=1 and R=1, then Q (t+1) = _____ for negative edge triggered flip-flop.

A. 0

B. 1

C. Invalid

142. In _____ outputs depend only on the combination of current state and inputs.

A. Mealy machine

B. Moore Machine

C. State Reduction table

143. A divide-by-50 counter divides the input _____ signal to a 1 Hz signal.

A. 10 Hz

B. 50 Hz

144. The process of converting the analogue signal into a digital representation (code) is known as _____

A. Strobing

B. Amplification

C. Quantization

145. NAND gate is formed by connecting _____

A. AND Gate and then NOT Gate
B. NOT Gate and then AND Gate

146. The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called

A. Radiation-Erase programming method (REPM)
B. In-System Programming (ISP)

147. A negative edge-triggered flip-flop changes its state when _____

A. Enable input (EN) is set
B. Preset input (PRE) is set
C. Low-to-high transition of clock
D. High-to-low transition of clock

148. Consider the sum of weight method for converting decimal into binary value; _____ is the highest weight for 411.

A. 64
B. 128
C. 256
D. 512

149. The Adjacent 1s Detector accepts 4-bit inputs. If _____ adjacent 1s are detected in the input, the output is set to high.

A. 2
B. 4
C. 1
D. 0

150. The CONSTATE.CLK = Clock is used to indicate that the _____ state variables change on a clock transition.

A. CONSTATE
B. FLOOR
C. MOTION
D. OPEN

151. If the number of samples that are collected is reduced by half, the reconstructed signal will be _____ from/to the original.

A. Different
B. Same
C. Equal
D. Opposite

152. In order to synchronize two devices that consume and produce data at different rates, we can use _____

A. Read Only Memory
B. Fist In First Out Memory
C. Flash Memory
D. Fast Page Access Mode Memory

153. A frequency counter _____

A. Counts pulse width
B. Counts no. of clock pulses in 1 second
C. Counts high and low range of given clock pulse
D. None of given options

154. In a state diagram, the transition from a current state to the next state is determined by

A. Current state and the inputs
B. Current state and outputs

155. _____ is used to simplify the circuit that determines the next state.

A. State diagram
B. Next state table
C. State reduction
D. State assignment

156. In _____, all the columns in the same row are either read or written.

A. Sequential Access
B. MOS Access
C. FAST Mode Page Access

157. The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

A. Doesn't have an invalid state
B. Sets to clear when both J = 0 and K = 0

158. A GAL is essentially a _____.

A. Non-reprogrammable PAL
B. PAL that is programmed only by the manufacturer
C. Very large PAL
D. Reprogrammable PAL

159. Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using _____.

A. Shift Registers
B. Circular Buffers

160. The simplest and most commonly used Decoders are the _____ Decoders

A. n to 2n
B. (n-1) to 2n

161. The _____ Encoder is used as a keypad encoder.

A. 2-to-8 encoder
B. 4-to-16 encoder
C. BCD-to-Decimal
D. Decimal-to-BCD Priority

162. RCO Stands for _____

A. Reconfiguration Counter Output
B. Reconfiguration Clock Output
C. Ripple Counter Output
D. Ripple Clock Output

163. Smallest unit of binary data is a _____

A. Bit
B. Nibble

164. Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires _____ gates for the 8 product terms with an 8-input OR gate.

A. 8 OR
B. 8 AND
C. 8 XOR
D. 8 NOR

165. For a Standard SOP expression, a _____ is placed in the cell

corresponding to the product term (Minterm) present in the expression.

A. 0

B. 1

C. Any of given option depending on SOP term

Contact for Help.

We have checked all the Answers if you find any mistake let us know.

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Remember in Prayers.

Best of Luck.