

Cs302 Quiz no 2

To write data to the memory the memory the write cycle is initiated by

Applying the address signals

The counter states or the range of the number of a counter is determined by the formula ("n" represented the total number of flip-flops)

2 raise to power n

THE FOUR OUTPUTS OF TWO 4-INPUT MULTIPLEXERS, CONNECTED TO FORM A 16-INPUT MULTIPLEXER, ARE CONNECTED TOGETHER THROUGH A 4-INPUT _____ GATE

OR

A FIELD-PROGRAMMABLE LOGIC ARRAY CAN BE PROGRAMMED BY THE USER AND NOT BY THE MANUFACTURER.

TRUE

in sequential circuits memory elements are connected with_____.

common clock

A synchronous decade counter will have _____ flip-flops

4

the terminal count of a modulus -13 binary counter is

1101

The alternate solution for a multiplexer and a register circuit is _____

Parallel in / Serial out shift register

A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

8

Which of the following output equations determines the output of the state machine?

Max-Q0Q1EN

The CONSTATE.CLK = Clock is used to indicate that the _____ state variables change on a clock transition.

CONSTATE

Memory is arranged in _____.

two-dimensional manner

The n flip-flops store _____ states.

2^n

PALs tend to execute _____ logic.

SOP

In DRAM read cycle R /W- signal is activated to read data which is made available on the _____ data line.

D(OUT)

A SOP expression can be implemented by an _____ combination of gates.

AND-OR

Why demultiplexer is called a data distributor?

Single input to Single Output

If the number of samples that are collected is reduced by half, the reconstructed signal will be _____ from/to the original.

Same

The AND Gate performs a logical _____ function.

Division

The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the _____ can be pressed at any time either on the first floor or the second floor in elevator.

REQ1

_____ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.

Combinational Input

The 64-cell array organized as 8 x 8 cell array is considered

as an 8 byte memory

A 3-variable karnaugh map has

eight cells

_____ Counters as the name indicates are not triggered simultaneously.

Synchronous

The ABEL Input file can use a _____ instead of the equation to specify the Boolean expressions.

Truth Table

The _____ gate and _____ gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.

XOR, NAND

In the keyboard encoder, how many times per second does the ring counter scan the key board?

650 scans/second

Flash memory Operation are classified into _____ different operation.

Two

A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:

1111

The outputs of SR latches in elevator state machine are feed back to the _____ gate array for connection to the D-flipflops.

AND

The domain of the expression $AB'CD + AB' + C'D + B$ is

A, B, C and D

The Adjacent 1s Detector accepts 4-bit inputs. If _____ adjacent 1s are detected in the input, the output is set to high.

1

Which of the following Output Equations determines the output of the State Machine?

$MAX = Q0Q1EN$

When the transmission line is idle in an asynchronous transmission

It is set to logic high

In NAND based S-R latch, output of each _____ gate is connected to the input of the other _____ gate.

NAND, NAND

PLDs have In-System Programming (ISP) capability that allows the _____ to be programmed after they have been installed on a circuit board.

PLDs

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

True

The terminal count of a 4-bit binary counter in the UP mode is _____.

1100

Select the mode of programming in which GAL16V8 can be programmed:

All of the given

Consider the sum of weight method for converting decimal into binary value, _____ is the highest weight for 411.

256

If two numbers in BCD representation generate an invalid BCD number then the binary _____ is added to the result.

1001

In memory write cycle, the time for which the WE signal remains active is known as the _____.

Write pulse width

GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a _____ with a _____.

row, column

The S-R latch has two inputs, therefore _____ different combinations of inputs can be applied to control the operation of the S-R latch.

four

The Transition table is very similar to the _____ table.

State

A NOR based S-R latch is implemented using _____ gates instead of _____ gates.

NOR, NAND

Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using _____.

Shift Registers

For a down counter that counts from (111 to 000), if current state is "101" the next state will be _____.

None of the given

The NOR logic gate is the same as the operation of the _____ gate with an inverter connected to the output.

NAND

The ROM used by a computer is relatively _____ as it stores few bytes of code used to Boot the Computer system on power up.

Small

Canonical form is a unique way of representing _____.

SOP

UVERPROM is stands for

Ultra-Violet

If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a _____.

1

Cin is part of _____ Adder.

Full

Which one flip-flop has an invalid output state?

SR

Which of the following is a volatile memory?

DRAM

The maximum value, represented by a single hexadecimal digit is _____.

"F"

As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack _____.

Top

8-bit parallel data can be converted into serial data by using _____ multiplexer.

8-to-1

You have to choose suitable option when your timer will reset by considering this given code:

```
TRSTATE.CLK = clk;
```

```
TMRST: = (TRSTATE == NSY2) # (TRSTATE == EWY2);
```

NSY2 or EWY2

The FAST Model Page Access allows _____ memory read and access times when reading successive data values stored in consecutive locations on the same row.

Faster

Adding two octal numbers "36" and "71" result in _____.

127

The Static Ram (SRAM) is non-volatile and is not a _____ density memory as a latch is required to store a single bit of information.

High

In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.

True

Demorgan's two theorems prove the equivalency of the NAND and _____ gates and the NOR and _____ gates respectively.

Negative-OR, Negative-AND

A multiplexer with a register circuit converts

Parallel data to serial

Implementation of Latch is required almost _____ transistor.

Six

The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as _____ inputs.

Synchronous

The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to _____ location(s) using a single address.

Four

Consider $A=1$, $B=0$, $C=1$. A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be _____.

One

The 74HC163 is a 4-bit Synchronous counter, it has _____ data output pins.

4

The _____ input overrides the _____ input.

Asynchronous, synchronous

The Test Vector definition defines the test vectors for all the three counter inputs and _____ counter output/outputs.

Three

Subtractors also have output to check if 1 has been _____.

Primed

An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting _____.

Q output of all flip-flops to clock input of next flip-flops

Divide-by-32 counter can be achieved by using

Flip-Flop and DIV 32

For a Standard SOP expression, a _____ is placed in the cell corresponding to the product term (Minterm) present in the expression.

1

Two signals _____ and _____ provide the timing inputs to the State Machine.

PTIME and QTIME

Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration t_{WD} ?

-WE

Implementation of the FIFO buffer in _____ is usually takes the form of a circular buffer.

RAM

In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in _____ when Distributed refresh is used.

7.8 microsec

The output of a NAND gate is _____ when all the inputs are one.

Zero

Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires _____ gates for the 8 product terms (minterms) with an 8-input OR gate.

8 AND

WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO -----

THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED

The terminal count of a 4-bit binary counter in the UP mode is .

1111

For a down counter that counts from (111 to 000). If current state is “101” the next state will be

110

The n flip-flops store states.

2^n

An Asynchronous Down-counter is implemented (using J-K flip-flop) by connecting

Q output of all flip-flops to clock input of next flip-flops

In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated. Circuit counters allow cascading of multiple counters together.

True

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

False

The 74HC163 is a 4-bit Synchronous Counter, it has data output pins.

4

Divide-by-32 counter can be achieved by using

Flip-Flop and DIV 16

The synchronous counters are also known as Ripple Counters:

False

Each stage of Master-slave flip-flop works at of the clock signal

One half

With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in

80 micro seconds

Number of states in an 8-bit Johnson counter sequence are:

16

In moore machine the output depends on

The current state

Asynchronous mean that

Each flip-flop after the first one is enabled by the output of the preceding flip-flop

According to moore circuit, the output of synchronous sequential circuit depend/s on of flip flop.

Present state

In gated SR latch, what is the value of the output if $EN=1$, $S=0$ and $R=1$?

0

A Divide-by-20 counter can be achieved by using

Flip-Flop and DIV 10

A one-shot mono-stable device contains _

NOR gate, Resistor, Capacitor and NOT Gate

The inputs can be directly mapped to karnaugh maps.

J-K

A mono-stable device only has a single stable state

True

When the Hz sampling interval is selected, the signal at the output of the J-K flipflop has a time period of seconds.

1, 2

The _____ Encoder is used as a keypad encoder.

Decimal-to-BCD Priority

3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions

True

If $S=1$ and $R=0$, then $Q(t+1) = \underline{\hspace{2cm}}$ for positive edge triggered flip-flop

1

NOR gate is formed by connecting

OR Gate and then NOT Gate

A particular half adder has

2 INPUTS AND 2 OUTPUT

Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause the output to .

Toggle

A stage in the shift register consists of

A flip flop

If a circuit suffers “Clock Skew” problem, the output of circuit can’t be guaranteed.

True

A modulus-14 counter has fourteen states requiring

4 flip flops

In Master-Slave flip-flop the clock signal is connected to slave flip-flop using gate.

NOT

flip-flops are obsolete now.

Master-Slave

The glitches due to “Race Condition” can be avoided by using a .

Negative-Edge triggered flipflops

For a gated D-Latch if EN=1 and D=1 then $Q(t+1)=$

1

occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Clock skew

An Astable multivibrator is known as a (n) .

Oscillator

In Master-Slave flip-flop setup, the master flip-flop operators at

Both Master-Slave operator simultaneously

The power consumed by a flip-flop is defined by _

$$c.P = V_{cc} \times I_{cc}$$

The 3-bit up counter can be implemented using flip-flop(s).

S-R flip-flops and D-flip-flops

The terminal count of a 4-bit binary counter in the DOWN mode is

0000

If the S and R inputs of the gated S-R latch are connected together using a _____ gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)

NOT

The low to high or high to low transition of the clock is considered to be a(n)

Edge

RCO Stands for _____

Ripple Clock Output

A transparent mode means _____

The changes in the data at the inputs of the latch are seen at the output

In _____ outputs depend only on the current state.

Moore Machine

Smallest unit of binary data is a _____

Bit

Which mechanisms allocate the binary values to the states in order to reduce the cost of the combinational circuits?

State assignment

State of flip-flop can be switched by changing its

Input signal

Once the state diagram is drawn for any sequential circuit the next step is to draw

Next-state table

Design of state diagram is one of many steps used to design

A truncated counter

Flip flops are also called_____.

Bi-stable multivibrators

Three cascaded modulus-10 counters have an overall modulus of

1000

The term hold always means .

No change

A flip-flop is presently in SET state and must remain SET on the next clock pulse.

What must j and k be?

$J=X(\text{Don't care}), K=0$

To parallel load a byte of data into a shift register, there must be

One clock pulse

Invalid state of NOR based SR latch occurs when _____.

S=1, R=1

The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

Hold time

74HC163 has two enable input pins which are _____ and _____

ENP, ENT

_____ is said to occur when multiple internal variables change due to change in one input variable

Race condition

The _____ input overrides the _____ input

Asynchronous, synchronous

A decade counter is _____.

Mod-10 counter

In asynchronous transmission when the transmission line is idle, _____

It is set to logic high

A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

8

In a sequential circuit the next state is determined by _____ and _____

Current state and external input

The divide-by-60 counter in digital clock is implemented by using two cascading counters:

Mod-6, Mod-10

In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

True

A Nibble consists of _____ bits

4

Excess-8 code assigns _____ to “-8”

0000

The voltage gain of the Inverting Amplifier is given by the relation _____

$V_{out} / V_{in} = - R_f / R_i$

LUT is acronym for _____

Look Up Table

The three fundamental gates are _____

NOT, OR, AND

The total amount of memory that is supported by any digital system depends upon _____

The size of the address bus of the microprocessor

Stack is an acronym for _____

LIFO memory

Addition of two octal numbers “36” and “71” results in _____

127

_____ is one of the examples of synchronous inputs.

J-K input

_____ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Clock Skew

In a state diagram, the transition from a current state to the next state is determined by

Current state and the inputs

_____ is used to simplify the circuit that determines the next state.

State assignment

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse?
(Right-most bit first.)

0000

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

Doesn't have an invalid state

A multiplexer with a register circuit converts _____

Parallel data to serial

GAL is essentially a _____.

Reprogrammable PAL

in _____, all the columns in the same row are either read or written.

FAST Mode Page Access

In order to synchronize two devices that consume and produce data at different rates, we can use _____

First In First Out Memory

A flip-flop changes its state when _____

Low-to-high transition of clock

A frequency counter _____

Counts no. of clock pulses in 1 second

In a sequential circuit the next state is determined by _____ and _____

Input and clock signal applied

Flip flops are also called _____

Bi-stable multivibrators

Given the state diagram of an up/down counter, we can find _____

The next state of a given present state

A Nibble consists of _____ bits

4

The output of this circuit is always _____.

1

A logic circuit with an output $X = ABC + AB$ consists of _____.

two AND gates, one OR gate, two inverters

The diagram given below represents _____

Sum of product form

The voltage gain of the Inverting Amplifier is given by the relation _____

$V_{out} / V_{in} = - R_f / R_i$

DRAM stands for _____

Dynamic RAM

The three fundamental gates are _____

NOT, OR, AND

Which of the following statement is true regarding above block diagram?

Triggering can take place anytime during the HIGH level of the CLK waveform

The expression $F = A + B + C$ describes the operation of three bits _____ Gate.

OR

Addition of two octal numbers "36" and "71" results in _____

127

The ANSI/IEEE Standard 754 defines a _____ Single-Precision Floating Point format for binary numbers.

32-bit

The decimal “17” in BCD will be represented as _____

10111

The output of the expression $F=A.B.C$ will be Logic _____ when $A=1$, $B=0$, $C=1$.

Zero

_____ is invalid number of cells in a single group formed by the adjacent cells in K-map

12

The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.

AND

_____ is one of the examples of asynchronous inputs. ?

J-K input

Consider an up/down counter that counts between 0 and 15, if external input(X) is “0” the counter counts upward (0000 to 1111) and if external input (X) is “1” the counter counts downward (1111 to 0000), now suppose that the present state is “1100” and $X=1$, the next state of the counter will be _____.

1101 (not sure)

In a state diagram, the transition from a current state to the next state is determined by

Current state and the inputs

_____ is used to minimize the possible no. of states of a circuit.

State assignment

The best state assignment tends to _____.

Maximizes the number of state variables that don't change in a group of related states

5-bit Johnson counter sequences through _____ states

10

The address from which the data is read, is provided by _____

Microprocessor

FIFO is an acronym for _____

First In, First Out

The voltage gain of the Inverting Amplifier is given by the relation _____

$V_{out} / V_{in} = - R_f / R_i$

_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

Accuracy

Above is the circuit diagram of _____.

Asynchronous up-counter

The sequence of states that are implemented by a n-bit Johnson counter is

$2n$ (n multiplied by 2)

" $A + B = B + A$ " is _____

Commutative Law

Following is standard POS expression

True

An alternate method of implementing Comparators which allows the Comparators to be easily cascaded without the need for extra logic gates is _____

Using Iterative Circuit based Comparators

DE multiplexer is also called

Data distributor

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

25 mW

_____ Counters as the name indicates are not triggered simultaneously.

Asynchronous

In a state diagram, the transition from a current state to the next state is determined by

Current state and the inputs

A synchronous decade counter will have _____ flip-flops

4

The alternate solution for a demultiplexer-register combination circuit is

Serial in / Parallel out shift register

The 4-bit 2's complement representation of "+5" is _____

0101

The storage cell in SRAM is

a capacitor

What is the difference between a D latch and a D flip-flop?

The D flip-flop has a clock input.

For a positive edge-triggered J-K flip-flop with both J and K HIGH, the outputs

Will _____ if the clock goes HIGH.

toggle

The OR gate performs Boolean _____.

addition

If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input

goes to 0, the latch will be

set

The power dissipation, PD, of a logic gate is the product of the
dc supply voltage and the peak current

A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.

True

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

True

Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer

A parallel to serial converter circuit

The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms

8

In designing any counter the transition from a current state to the next state is determined by

Current state and inputs

Sum term (Max term) is implemented using _____ gates

OR

AT TO THE VALUE STORED IN A 4-BIT LEFT SHIFT WAS "1". WHAT
WILL
BE THE VALUE OF REGISTER AFTER THREE CLOCK PULSES?

8 (not sure)

If $S=1$ and $R=0$, then $Q(t+1) = \underline{\hspace{2cm}}$ for positive edge triggered flip-flop

1

If $S=1$ and $R=1$, then $Q(t+1) = \underline{\hspace{2cm}}$ for negative edge triggered flip-flop

Invalid

We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by

J-K flip-flop

In Q output of the last flip-flop of the shift register is connected to the data input of the first flipflop of the shift register.

Ring counter

The of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines

Access Time

Bi-stable devices remain in either of their states unless the inputs force the device to switch its state

Two

A counter is implemented using three (3) flip-flops, possibly it will have maximum output status.

8

A full-adder has a $C_{in} = 0$. What are the sum (<PRIVATE

"TYPE=PICT;ALT=sigma">) and the carry(C_{out}) when $A = 1$ and $B = 1$?

$= 0, C_{out} = 1$

THE GLITCHES DUE TO RACE CONDITION CAN BE AVOIDED BY USING

A _____

NEGATIVE-EDGE TRIGGERED FLIP-FLOPS

The design and implementation of synchronous counters start from _____

state diagram

THE HOURS COUNTER IS IMPLEMENTED USING _____

A SINGLE DECADE COUNTER AND A FLIP-FLOP

The high density FLASH memory cell is implemented using _____

1 floating-gate MOS transistor

$Q2 := Q1 \text{ OR } X \text{ OR } Q3$ The above ABEL expression will be

$Q2 := Q1 \# X \# Q3$

When the control line in tri-state buffer is high the buffer operates like a

_____ gate

NOT

The output of an AND gate is one when _____

All of the inputs are one

The binary numbers $A = 1100$ and $B = 1001$ are applied to the inputs of a comparator. What are the output levels?

$A > B = 1, A < B = 0, A = B = 0$

The diagram above shows the general implementation of _____ form

POS

The device shown here is most likely a

Multiplexer

DE multiplexer converts _____ data to _____ data

Serial data, parallel data

If $S=1$ and $R=0$, then $Q(t+1) =$ _____ for positive edge triggered flip-flop

1

If $S=1$ and $R=1$, then $Q(t+1) =$ _____ for negative edge triggered flip-flop

Invalid

In asynchronous digital systems all the circuits change their state with respect to a common clock

False

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

25 mW

A divide-by-50 counter divides the input _____ signal to a 1 Hz signal.

50 Hz

The design and implementation of synchronous counters start from _____

state diagram

The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called _____

In-System Programming (ISP)

Following is the circuit diagram of mono-stable device which gate will be replaced by the red colored rectangle in the circuit.

XNOR

In _____ outputs depend only on the combination of current state and inputs.

Mealy machine

In the following statement Z PIN 20 ISTYPE „reg.invert“;

Active-low Registered Mode output

A Nibble consists of _____ bits

4

A bidirectional 4-bit shift register is storing the nibble 1110. Its input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing _____.

1001

In order to synchronize two devices that consume and produce data at different rates, we can use _____

Fist In First Out Memory

If the FIFO Memory output is already filled with data then _____

None of given options

The process of converting the analogue signal into a digital representation (code) is known as _____

Quantization

$Q2 := Q1 \text{ OR } X \text{ OR } Q3$ The above ABEL expression will be

$Q2 := Q1 \# X \# Q3$

The simplest and most commonly used Decoders are the _____ Decoders

n to 2^n

In _____ the output of the last flip-flop of the shift register is connected to the data input of the first flipflop. ?

Johnson counter

Which is not characteristic of a shift register?

Serial in/parallel in

NOR Gate can be used to perform the operation of AND, OR and NOT Gate

TRUE

The output of an XNOR gate is 1 when _____ I) All the inputs are zero II) Any of the inputs is zero III) Any of the inputs is one IV) All the inputs are one

II and III only

NAND gate is formed by connecting _____

AND Gate and then NOT Gate

Consider $A=1, B=0, C=1$. A, B and C represent the input of three bit NAND gate the output of the NAND gate will be _____

One