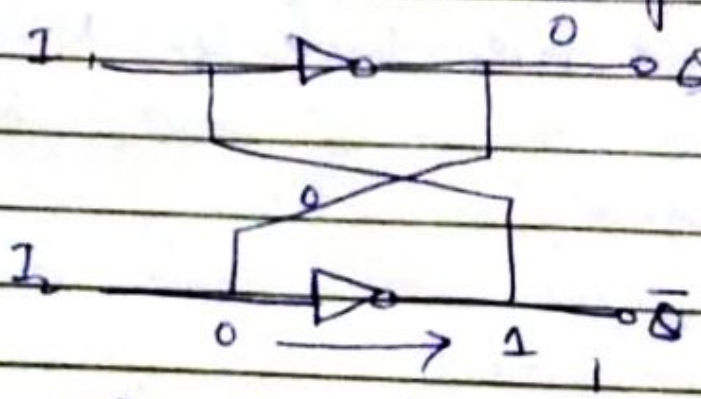
CS302.

IMPORTANT TOPIC NOTES:-

→ The latch & flip flop:-

Latches:-

- Latches are building block of sequential circuit.
- Built from logic gates
- without clock
- latches is created using NOT gate.



- The operation of latches depends on

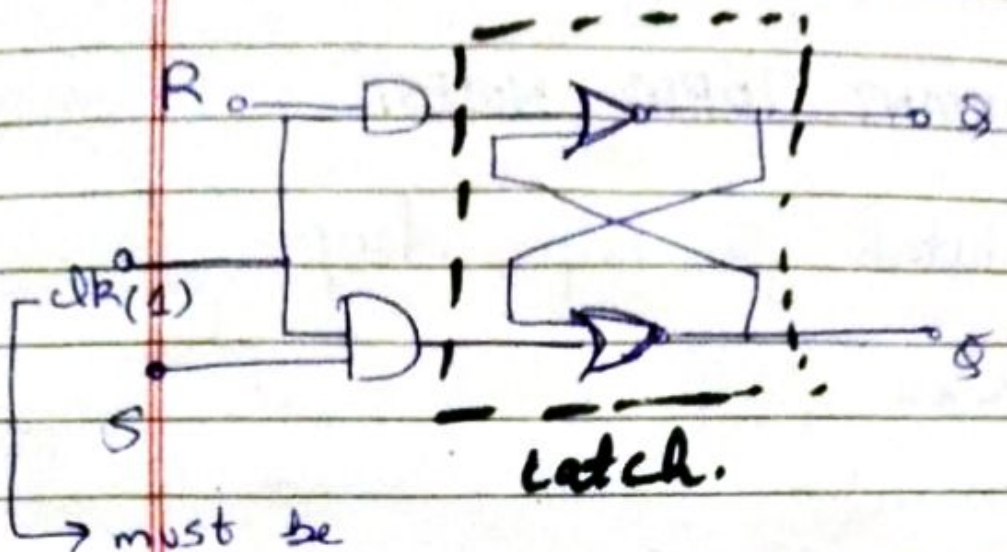
→ Sequential Circuit:-

output depends on Present and Past input.

Flip flop:-

- Also sequential circuit used to store one bit binary no (logic 1 and 0)
- Built from latches
- with clock

- (Jk, SR, D, T).



latch.

→ must be high

- The flip flop depends on clock Pulses.

★ **ABEL input file 1-of-4 MUX:-**

→ A Quad 1-of-4 MUX has four Multiplexer.

→ Each Multiplexer has four input and single output

★ **Implementation of Quad MUX:-**

★ The Quad Multiplexer has 16 inputs. 4 input for each multiplexer.

★ Each multiplexer have single input and 4 outputs

★ The **GAL20V8 PLD** is used for implementation of 1-of-4 Multiplexer.

M T W T F S

Sequential Circuits:-

The combinational digit circuit have no storage element. The output of sequential circuit depends on Present and Past inputs.

* Latches & flip flop:-

- A latch is a temporary storage device that has two stable states
- latch output can change from one state to another using appropriate inputs
- Latch have two inputs. (0, 1)
- latch have two outputs. $(Q, \bar{Q})$
- → latch is high when $Q=1$, $\bar{Q}=0$.
- → Latch is low when, $Q=0$, $\bar{Q}=1$
- → A latch is a memory element which is able to retain the information stored in it

* Gated S-R latch:-

- The gated SR latch has an element that enables input which has to be activated to operate latch.
- In gated SR latch the S and R inputs

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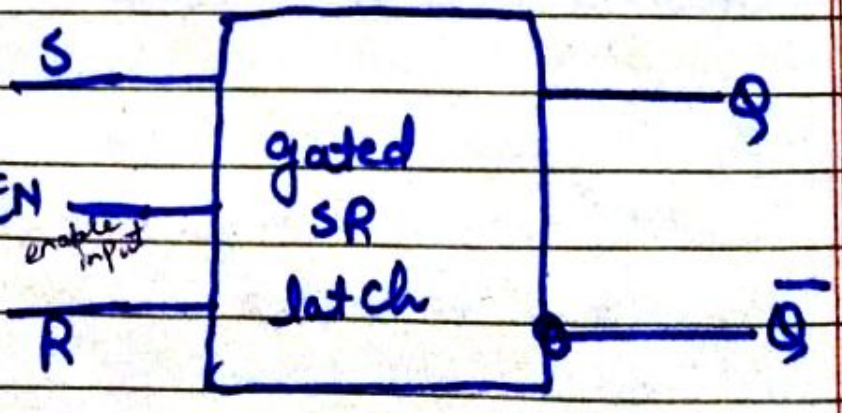
are applied at the input of the NAND gates 1 and 2. When the enable input is set to active high.
If the enable input is disabled by setting it to logic low the output of NAND gates 3 to 4 remain logic 1, whatever state of S, R inputs logic 1 applied at the inputs of NAND gates 1 and 2 keeps the Q and $\bar{Q}$ to Previous state.

Input			output
EN	S	R	Q_{t+1}
0	X	X	Q_t
1	0	0	Q_t
1	0	1	0
1	1	0	1
1	1	1	invalid.

truth Table.



Logic Symbol. S-R

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★ Gated D-latch:-

- if the S and R inputs of the gated S-R latch are connected together using NOT gate.
- Then there is only a single output to a latch.
- Input is represented by **D** instead of **S** & **R**.
- The gated D latch can either have D set to **0, 1.**
- Then four input combinations applied at **S-R inputs** of an S-R **latch** reduce to only two inputs combination.

Logic Symbol:-

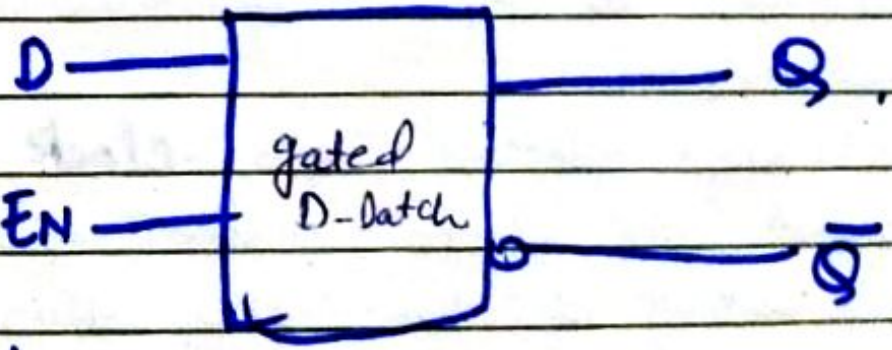

Table:-

Input			Output
EN	S(D)	R	Q_{t+1}
0	X	X	Q_t
1	0	0	Q_t
1	0	1	0
1	1	0	1
1	1	1	invalid

Input		Out
EN	D	Q_{t+1}
0	X	Q_t
1	0	0
1	1	1

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Applications:-

- The D-latch is available in form of an integrated circuit
- The **74LS75** has **four D latches** which can be used independently
- The D-gated latch is used to store binary information
- 8-bit parrallel data is converted into serial data.

---

* Edge Triggered flip-flops:-

- Flip-flops are synchronous bi-stable devices known as bi-stable multivibrators
- Flip flop have a **clock input** instead of simple enable input
- The output of the flip flop can only change when appropriate inputs are applied at **S & R** inputs and **"clock signal"** is applied at **"clock input"**.
- In Synchronous system the output of all the digital circuit changes when a clock

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signal is applied instead of enable signal.

- The change in the state of digital circuit occurs either at
  - → low-to-high.
  - → high-to-low

transition of clock signal.

★ Types of Edge Triggered :-

1- S-R edge Triggered flip flop.
2- D edge Triggered flip flop.
3- J-K edge triggered flip flop

Each flip flop have two variation.

- Positive edge Triggered.
- Negative edge Triggered.

→ **Positive edge Triggered:-**
A positive edge triggered flip-flop changes its state on a **low-to-high** transition of clock.

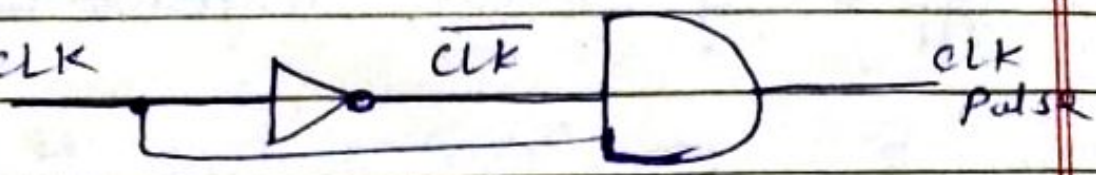
→ **Negative edge Triggered:-**
A negative edge triggered flip-flop changes its state on a **high-to-low** transition of a clock.

- The edge detection circuit

which allows a flip flop to change its state on either positive or negative transition of clock is implemented using a simple combinational circuit.

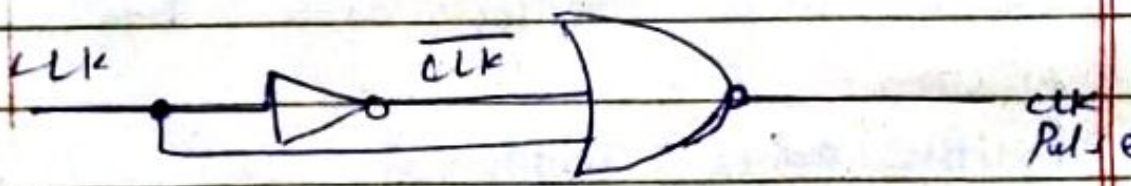
★ **POSITIVE CLOCK Edge detection:**

circuit



★ **Negative CLOCK Edge detection:**

circuit



1- Edge-Triggered S-R flip flop:-

Logic Symbols of Positive & Negative S-R triggered flip-flop:-

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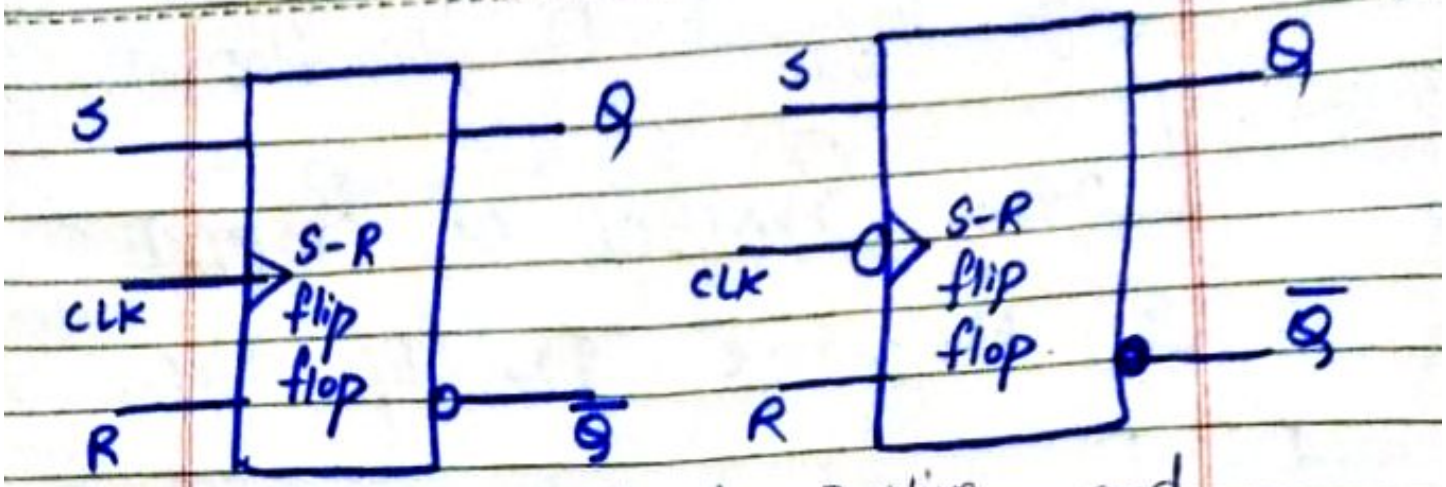

Logic Symbol of Positive and Negative edge triggered S-R flip-flops

- The difference is only that in negative edge flip flop we use negative sign.

Truth Tables of Positive & Negative S-R flip-flops:-

Input			output
CLK	S	R	Q_{t+1}
0	X	X	Q_t
1	X	X	Q_t
↑	0	0	Q_t
↑	0	1	0
↑	1	0	1
↑	1	1	invalid

Positive.

Input			output
CLK	S	R	Q_{t+1}
0	x	x	Q_t
1	x	x	Q_t
↓	0	0	Q_t
↓	0	1	0
↓	1	0	1
↓	1	1	invalid

Negative.

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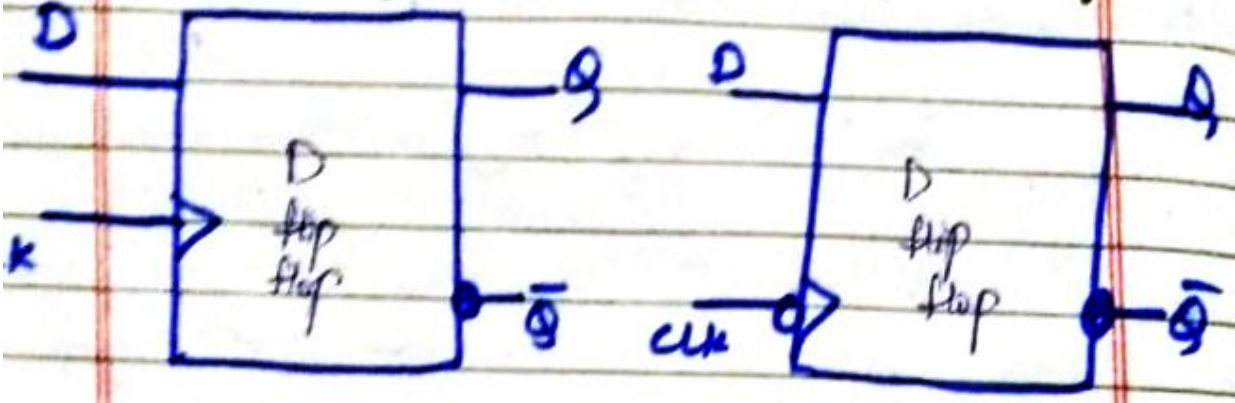
2- Edge Triggered D-flip flop:-

Logic Symbol of Positive & Negative D-flip flop:-



Positive

Negative

Truth Tables of +ve & -ve D-flip flop:-

Input		output
CLK	D	Q_{t+1}
0	X	Q_t
1	X	Q_t
↑	0	0
↑	1	1

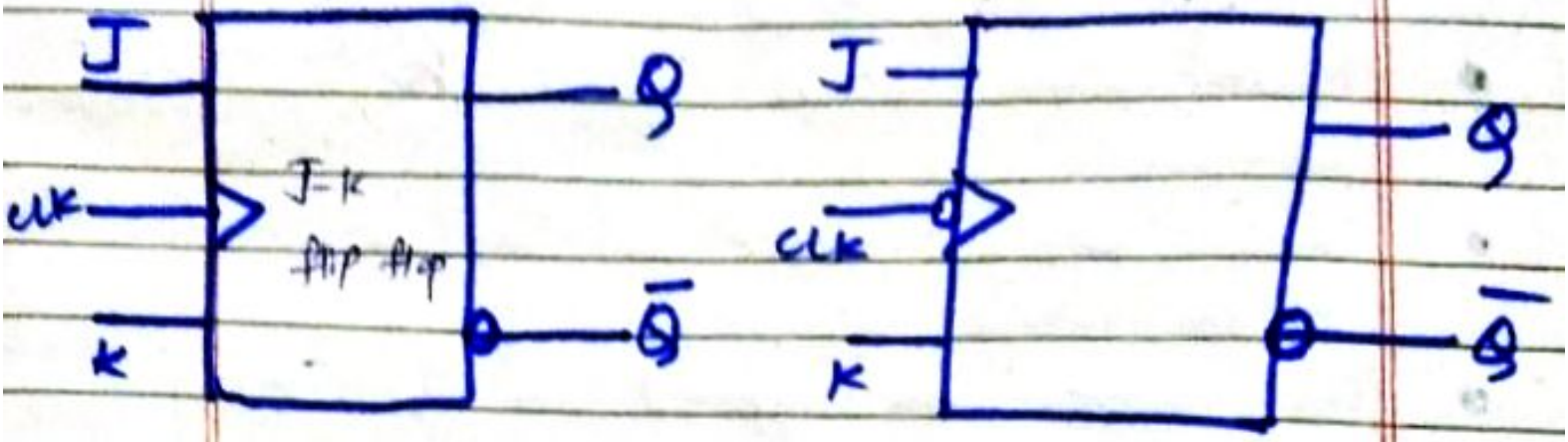
Positive

input		output
CLK	D	Q_{t+1}
0	X	Q_t
1	X	Q_t
↓	0	0
↓	1	1

Negative

3. Edge Triggered J-K flip flop:-

Logic Symbols of Positive & Negative J-K flip flop:-



Positive

Negative.

TRUTH TABLE OF +ve & -ve J-K flip flop:-

Inputs			output
CLK	J	K	Q_{t+1}
0	x	x	Q_t
1	x	x	Q_t
↑	0	0	Q_t
↑	0	1	0
↑	1	0	1
↑	1	1	$\bar{Q_t}$

Input			Output
CLK	J	K	Q_{t+1}
0	x	x	Q_t
1	x	x	Q_t
↓	0	0	Q_t
↓	0	1	0
↓	1	0	1
↓	1	1	$\bar{Q_t}$

★ Master Slave flip-flops-

- Master slave flip-flop have become obsolete and are being replaced by edge triggered flip flops
- Master slave flips have 2 stages.
- Each stage work in a one half of the clock signal
- The inputs are applied in the first half single (of clock).

Truth Table :-

Inputs			Outputs.
CLK	J	K	Q_{t+1}
Pulse	0	0	Q_t
Pulse	0	1	0
Pulse	1	0	1
Pulse	1	1	$\overline{Q_t}$

flip flop Operating Characteristics-

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Following are the Operating Characteristics of flip flop

Propogation delay.
Set-up time
Hold time.
Maximum clock frequency.
pulse width
power dissipation.

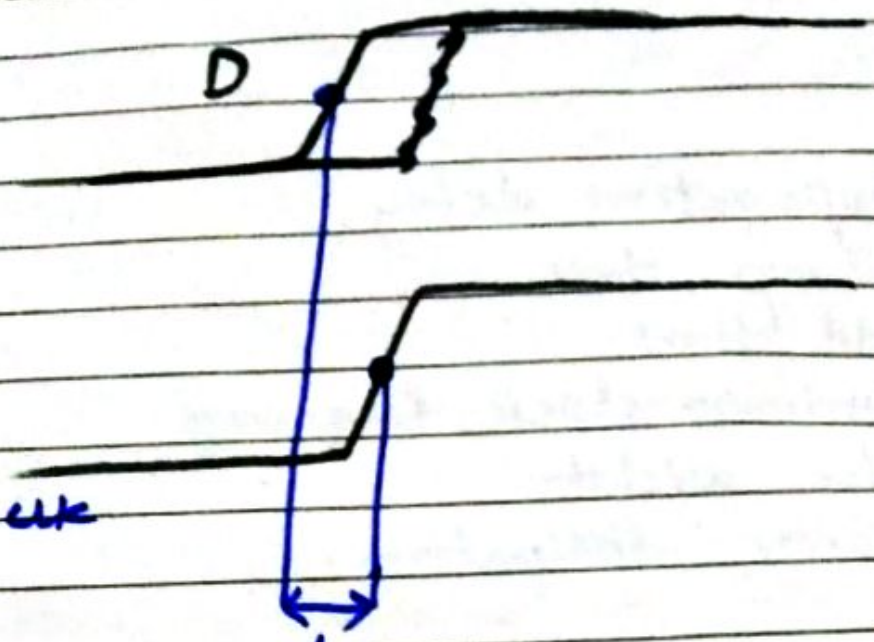
1. Propogation Delays-

The Propogation delay time is the interval of time when the input is applied and the output changes

2. Set-up time:-

- When a clock transition occurs at the clock input of a flip flop. The output of a flip flop is set to a new state based on inputs
- For the flip flop to change its output to a new state at clock transition, the input should be stable.
- The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as set-up time.

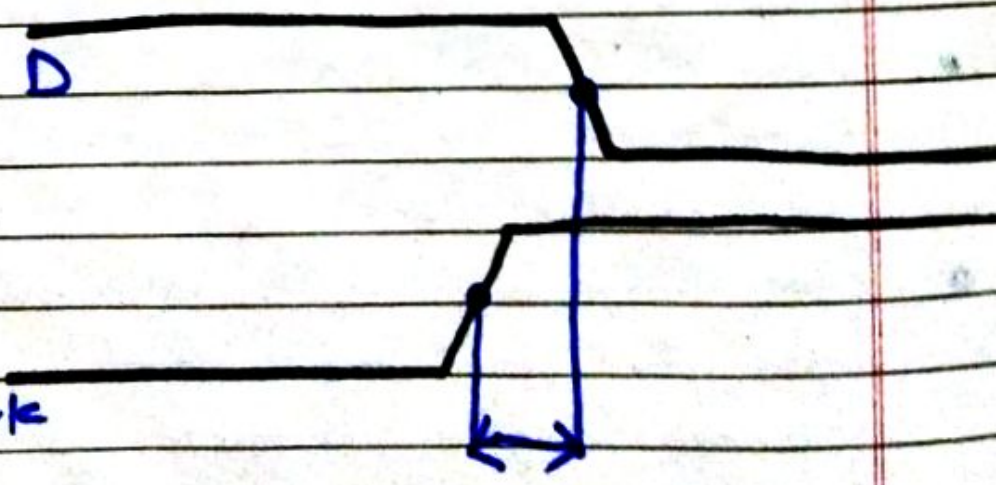
Date:



Set up for D-flip-flop

3- **Hold Time:-**

- The input signal maintained at the flip flop input has to be maintained for a minimum time after the clock transition for the flip flop to reliably clock in input signal.
- The minimum time for which the input signal has to be maintained at the input is hold time of flip-flop



Set up for hold time

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4- Maximum clock Frequency-

A flip flop can be operated at a certain clock frequency. if the clock frequency is increased beyond a certain limit the flip flop will be unable to respond to the fast changing clock transitions.

5- Pulse width:-

- A flip flop uses the clock, Preset and clear inputs for its operation
- Each signal has to be a specified duration for correct operation of flip flop
- The manufacturer specifies the minimum pulse width t_w for each of the three signals
- The clock signal is specified by minimum high time and minimum low time.

6- Power dissipation:-

- A flip flop consumes power during its operation.
- The power consumed by a flip-flop is defined by $P = V_{cc} \times I_{cc}$

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- The flip flop is connected to +5 volts and it draw 5mA of current during operation.
- Power dissipation of flip flop is 25MW.
- A digital circuit is made of a number of gates, functional unit & flip-flops
- The total requirement power of each device should be known so than appropriate dc power source is used to supply Power to digital circuit.

* The 555 timer:-

→ The 555 timer is a versatile and widely used device which can be configured as a **mono-stable one shot** or an **Astable Multivibrator.**

→ An Astable multivibrator is known as an oscillator which does not have any stable state.

→ Therefor it continously changes from one unstable state to the other without any external trigger.

Counters:-

- Counters circuit based on flip flops, are widely used in digital

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System

- Beside counting, these counters are used as frequency dividers and with minor changes in the circuit
- Counters are classified as Synchronous and Asynchronous.
- Asynchronous and synchronous are further classified as up counters & down counters

★ State reduction and its Table:-

- The transition from a current state to the next state is determined by current state and the inputs
- The outputs of the state machine may also change during the transition from the current state to next state
- The output may depends only on the current state
- It is Possible that Two or more state are equivalent
- If equivalent states exist then one of the equivalent state is removed
- Reduction in the number of state results in fewer flip flops

Table :-

state	a	b	c	f	d	d	e	g	d	e	a	1	d
Input	1	1	1	0	1	0	1	0	0	1	0	0	0
output	0	1	1	0	0	1	1	0	1	1	0	0	0

Pg: 327 diagrams

★ Up-down Counterss-

→ Up and down counters depending upon the sequence in which they count

→ They are further classified in terms of the number of states or the range of numbers to which the counters can count

→ An up-down counter can increment its output count value at each clock transition or decrement its count value at clock transition, depending upon the count mode it is configured in.

→ The counter can be reconfigured to count in the opposite during direction its count sequence

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Clock Pulse	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Up-counting sequence of 3-bit Synchronous Counter.

Clock Pulse	Q_2	Q_1	Q_0
0	1	1	1
1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	0	1	0
6	0	0	1
7	0	0	0

down counting sequence of 3-bit Synchronous counter.

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→ A 3-bit synchronous up counter has been discussed earlier. Consider implementation of down counter, the up and down counter can be combined to form a single **configurable up-down counter.**

→ **Integrated Circuit Up/down decade Counter:-** Imp

→ Implementing a four-bit up-down counter by connecting flip flop and logic gates increase circuit size and requires more connection.

→ The 74HC190 is 4-bit up-down synchronous counter available in an integrated circuit form.

Pins:-

1. Parallel data inputs D_0, D_1, D_2 and D_3
2. Data outputs Q_0, Q_1, Q_2 and Q_3
3. Positive edge triggered clock signal.
4. Active-low load input which loads the 4-bit data applied at the counter inputs.
5. Active low CTEN counter Enable input
6. D/$\bar{U}$ the count down/up input; when the input is set to

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logic 1, the counter count down and when input set to logic 0, the counter counts up.

7. The MAX/MIN output that is set to high when terminal counts 1001 is reached when counting up or when the terminal count 0000 is reached when counting down. The MAX/MIN output is logic high for one complete cycle when a terminal count is reached.

8. The Ripple Clock output RCO goes low when the counter reaches the terminal count 1001 and 0000 when counting up and down respectively. The RCO output remains low during the negative half of the clock cycle. The RCO MAX/MIN output along with CTEN input is used to cascade multiple counter ICs for implementing larger counters.

* Circuit diagram for ICs Up & Down:-

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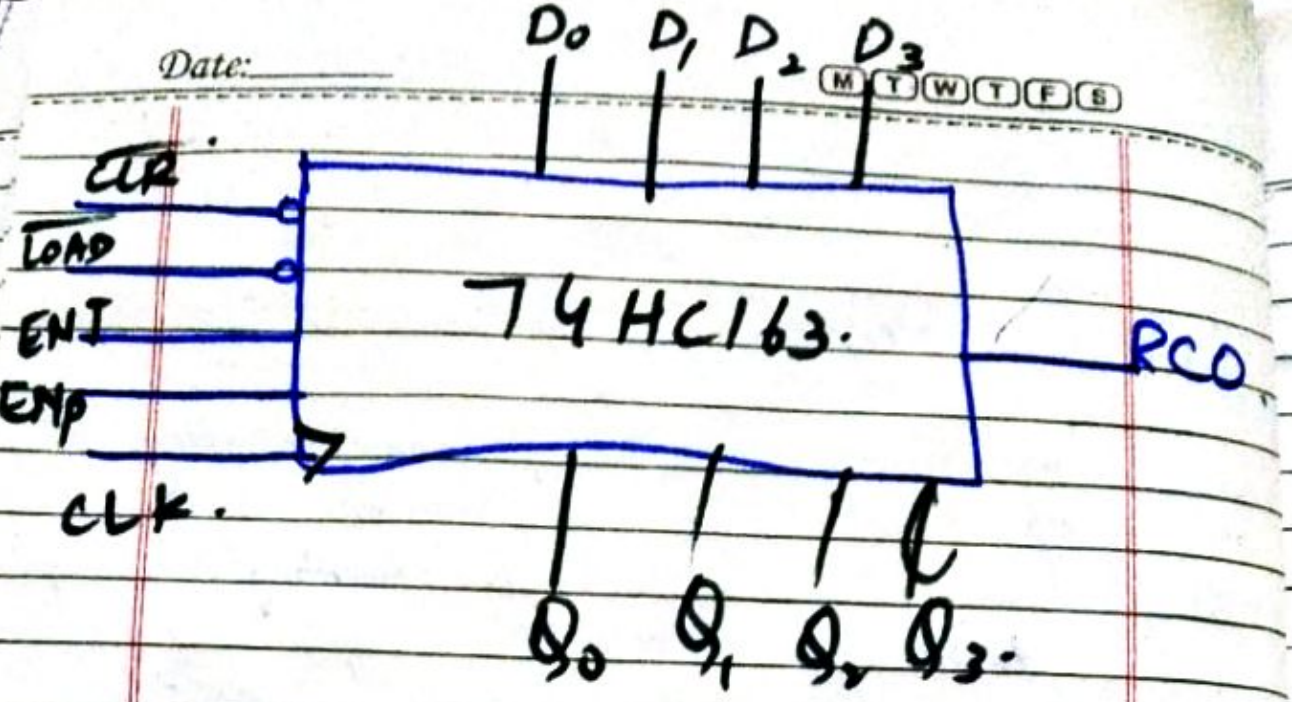

74HC1630 4-bit synchronous counter.

★ Clockwise :-

★ Clockwise moment moves in sequence direction.

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* State Assignment :-

- Each state in a sequential circuit is identified by a unique combination of binary bits.
- Unless the output of the sequential is directly taken from the flip-flop outputs such as counter.
- The state can be selected to allow minimum bit changes when changing from one state to another
- keeping the bits changes to minimum when changing from one state to next, result in simple combinational circuit

State	State Assignment 1	State Assignment 2	State Assignment
a	0 0 0	0 0 1	0 0 0
b	0 0 1	0 1 0	0 0 1
c	0 1 0	0 1 1	0 1 1
d	0 1 1	1 0 0	0 1 0
f	1 0 0	1 1 0	1 1 0

→ **Guidelines :-**

1. Choose an initial code state into which the state machine

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can easily be forced to reset (000 or 111).

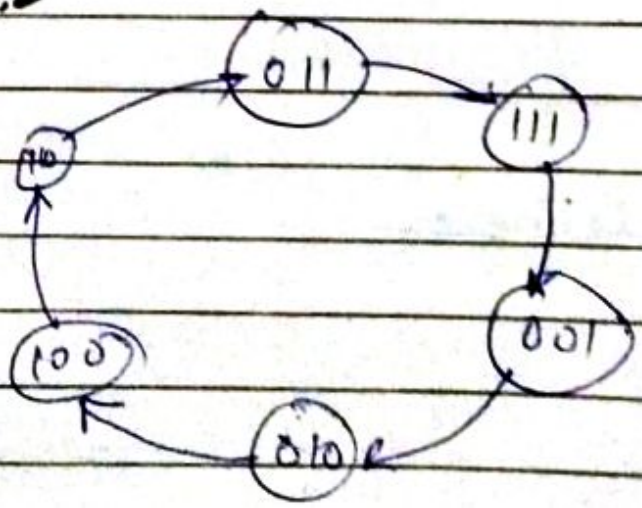
2. Minimize the state variables that change on each transition.
3- Maximize the state variables that change on each transition.
3- Maximize the number of state variable that don't change in a group of related states.
4. if there are unused state, Then choose the best state variable combination to achieve first three goals.

---

* Moore Machine:-

1. The clocked synchronous sequential circuit has six states.
2. On each clock transition the machine sequence through states 011, 111, 001, 010, 100 and 110.

Digram:-



Date:

* Mealy Machine:-

1- The sequential circuit represented earlier as a Moore Machine is described as Mealy Machine.

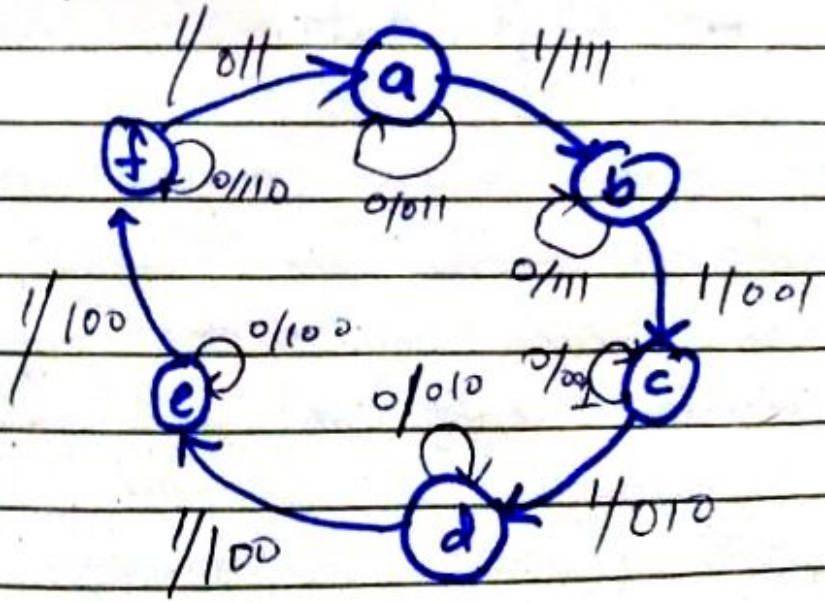
2- The output depends upon the Present state at the inputs

3. The state diagram shows six stat

4- When input is 1, the machine switches from its Present state to next.

5. if input is Zero, machine will remain in present state.

Diagram :-



* Shift Registerse-

→ The need to storage binary data was discussed

Date: M T W T F S

earlier.

→ In digital circuit multi bit data has to be stored temporarily until it is processed.

→ A flip flop is able to store a single binary bit of information

→ Multiple bits of data are stored by using multiple flip-flops which have their clock input connected together

A register basically Performs TWO function.

→ **it stores data.**

→ **Move or shift data.**

→ shifting of data involves shifting of bits from one flip flop to the other within the register or moving data in and out of register

Types-

(i) Serial In / Shift Right / Serial out
(ii) Serial in / shift left / "
(iii) Serial in / Parallel out

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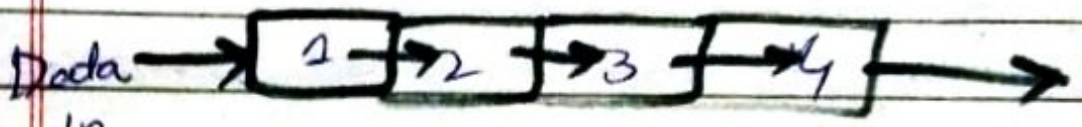
(iv) Parallel In/Serial out

(v) Parrallel In/Parallel out

(i) Serial In/Shift right/Serial out operation:-

→ Data is shifted in right hand direction one bit at a time with each transition of clock signal.

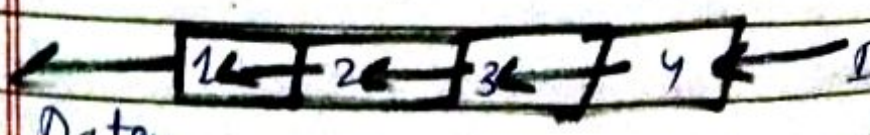
→ The data enters the shift registers serially from left hand side and four clock transition the 4-bit register has 4 bits of data.



(ii) Serial out/shift left/Serial out operation

→ Data is shifted in left hand direction one bit of a time with each transition of the clock signal

→ The data enters serially in shift register from the right hand side and after four clock transition the 4 bit registers has 4 bits of data



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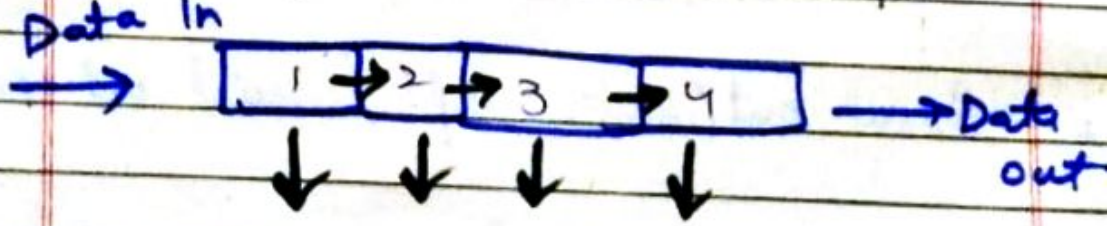
(iii) Serial In / Parallel out Operation:

→ Data is shifted in the left-hand direction one bit at a time with each transition of clock signal.

→ The data enters the shift register serially from the right hand side and after four clock transitions the 4-bit register has 4 bits of data.

→ The data is shifted out in Parrallel by application of a single clock signal.

→ Shift register has 4 Parallel outputs.



(iv) Parallel In/Serial out Operation:

→ The register has Parallel inputs, data bits are loaded in Register in Parallel by activating a load signal.

→ The data is shifted out serially by application of clock signals.

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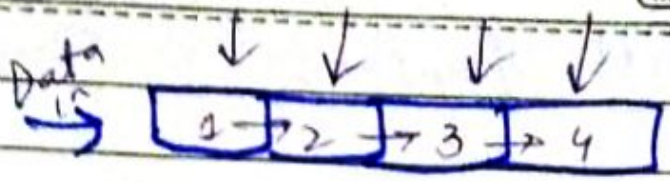


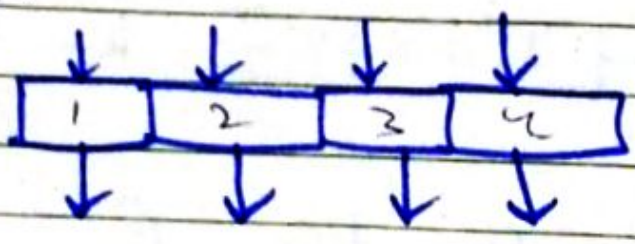
(V) Parallel in / Parallel out operation:-

→ The register has Parallel inputs and Parallel outputs.

→ Data is entered in Parallel by applying a single clock Pulse

→ Data is latched by flip-flops on

→ the clock transition and its available in Parrallel form at the flip-flop outputs



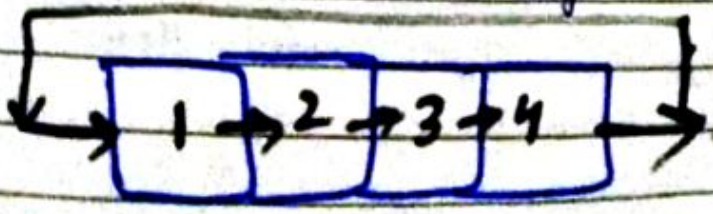
(VI) Rotate Right operation:-

→ The serial output of the register is connected to the serial input of register.

→ By applying clock pulses data is shifted

→ right.

→ The data shifted out of the serial out pin at the right hand side.



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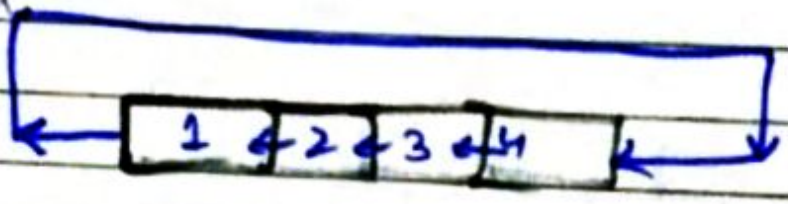
(vii) Rotate left Operation:-

→ The serial output of the register is connected to serial input of registers.

→ By applying clock pulses data is shifted.

→ The data shifted out of the serial out pin at the left hand side is re-circulated back into shift register input at right hand.



* Shift Register Counters-

→ Shift register counters are basically, shift registers connected to perform left and rotate right operations.

→ When data is rotated through a register counter a specific sequence of state is repeated.

→ Two commonly used register counters in digital logic are the Johnson counter & Ring counter.

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Types:-

(i) Johnson Counter:-

In a Johnson counter, the $\overline{Q}$ output of the last flip-flop of the shift register is connected to the data input of the first flip flop

(ii) Ring Counter:-

The Ring counter is similar to the Johnson counter, except that the Q output of the last flip-flop of the shift register is connected to data input of the first flip-flop of shift register.

Application of Shift Register:-

- Serial to Parallel converter.
- Keyboard Encoder.
- Programmable sequential logic
- The Registered Mode
- Software Mode Specification

Memory:-

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- Sequential Circuits can not operate without a memory element.
- Memory elements used in sequential circuits are relatively small and store few binary bit of information
- Large Memories capable of storing very large amounts of information are used in computer system.
- Memories store data in Units that have one, four, eight or higher number of bits.
- Smallest Unit of binary data is bit.
- Data is also handled in a 4-bit unit called Nibble.

Types of Memory:-

→ **RAM**
→ **ROM.**

1- RAM:-

RAM is known as Random Access Memory. Ram is divided into two types i.e static RAM, Dynamic RAM.

- Static RAM which uses flip-flop as storage elements
- DYNAMIC RAM which uses capacitors to store binary information.

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- In static Ram, each cell which is capable of storing a binary 0 or 1 is made up of a flip-flop which retains information.
- Dynamic RAM on the other hand, uses a capacitor to store a single bit of data. To store binary 1, the capacitor is Charged and to store binary 0, the capacitor is uncharged state.

2- ROM:-

ROM contains Permenent data - that can not be changed. ROM memory does nd allow write operation. ROM stores data that are used repeatdly in system applications, such as tables, conversion. ROM retains data when the power is turned off.

→ **MASK ROM:** Data is Permenantly stored during manufacturing Process

→ **PROM:** Programmable ROM allows storage of da by user using a PROM Programmer.

→ **EPROM:** Erasable Program ROM allows erasing of stored data.

→ **VU EPROM:** Data is erased by exposing PROM to UV.

→ **EEPROM:-** Electrically Erasable PROM is

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★ Memory Capacity & Density

- Each Memory array has a maximum capacity to store information in the form of bits
- Thus a 16k x 8 memory, stores 16k bytes or 16x1024 = 16384 bytes or 131072 bits.
- A 32 k x 4 memory stores 32k nibble or 32x1024 = 32768 nibbles or 131072 bits
- The total number of cell in each case is 131072.
- Memory density on other hand Specifies the number of bits stored Per unit area.
- More the number of bits stored in unit area more dense the memory, more bits are stored in less space.
- The capacity and the density of the Memory are determined by total number of cell implemented in Unit Area.

★ First In / First Out Operations-

→ Digital system recieves data or transfer data to recieve

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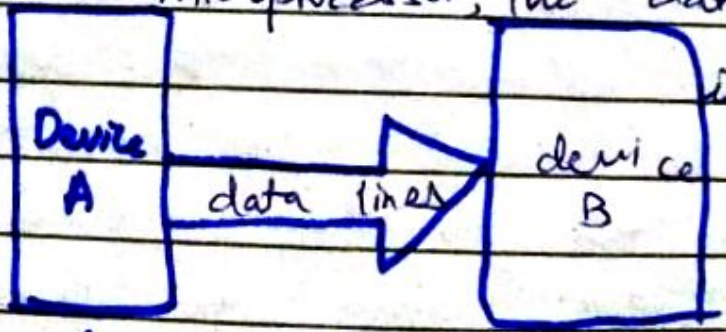
that are operating at different data rates.

→ A Computer (microprocessor), for example recieve data from keyboard as a user types information. The keyboard is very slow device which generates data at a rate of few bytes per second.

→ **Microprocessor** on the other hand is very fast and can process information at very high data rates

• Devices that operate at different data rates can not be connected to each other directly through their data lines because the device that operate at very high data rates are slow down to data rate of slow device

In microprocessor, the data insertion is fast



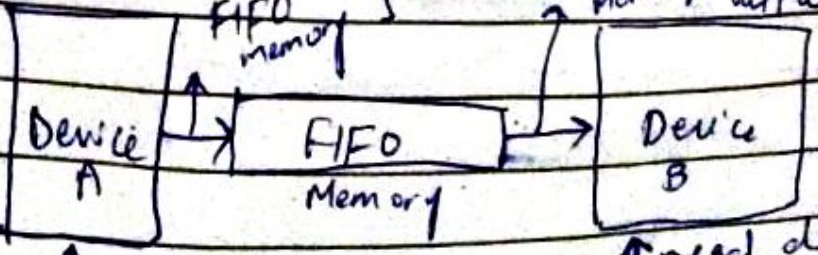
→ Imp diagram

↑ write data

↑ read data

FIFO memory output.

FIFO memory



↑ write data

↑ read data

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* Last In/First Out Operation:-

→ Last in first out memory finds application the computer systems where it is used to implement a stack. The operation of a stack can be understood by viewing stack of plates

→ In a stack of Plates the first placed at the bottom and the next place placed is placed on top and the third plate is placed on the top of second place & so on.

→ Plates are removed one at a time from the top of the stack, thus the last plate placed on the stack top is the first place to be removed.

→ In a register base (LIFO) memory implementation a set of Parallel In/Parallel out registers are connected together such that data data is Pushed down or pulled down when data is stored or removed from memory respectively.

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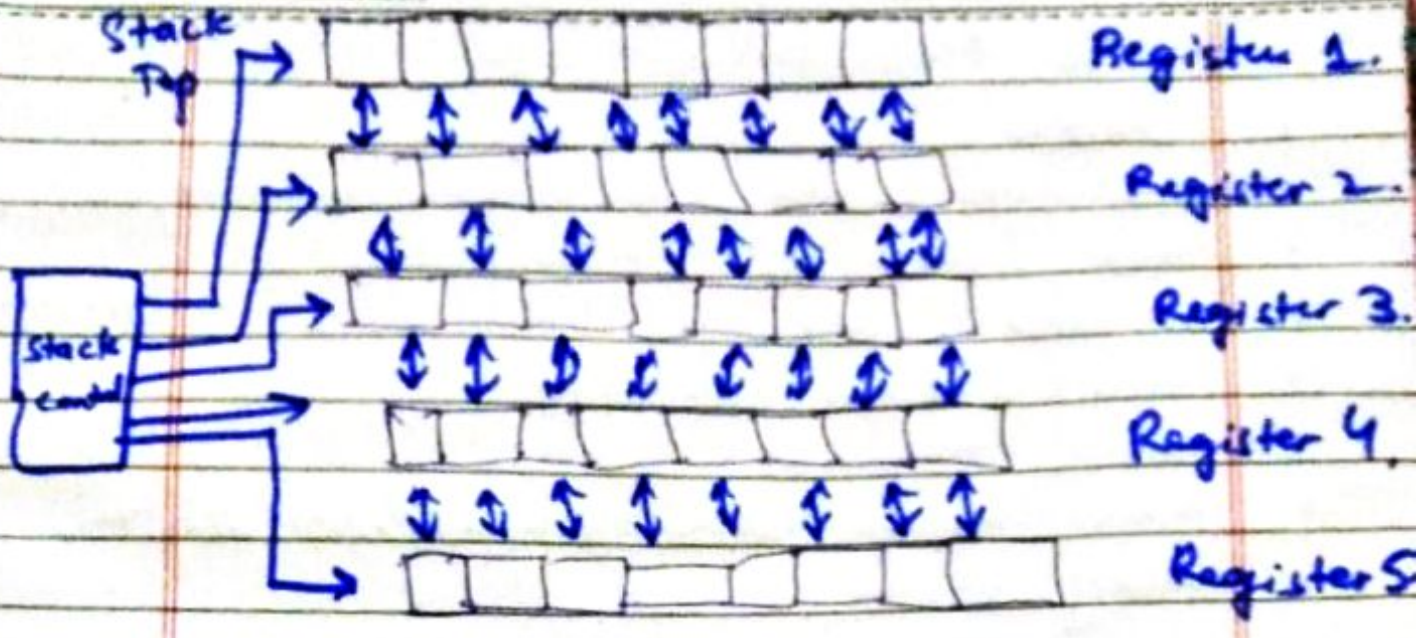

A five bit LIFO.

CS302 final Tips.

→ Latches / flip-flops.
→ State Machines (Diagrams)
→ Shift Register.
→ Memory

Latches & flip flop:-

- The gated S-R latch.
- The gated D latch
- Edge triggered flip flop
- Types of edge trigered flip flops (3)
- Master slave flip flop.
- Flip-flop operating characterstics → MCQs.
- Propogation delay, setup time, Power dissipation
- The 555 timer.
- Clock Skew.

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State Machines :-

- Counters
- Up counter (with state diagram and table)
- Down counter (" " ")
- Up down counter (" " ")
- State reduction / its table
- State Assignment
- Moore Machine (state diagram / next stat table)
- Mealy Machine (" / ")

Shift Register :-

- Shift Register.
- Types.
- Shift register counter & its types (2)
- Application of shift register (2).
  (keyboard encoder, series to parallel converter).

Memory :-

- Memory
- Types of Memory (RAM, ROM)
- Types of RAM (2), ROM (3).
- Memory capacity and density.
- Flash memory.
- First In / first out.
- Last In / first out.

Past Papers.

→ Truth tables → gated S-R latch
→ logic diagram → gated D latch

→ ± edge triggered S-R flip flop
→ ± edge triggered D " "
→ ± edge triggered J-K flip flop

→ Master slave ± J-K flip flop.
→ J-K flip flop with asynchronous input

Q: ABEL symbols for NOT, AND, OR, EOR.

Q: D/b Moore Machine / Mealy machine.

Q: How many bytes will be there in 16K×8 memory.

16 K bytes
16×1024 = 16384 bytes
16384 × 8 = 131072 bits

Q: Explain Latches.

Q. Write down application of shift registers:
① Serial to Parallel converter ② Keyboard encod

Q. Explain Rotate left right operation with help of diagram?

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Q. Define quantization Process.

The Process of converting analogue signal into digital signals are called quantization Process.

Q. Name three operation Performed on flash memory.

→ Programming Operation.
→ Read operation
→ Erase operation.

Bytes to bit conversion.

→ Mooz Subjective file.

- Asynchronous 3-bit up counter output table.
- Serial in / serial out circuit diagram.
- Types of edge triggered flip-flop
- SR latch table
- Volatile memory time.
- State assignment / State reduction
- D-flip flop table
- J-K flip-flop timing diagram.

→ Next state - table diagram.
→ Counters.
→ J-K flip flop.
→ shift registers.

→ EWB → 5.12.1

→ Electronic workbench.

CS302P → VU Rocky malik. Youtube channel.

CS302 → VU Knowledge MCQ Preparation

→ **Memory Units.**

1 bit — Binary (0, 1)

4 bits = 1 nibbles.

8 bits = 1 byte

1024 Bytes = 1KB

→ **Step by step capacity of total number to store cell.**

16K → bytes

16 × 8 → Ans × 8 → Ans.

→ **Memory Signals & Basic operations.**

- **Read** : Reading of information from memory
- **Write** : writing of data to the memory.

→ **Application of Multiplexer.**

- Data Routing
- Parrallel to Serial conversion
- Logic function generator

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→ Three application of edge triggered J-K flip-flop:-

→ J-K flip flop used as sequence detector.
→ J-K flip flop used as a frequency divider
→ J-K flip flop used as shift register

→ Three application of edge triggered D- flip flop:

→ Data storage
→ Syncharonyzing inputs
→ Parallel data transfer

→ Memory types:-
RAM ⟶ MBS → volatile → temporary
ROM ⟶ GBS → non-volatile → Permenant

Types of RAM:-

SRAM: static RAM → Use flip-flop → don't need refresh again
DRAM: Dynamic RAM → use capacitor → ne to refresh again.

Types of ROM:-

PROM:- it modified once by users
EPROM: Erasable and Programable it

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is used many times. you can used it and erased many times. UV light is used to erase. (40 mints)

EEPROM:- electricity erasable & PROM. it is programmed and erase electrically (10,000 times) (4 to 10 ms) particular location.

Q: Convert decimal to gray code.

pg 36 → MCQs

→ **74HC163 has how many bits.**

74HC163 has two input bits.

ENP, ENT → inputs } -diagram

RCO → output }

→ **Convert decimal number to equivalent binary 392.**

2	392
2	196 - 0
2	98 - 0
2	49 - 0
2	24 - 1
2	12 - 0
2	6 - 0
2	3 - 0
	1 - 1

$(110001000)_2$.

2 | 192

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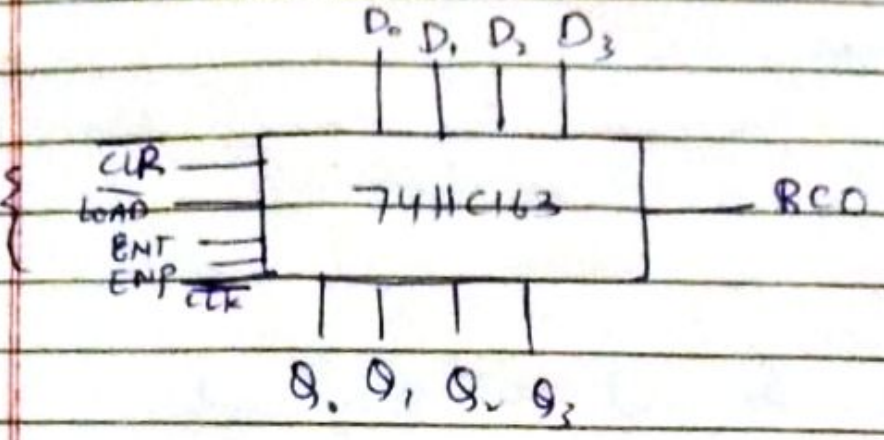
→ Integrated Circuit Synchronous Counters.



inputs → $\overline{CLR}$, $\overline{CLK}$, $\overline{LOAD}$, ENT, ENP

output → RCO.

→ Parallel data input (D_0, D_1, D_2, D_3)

→ Data output (Q_0, Q_1, Q_2, Q_3)

→ Low inputs ($\overline{CLR}$, $\overline{LOAD}$)

→ High inputs (ENT, ENP)

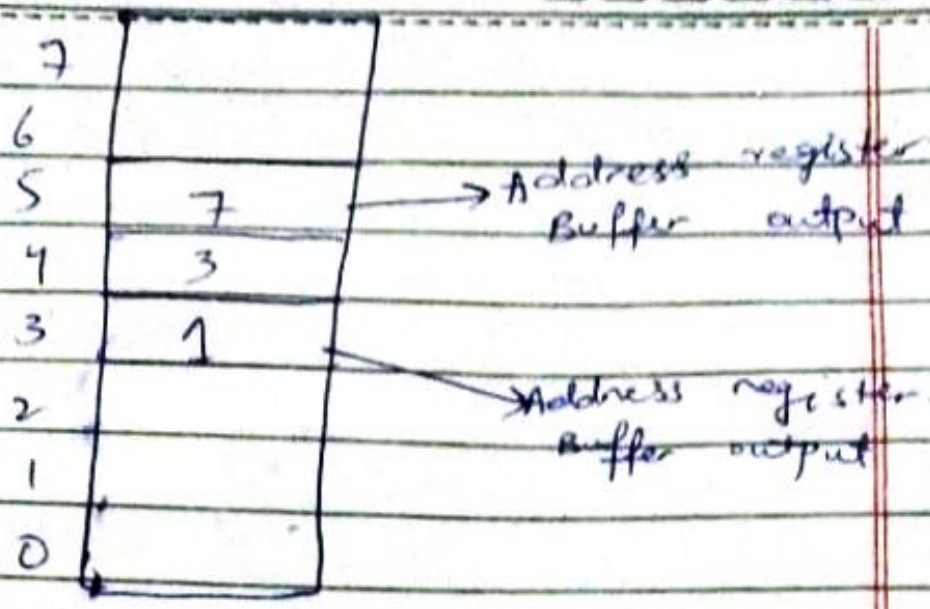
→ Identification of object in circuits.

→ output of circuit is always its input

output is same (A).

→ Caveman Numbers → Pg. 11.

→ Implementation of a model of FIFO buffer using RAM;



→ State diagram of 3-bit up/down counter

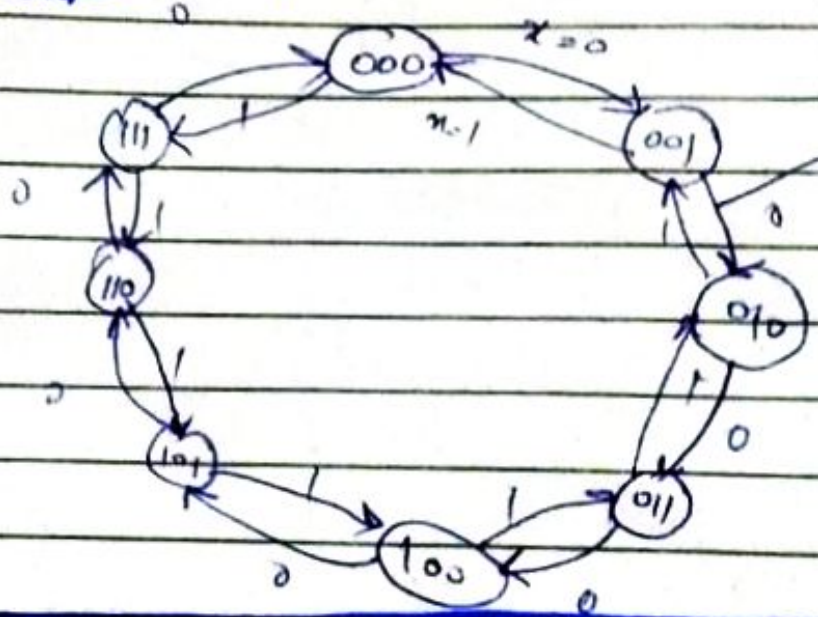


Table 2.8.5

Present State			Next state (x=0)			Previous State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1	1	1	1
0	0	1	0	1	0	0	0	0
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	0	1	0
1	0	0	1	0	1	0	1	1
1	0	1	1	1	0	1	0	0
1	1	0	1	1	1	1	0	1
1	1	1	0	0	0	1	1	0