

**CS-302 Important Mcq's**  
**For Final Term !!**  
**Solve By Vu-Topper RM!!**

وَتَعَزُّ مِنْ تَشَاءٍ وَتُذَلُّ مِنْ تَشَاءٍ



PROFESSIONAL & ONLINE ACADEMY



**NOTHING IS  
IMPOSSIBLE**

**All Paid Services**

- ❖ LMS Handling
- ❖ Important Notes
- ❖ Online Classes
- ❖ Projects
- ❖ Assignments
- ❖ Quiz
- ❖ GDB's

**JOIN US NOW**

For More Info  
Contact us at:

**Rizwan Manzoor**

**0322-4021365**

**Question No:1**

**(Marks:1)**

**Vu-Topper RM**

The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the \_\_\_\_\_ can be pressed at any time either on the first floor or the second floor in elevator.

REQ0

OPEN

**REQ1 Page370**

FLOOR1

**Question No:2**

**(Marks:1)**

**Vu-Topper RM**

A decade counter is \_\_\_\_\_

Mod-3 counter

Mod-5 counter

Mod-8 counter

**Mod-10 counter Page274**

**Question No:3**

**(Marks:1)**

**Vu-Topper RM**

PALs tend to execute \_\_\_\_\_ logic.

SPD

**SOP**

SAC

SAP

**Question No:4**

**(Marks:1)**

**Vu-Topper RM**

A counter is implemented using three (3) flip-flops, possibly it will have \_\_\_\_\_ maximum output status.

2

4

**8 Page272**

10

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:5**

**(Marks:1)**

**Vu-Topper RM**

There are \_\_\_\_\_ possible combinations of the Simple Mode in which OLMC can be configured.

**Three Page201**

Four

Five

Six

**Question No:6**

**(Marks:1)**

**Vu-Topper RM**

Once the state diagram is drawn for any sequential circuit the next step is to draw

Transition table

Karnaugh map

**Next- state table**

Logic expression

**Question No:7**

**(Marks:1)**

**Vu-Topper RM**

In gated SR latch, what is the value of the output if  $EN=1$ ,  $S=0$  and  $R=1$ ?

**0**

1

2

3

**Question No:8**

**(Marks:1)**

**Vu-Topper RM**

If  $S=1$  and  $R=0$ , then for positive edge triggered flip-flop

0

**1 Page230**

2

3

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:9**

**(Marks:1)**

**Vu-Topper RM**

According to Moore circuit, the output of synchronous sequential circuit depend/s on \_\_\_\_\_ of flip flop.

Previous state

**Present state**

Next state

External state

**Question No:10**

**(Marks:1)**

**Vu-Topper RM**

The outputs of SR latches in elevator state machine are feed back to the \_\_\_\_\_ gate array for connection to the D-flipflops.

NOT

**AND Page372**

OR

XOR

**Question No:11**

**(Marks:1)**

**Vu-Topper RM**

In memory write cycle, the time for which the WE signal remains active is known as the \_\_\_\_\_.

Write address setup

**Write pulse width Page397**

Write delay width

Write data time

**Question No:12**

**(Marks:1)**

**Vu-Topper RM**

\_\_\_\_\_ is one of the examples of synchronous inputs.

**J-K input Page235**

EN input

Preset input (PRE)

Clear Input (CL)

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:13** (Marks:1) **Vu-Topper RM**

\_\_\_\_\_ occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

Race condition

**Clock Skew Page226**

Ripple Effect

None of given options

**Question No:14** (Marks:1) **Vu-Topper RM**

A latch is a temporary storage device that has \_\_\_\_\_ stable states.

**Two Page211**

Three

Four

Five

**Question No:15** (Marks:1) **Vu-Topper RM**

A NOR based S-R latch is implemented using \_\_\_\_\_ gates instead of \_\_\_\_\_ gates.

XOR, NAND

NOR, XOR

**NOR, NAND Page213**

OR, XOR

**Question No:16** (Marks:1) **Vu-Topper RM**

RCO stands for \_\_\_\_\_

Reconfiguration Counter Output

Ripple Counter Output

Reconfiguration Clock Output

**Ripple Clock Output Page285**

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:17**

**(Marks:1)**

**Vu-Topper RM**

A Divide-by-20 counter can be achieved by using

**Flip-Flop and DIV 10**

Flip-Flop and DIV 16

Flip-Flop and DIV 32

Div 10 and DIV 16

**Question No:18**

**(Marks:1)**

**Vu-Topper RM**

The terminal count of a modulus-13 binary counter is Select correct option:

0000

1111

**1101**

1100

**Question No:19**

**(Marks:1)**

**Vu-Topper RM**

A synchronous decade counter will have \_\_\_\_\_ flipflops.

3

**4 Page281**

7

10

**Question No:20**

**(Marks:1)**

**Vu-Topper RM**

Divide-by-32 counter can be achieved by using-----

Flip-Flop and DIV 10

**Flip-Flop and DIV 16**

Flip-Flop and DIV 32

DIV 16 and DIV 32

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:21**

**(Marks:1)**

**Vu-Topper RM**

A 4-bit binary up/down counter is in the binary state of zero. The next state in the UP mode is-----

0001

1000

1110

**1111**

**Question No:22**

**(Marks:1)**

**Vu-Topper RM**

An Astable multivibrator is known as a(n) \_\_\_\_\_

**Oscillator Page258**

Booster

One-shot

Dual-shot

**Question No:23**

**(Marks:1)**

**Vu-Topper RM**

Flash memory Operation are classified into \_\_\_\_\_ different operation.

One

Two

**Three Page413**

Four

**Question No:24**

**(Marks:1)**

**Vu-Topper RM**

In designing any counter, the transition from a current state to the next state is determined by-----

**Current state and inputs Page332**

Only inputs Only current state

Positive-Edge triggered

Negative-Edge triggered

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:25**

**(Marks:1)**

**Vu-Topper RM**

A negative edge-triggered flip-flop changes its state when-----

Enable input (EN) is set

Preset input (PRE) is set

Low-to-high transition of clock

**High-to-low transition of clock (Page 228)**

**Question No:26**

**(Marks:1)**

**Vu-Topper RM**

The S-R latch has two inputs, therefore \_\_\_\_\_ different combinations of inputs can be applied to control the operation of the S-R latch.

two

**four Page212**

eight

sixteen

**Question No:27**

**(Marks:1)**

**Vu-Topper RM**

Three cascaded modulus-10 counters have an overall modulus of Select correct option:

30

100

**1000**

10000

**Question No:28**

**(Marks:1)**

**Vu-Topper RM**

In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in \_\_\_\_\_ when Distributed refresh is used.

4.8 microsec

5.9 microsec

**7.8 microsec Page406**

5.5 microsec

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:29**

**(Marks:1)**

**Vu-Topper RM**

The 64-cell array organized as 8 x 8 cell array is considered as an 64 byte memory  
as a 16 byte memory

**as an 8 byte memory Page387**

as an 4 byte memory

**Question No:30**

**(Marks:1)**

**Vu-Topper RM**

\_\_\_\_\_ Counters as the name indicates are not triggered simultaneously

**Asynchronous Page262**

Synchronous

Positive-Edge triggered

Negative-Edge triggered

**Question No:31**

**(Marks:1)**

**Vu-Topper RM**

You have to choose suitable option when your timer will reset by considering this given code:

TRSTATE.CLK = clk;

TMRST: = (TRSTATE == NSY2) # (TRSTATE == EWY2);

**NSY2 or EWY2**

NSSR or TMRST

EWSR or NSRED

EWRed or EWYel

**Question No:32**

**(Marks:1)**

**Vu-Topper RM**

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

True

**False**

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:33** (Marks:1) **Vu-Topper RM**

In asynchronous digital systems all the circuits change their state with respect to a common clock

**False Page245**

True

**Question No:34** (Marks:1) **Vu-Topper RM**

A \_\_\_\_\_ can not operate without a memory element.

**Counter Page211**

**Question No:35** (Marks:1) **Vu-Topper RM**

A complete unit of information is sometimes called a \_\_\_\_\_.

**Word Page387**

**Question No:36** (Marks:1) **Vu-Topper RM**

The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the \_\_\_\_\_

**Set-up time Page234**

Hold time

Pulse Interval time

Pulse Stability time (PST)

**Question No:37** (Marks:1) **Vu-Topper RM**

Which of the following is a volatile memory?

**DRAM**

PROM

EPROM

EEPROM

**Question No:38** (Marks:1) **Vu-Topper RM**

The combinational digital circuits have \_\_\_\_\_ storage element; therefore combinational circuits handle only instantaneous inputs.

**No Page210**

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:39**

**(Marks:1)**

**Vu-Topper RM**

The inputs can be directly mapped to Karnaugh maps.

**J-K Page300**

**Question No:40**

**(Marks:1)**

**Vu-Topper RM**

To write data to the memory the memory the write cycle is initiated by

**Applying the address signals Page397**

**Question No:41**

**(Marks:1)**

**Vu-Topper RM**

If  $S=1$  and  $R=1$ , then  $Q(t+1) = \underline{\hspace{2cm}}$  for negative edge triggered flip-flop

**Invalid Page233**

**Question No:42**

**(Marks:1)**

**Vu-Topper RM**

The minimum time for which the input signal has to be maintained at the input of flip-flop is called \_\_\_\_\_ of the flip-flop.

**Hold time Page242**

**Question No:43**

**(Marks:1)**

**Vu-Topper RM**

The chip enable access time which is the time for the valid data to appear after the \_\_\_\_\_ transition of the chip select signal  $\bar{CS}$ .

**High-to-low Page397**

**Question No:44**

**(Marks:1)**

**Vu-Topper RM**

The FAST Model Page Access allows \_\_\_\_\_ memory read and access times when reading successive data values stored in consecutive locations on the same row.

**Faster Page406**

**Question No:45**

**(Marks:1)**

**Vu-Topper RM**

A modulus-14 counter has fourteen states requiring

**4 flip flops**

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:46** (Marks:1) **Vu-Topper RM**

A memory organized to store nibble data values requires a \_\_\_\_\_ wide data bus.

**4-bit Page390**

**Question No:47** (Marks:1) **Vu-Topper RM**

A-stable multi-vibrator is an Oscillator which does not have any\_\_\_\_\_.

**Astable Multivibrator Google**

**Question No:48** (Marks:1) **Vu-Topper RM**

The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as \_\_\_\_\_ inputs.

**Synchronous**

**Question No:49** (Marks:1) **Vu-Topper RM**

With a 100 KHz clock frequency, eight bits can be serially entered into a shift register in

**80 micro seconds**

**Question No:50** (Marks:1) **Vu-Topper RM**

Number of states in an 8-bit Johnson counter sequence are:

**16**

**Question No:51** (Marks:1) **Vu-Topper RM**

UVEPROM is stands for-----

**Ultra-Violet Erasable Programmable Read Only Memory.**

**Question No:52** (Marks:1) **Vu-Topper RM**

The synchronous counters are also known as Ripple Counters:

**False**

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:53** (Marks:1) **Vu-Topper RM**  
-----are implemented by combining combinational circuits with memory elements.

**Sequential circuits Page 211**

**Question No:54** (Marks:1) **Vu-Topper RM**  
The EPROM uses \_\_\_\_\_array with an isolated-gate structure.

**NMOSFET Page 411**

**Question No:55** (Marks:1) **Vu-Topper RM**  
A one-shot mono-stable device contains \_

**NOR gate, Resistor, Capacitor and NOT Gate**

**Question No:56** (Marks:1) **Vu-Topper RM**  
The counter states or the range of the number of a counter is determined by the formula(“n” represented the total number of flip-flops )

**2 raise to power n**

(n raise to power 2)

(n raise to power 2 and then minus 1)

(2 raise to power n and then minus 1)

**Question No:57** (Marks:1) **Vu-Topper RM**  
THE FOUR OUTPUTS OF TWO 4-INPUT MULTIPLEXERS,  
CONNECTED

TO FORM A 16-INPUT MULTIPLEXER, ARE CONNECTED  
TOGETHER THROUGH A 4-INPUT \_\_\_\_\_ GATE

**OR Page171**

**Question No:58** (Marks:1) **Vu-Topper RM**  
A FIELD-PROGRAMMABLE LOGIC ARRAY CAN BE  
PROGRAMMED BY THE USER AND NOT BYTHE  
MANUFACTURER.

**TRUE Page182**

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:59** (Marks:1) **Vu-Topper RM**

In sequential circuits memory elements are connected with\_\_\_\_\_.

**Common clock**

**Question No:60** (Marks:1) **Vu-Topper RM**

The terminal count of a modulus -13 binary counter is

**1101**

**Question No:61** (Marks:1) **Vu-Topper RM**

The alternate solution for a multiplexer and a register circuit is \_\_\_\_\_.

**Parallel in / Serial out shift register Page356**

**Question No:62** (Marks:1) **Vu-Topper RM**

A 8-bit serial in / parallel out shift register contains the value "8", \_\_\_\_\_ clock signal(s) will be required to shift the value completely out of the register.

**8 Page356**

**Question No:63** (Marks:1) **Vu-Topper RM**

Which of the following output equations determines the output of the state machine?

**Max-Q0Q1EN Page382**

**Question No:64** (Marks:1) **Vu-Topper RM**

The CONSTATE.CLK = Clock is used to indicate that the \_\_\_\_\_ state variables change on a clock transition.

**CONSTATE**

**Question No:65** (Marks:1) **Vu-Topper RM**

Memory is arranged in \_\_\_\_\_.

**Two-dimensional manner Page396**

linear fashion

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:66** (Marks:1)

**Vu-Topper RM**

The n flip-flops store \_\_\_\_\_ states.

**$2^n$**

**Question No:67** (Marks:1)

**Vu-Topper RM**

In DRAM read cycle R /W<sup>-</sup> signal is activated to read data which is made available on the \_\_\_\_\_ data line.

D(IN)

**D(OUT) Page405**

D(AB)

D(INT)

**Question No:68** (Marks:1)

**Vu-Topper RM**

A SOP expression can be implemented by an \_\_\_\_\_ combination of gates.

**AND-OR Page78**

OR-XOR

AND-NAND

XOR-NOR

**Question No:69** (Marks:1)

**Vu-Topper RM**

Why demultiplexer is called a data distributor?

**Single input to Single Output**

**Question No:70** (Marks:1)

**Vu-Topper RM**

If the number of samples that are collected is reduced by half, the reconstructed signal will be \_\_\_\_\_ from/to the original.

**Very different Page1**

**Question No:71** (Marks:1)

**Vu-Topper RM**

The AND Gate performs a logical \_\_\_\_\_ function.

**Multiplication Page40**

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:72**

**(Marks:1)**

**Vu-Topper RM**

\_\_\_\_\_ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.

**Combinational Input/Output Page185**

Combinational Input/Output

Combinational Output

Programmable polarity

**Question No:73**

**(Marks:1)**

**Vu-Topper RM**

A 3-variable Karnaugh map has

**Eight cells Page89**

three cells

sixteen cells

four cells

**Question No:74**

**(Marks:1)**

**Vu-Topper RM**

The ABEL Input file can use a \_\_\_\_\_ instead of the equation to specify the Boolean expressions.

**Truth Table Page370**

State Diagram

Karnaugh Map

Logic Circuit

**Question No:75**

**(Marks:1)**

**Vu-Topper RM**

The \_\_\_\_\_ gate and \_\_\_\_\_ gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.

**AND,OR Page146**

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:76**

**(Marks:1)**

**Vu-Topper RM**

In the keyboard encoder, how many times per second does the ring counter scan the key board?

**650 scans/second**

600 scans/second

625 scans/second

700 scans/second

**Question No:77**

**(Marks:1)**

**Vu-Topper RM**

The domain of the expression  $AB'CD + AB' + C'D + B$  is

**A, B, C and D**

**Question No:78**

**(Marks:1)**

**Vu-Topper RM**

The Adjacent 1s Detector accepts 4-bit inputs. If \_\_\_\_\_ adjacent 1s are detected in the input, the output is set to high.

**1**

2

3

4

**Question No:79**

**(Marks:1)**

**Vu-Topper RM**

When the transmission line is idle in an asynchronous transmission

**It is set to logic high Page349**

**Question No:80**

**(Marks:1)**

**Vu-Topper RM**

In NAND based S-R latch, output of each \_\_\_\_\_ gate is connected to the input of the other \_\_\_\_\_ gate.

**NAND, NAND Page211**

NOR, NAND

NAND, NOR

NOR, NOR

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:81** (Marks:1) **Vu-Topper RM**  
PLDs have In-System Programming (ISP) capability that allows the \_\_\_\_\_ to be programmed after they have been installed on a circuit board.

**PLDs Page194**

**Question No:82** (Marks:1) **Vu-Topper RM**  
The terminal count of a 4-bit binary counter in the UP mode is

\_\_\_\_\_.  
**1111**

**Question No:83** (Marks:1) **Vu-Topper RM**  
Select the mode of programming in which GAL16V8 can be programmed:

**All of the given**

Simple Mode  
Complex Mode  
Registered Mode

**Question No:84** (Marks:1) **Vu-Topper RM**  
Consider the sum of weight method for converting decimal into binary value, \_\_\_\_\_ is the highest weight for 411.

**256**

257

**Question No:85** (Marks:1) **Vu-Topper RM**  
If two numbers in BCD representation generate an invalid BCD number then the binary \_\_\_\_\_ is added to the result.

**1001**

1000

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:86** (Marks:1) **Vu-Topper RM**

GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a \_\_\_\_\_ with a \_\_\_\_\_.

**Column, row Page191**

- column, row
- column, column
- row, row

**Question No:87** (Marks:1) **Vu-Topper RM**

The Transition table is very similar to the \_\_\_\_\_ table.

**State Page382**

- Truth
- State
- Transition
- None of the given

**Question No:88** (Marks:1) **Vu-Topper RM**

Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using \_\_\_\_\_.

**Shift Registers Page417**

- Circular Buffers
- Ring Buffers
- Reduce Registers

**Question No:89** (Marks:1) **Vu-Topper RM**

For a down counter that counts from (111 to 000), if current state is "101" the next state will be \_\_\_\_\_.

**110**

- 101
- 100
- 001

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:90**

**(Marks:1)**

**Vu-Topper RM**

The NOR logic gate is the same as the operation of the \_\_\_\_\_ gate with an inverter connected to the output.

**NAND**

AND

OR

NOT

**Question No:91**

**(Marks:1)**

**Vu-Topper RM**

The ROM used by a computer is relatively \_\_\_\_\_ as it stores few bytes of code used to Boot the Computer system on power up.

**Small Page423**

Heavy

High

Normal

**Question No:92**

**(Marks:1)**

**Vu-Topper RM**

Cin is part of \_\_\_\_\_ Adder.

**Full**

Half

Single

Double

**Question No:93**

**(Marks:1)**

**Vu-Topper RM**

Which one flip-flop has an invalid output state?

**SR**

T

JK

D

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:94**

**(Marks:1)**

**Vu-Topper RM**

The maximum value, represented by a single hexadecimal digit is \_\_\_\_.

**"F"**

"E"

"G"

"H"

**Question No:95**

**(Marks:1)**

**Vu-Topper RM**

As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack \_\_\_\_.

**Top Page422**

Bottom

Down

Vertex

**Question No:96**

**(Marks:1)**

**Vu-Topper RM**

8-bit parallel data can be converted into serial data by using \_\_\_\_\_ multiplexer.

**8-to-1 Page175**

8-to-0

0-to-8

1-to-0

**Question No:97**

**(Marks:1)**

**Vu-Topper RM**

Adding two octal numbers "36" and "71" result in \_\_\_\_\_.

**127**

213

123

345

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:98** (Marks:1) **Vu-Topper RM**

The Static Ram (SRAM) is non-volatile and is not a \_\_\_\_\_ density memory as a latch is required to store a single bit of information.

**High Page417**

Low

Medium

Hot

**Question No:99** (Marks:1) **Vu-Topper RM**

In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.

**True**

False

**Question No:100** (Marks:1) **Vu-Topper RM**

Demorgan's two theorems prove the equivalency of the NAND and \_\_\_\_\_ gates and the NOR and \_\_\_\_\_ gates respectively.

**Negative-OR, Negative-AND Page74**

**Question No:101** (Marks:1) **Vu-Topper RM**

A multiplexer with a register circuit converts

**Parallel data to serial Page356**

Serial data to parallel

Serial data to serial

Parallel data to parallel

**Question No:102** (Marks:1) **Vu-Topper RM**

Implementation of Latch is required almost \_\_\_\_\_ transistor.

**Six Page417**

Two

Three

Four

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:103** (Marks:1) **Vu-Topper RM**

The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to \_\_\_\_\_ location(s) using a single address.

One

Two

Three

**Four Page399**

**Question No:104** (Marks:1) **Vu-Topper RM**

Consider A=1, B=0, C=1. A, B and C represent the input of three-bit NAND gate, the output of the NAND gate will be \_\_\_\_\_.

**One Page46**

**Question No:105** (Marks:1) **Vu-Topper RM**

The 74HC163 is a 4-bit Synchronous counter, it has \_\_\_\_\_ data output pins.

**4 Page278**

**Question No:106** (Marks:1) **Vu-Topper RM**

The \_\_\_\_\_ input overrides the \_\_\_\_\_ input.

**Asynchronous, synchronous Page369**

Synchronous, asynchronous

Preset input (PRE), Clear input (CLR)

Clear input (CLR), Preset input (PRE)

**Question No:107** (Marks:1) **Vu-Topper RM**

The Test Vector definition defines the test vectors for all the three counter inputs and \_\_\_\_\_ counter output/outputs.

**Three Page362**

Four

Five

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:108** (Marks:1) **Vu-Topper RM**

Subtractors also have output to check if 1 has been \_\_\_\_\_.

**Primed**

Shifted

Complemented

Borrowed

**Question No:109** (Marks:1) **Vu-Topper RM**

An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting \_\_\_\_\_.

**Q output of all flip-flops to clock input of next flip-flops**

**Question No:110** (Marks:1) **Vu-Topper RM**

For a Standard SOP expression, a \_\_\_\_\_ is placed in the cell corresponding to the product term (Minter) present in the expression.

**1 Page90**

**Question No:111** (Marks:1) **Vu-Topper RM**

Two signals \_\_\_\_\_ and \_\_\_\_\_ provide the timing inputs to the State Machine.

**LTIME and STIME Page374**

NSSR and EWSR

LTIME and STIME

PTIME and QTIM

**Question No:112** (Marks:1) **Vu-Topper RM**

Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration  $t_{WD}$ ?

**WE Page397**

CS

OE

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:113** (Marks:1) **Vu-Topper RM**  
Implementation of the FIFO buffer in \_\_\_\_\_ is usually takes the form of a circular buffer.  
**RAM Page420**

**Question No:114** (Marks:1) **Vu-Topper RM**  
The output of a NAND gate is \_\_\_\_\_ when all the inputs are one.  
**Zero Page47**

One  
Available  
Not available

**Question No:115** (Marks:1) **Vu-Topper RM**  
Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires \_\_\_\_\_ gates for the 8 product terms (minters) with an 8-input OR gate.  
**8 AND**  
**8 OR**

**Question No:116** (Marks:1) **Vu-Topper RM**  
WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO -----  
**THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED**

**Question No:117** (Marks:1) **Vu-Topper RM**  
The \_\_\_\_\_ Encoder is used as a keypad encoder.  
**Decimal-to-BCD Priority Page166**

**Question No:118** (Marks:1) **Vu-Topper RM**  
3-to-8 decoder can be used to implement Standard SOP and POS Boolean expressions  
**True Page161**  
False

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:119** (Marks:1)  
NOR gate is formed by connecting \_\_\_\_\_

**Vu-Topper RM**

**OR Gate and then NOT Gate Page47**

**Question No:120** (Marks:1)

**Vu-Topper RM**

A particular half adder has

**2 INPUTS AND 2 OUTPUT Page134**

**Question No:121** (Marks:1)

**Vu-Topper RM**

Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause the output to .

**Toggle**

**Question No:122** (Marks:1)

**Vu-Topper RM**

A stage in the shift register consists of

**A flip flop**

**Question No:123** (Marks:1)

**Vu-Topper RM**

If a circuit suffers “Clock Skew” problem, the output of circuit can’t be guaranteed.

**True**

False

**Question No:124** (Marks:1)

**Vu-Topper RM**

In Master-Slave flip-flop the clock signal is connected to slave flip-flop using gate.

**NOT**

OR

AND

**Question No:125** (Marks:1)

**Vu-Topper RM**

flip-flops are obsolete now.

**Master-Slave**

**For More Help Vu- Topper RM Contact What’s app 03224021365**

**Question No:126**

**(Marks:1)**

**Vu-Topper RM**

For a gated D-Latch if  $EN=1$  and  $D=1$  then  $Q(t+1)=$

**1**

0

**Question No:127**

**(Marks:1)**

**Vu-Topper RM**

In Master-Slave flip-flop setup, the master flip-flop operators at

**Both Master-Slave operator simultaneously Page230**

**Question No:128**

**(Marks:1)**

**Vu-Topper RM**

The power consumed by a flip-flop is defined by \_

**$P = V_{cc} \times I_{cc}$  Page235**

$P = I_{cc} \times R_{cc}$

$P = V_{cc} \times R_{cc}$

$P = M_{cc} \times V_{cc}$

**Question No:129**

**(Marks:1)**

**Vu-Topper RM**

The 3-bit up counter can be implemented using flip-flop(s).

**S-R flip-flops and D-flip-flops Page316**

**Question No:130**

**(Marks:1)**

**Vu-Topper RM**

The terminal count of a 4-bit binary counter in the DOWN mode is

**0000**

0011

**Question No:131**

**(Marks:1)**

**Vu-Topper RM**

The low to high or high to low transition of the clock is considered to be a(n) \_\_\_\_\_

**Edge Page228**

Add

Odd

Out

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:132 (Marks:1)**

**Vu-Topper RM**

A transparent mode means \_\_\_\_\_

**The changes in the data at the inputs of the latch are seen at the output**

**Page245**

**Question No:133 (Marks:1)**

**Vu-Topper RM**

In \_\_\_\_\_ outputs depend only on the current state.

**Moore Machine Page332**

**Question No:134 (Marks:1)**

**Vu-Topper RM**

Smallest unit of binary data is a \_\_\_\_\_

**Bit Page387**

**Question No:135 (Marks:1)**

**Vu-Topper RM**

Which mechanisms allocate the binary values to the states in order to reduce the cost of the combinational circuits?

**State assignment**

**Question No:136 (Marks:1)**

**Vu-Topper RM**

State of flip-flop can be switched by changing its

**Input signal**

**Question No:137 (Marks:1)**

**Vu-Topper RM**

Design of state diagram is one of many steps used to design

**A truncated counter**

**Question No:138 (Marks:1)**

**Vu-Topper RM**

Flip flops are also called \_\_\_\_\_.

**Bi-stable multivibrators Page228**

Bi-stable singlevibrators

Bi-stable dualvibrators

Bi-stable transformer

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:139** (Marks:1) **Vu-Topper RM**

The term hold always means.

**No change**

**Question No:140** (Marks:1) **Vu-Topper RM**

A flip-flop is presently in SET state and must remain SET on the next clock pulse. What must j and k be?

**J=X(Don'tcare),K=0**

**Question No:141** (Marks:1) **Vu-Topper RM**

To parallel load a byte of data into a shift register, there must be

**One clock pulse**

**Question No:142** (Marks:1) **Vu-Topper RM**

Invalid state of NOR based SR latch occurs when \_\_\_\_\_.

**S=1, R=1**

**Question No:143** (Marks:1) **Vu-Topper RM**

74HC163 has two enable input pins which are \_\_\_\_\_ and \_\_\_\_\_

**ENP, ENT**

**Question No:144** (Marks:1) **Vu-Topper RM**

\_\_\_\_\_ is said to occur when multiple internal variables change due to change in one input variable

**Race condition Page267**

**Question No:145** (Marks:1) **Vu-Topper RM**

In asynchronous transmission when the transmission line is idle, \_\_\_\_

**It is set to logic high Page356**

**Question No:146** (Marks:1) **Vu-Topper RM**

LUT is acronym for \_\_\_\_\_

**Look Up Table Page439**

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:147** (Marks:1) **Vu-Topper RM**  
The three fundamental gates are \_\_\_\_\_  
**NOT, OR, AND Page40**

**Question No:148** (Marks:1) **Vu-Topper RM**  
The total amount of memory that is supported by any digital system depends upon \_\_\_\_\_  
**The size of the address bus of the microprocessor Page430**

**Question No:149** (Marks:1) **Vu-Topper RM**  
Stack is an acronym for \_\_\_\_\_  
**LIFO memory Page429**

**Question No:150** (Marks:1) **Vu-Topper RM**  
In order to synchronize two devices that consume and produce data at different rates, we can use \_\_\_\_\_  
**Fist In First Out Memory Page425**

**Question No:151** (Marks:1) **Vu-Topper RM**  
A flip-flop changes its state when \_\_\_\_\_  
**Low-to-high transition of clock Page228**

**Question No:152** (Marks:1) **Vu-Topper RM**  
In a sequential circuit the next state is determined by \_\_\_\_\_ and \_\_\_\_\_  
**Input and clock signal applied Page305**

**Question No:153** (Marks:1) **Vu-Topper RM**  
\_\_\_\_\_ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.  
**Accuracy Page460**

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:154** (Marks:1)

**Vu-Topper RM**

Above is the circuit diagram of \_\_\_\_\_.

**Asynchronous up-counter Page270**

**Question No:155** (Marks:1)

**Vu-Topper RM**

The sequence of states that are implemented by a n-bit Johnson counter is

**2n (n multiplied by 2) Page354**

**Question No:156** (Marks:1)

**Vu-Topper RM**

"A + B = B + A" is \_\_\_\_\_

**Commutative Law**

**Question No:157** (Marks:1)

**Vu-Topper RM**

Following is standard POS expression

**True**

False

**Question No:158** (Marks:1)

**Vu-Topper RM**

An alternate method of implementing Comparators which allows the Comparators to be easily cascaded without the need for extra logic gates is \_\_\_\_\_

**Using Iterative Circuit based Comparators Page155**

**Question No:159** (Marks:1)

**Vu-Topper RM**

DE multiplexer is also called

**Data distributor Page178**

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:160** (Marks:1) **Vu-Topper RM**

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

**25 mW Page242**

10 mW

64 mW

1024 mW

**Question No:161** (Marks:1) **Vu-Topper RM**

In a state diagram, the transition from a current state to the next state is determined by

**Current state and the inputs Page332**

**Question No:162** (Marks:1) **Vu-Topper RM**

The alternate solution for a demultiplexer-register combination circuit is

**Serial in / Parallel out shift register Page356**

**Question No:163** (Marks:1) **Vu-Topper RM**

The 4-bit 2's complement representation of "+5" is \_\_\_\_\_

**0101**

**Question No:164** (Marks:1) **Vu-Topper RM**

The storage cell in SRAM is

**A capacitor Page407**

**Question No:165** (Marks:1) **Vu-Topper RM**

What is the difference between a D latch and a D flip-flop?

**The D flip-flop has a clock input.**

**Question No:166** (Marks:1) **Vu-Topper RM**

The OR gate performs Boolean \_\_\_\_\_.

**addition Page42**

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:167** (Marks:1) **Vu-Topper RM**  
In \_\_\_\_\_ Q output of the last flip-flop of the shift register is connected to the data input of the first flipflop of the shift register.  
**Ring counter Page355**

**Question No:168** (Marks:1) **Vu-Topper RM**  
The \_\_\_\_\_ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines  
**Access Time Page417**

**Question No:169** (Marks:1) **Vu-Topper RM**  
The design and implementation of synchronous counters start from \_\_\_\_.  
**State diagram Page319**

**Question No:170** (Marks:1) **Vu-Topper RM**  
THE HOURS COUNTER IS IMPLEMENTED USING \_\_\_\_\_  
**A SINGLE DECADE COUNTER AND A FLIP-FLOP**

**Question No:171** (Marks:1) **Vu-Topper RM**  
The high density FLASH memory cell is implemented using \_\_\_\_\_  
**1 floating-gate MOS transistor Page419**

**Question No:172** (Marks:1) **Vu-Topper RM**  
Q2 :=Q1 OR X OR Q3 The above ABEL expression will be  
**Q2:= Q1 # X # Q3 Page210**

**Question No:173** (Marks:1) **Vu-Topper RM**  
When the control line in tri-state buffer is high the buffer operates like a \_\_\_\_\_ gate  
**NOT Page196**

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:174** (Marks:1) **Vu-Topper RM**  
The output of an AND gate is one when \_\_\_\_\_  
**All of the inputs are one Page40**

**Question No:175** (Marks:1) **Vu-Topper RM**  
The binary numbers  $A = 1100$  and  $B = 1001$  are applied to the inputs of a comparator. What are the output levels?  
 **$A > B = 1, A < B = 0, A = B = 0$  Page109**

**Question No:176** (Marks:1) **Vu-Topper RM**  
The diagram above shows the general implementation of \_\_\_\_\_ form  
**POS Page122**

**Question No:177** (Marks:1) **Vu-Topper RM**  
The device shown here is most likely a  
**Multiplexer**

**Question No:178** (Marks:1) **Vu-Topper RM**  
DE multiplexer converts \_\_\_\_\_ data to \_\_\_\_\_ data  
**Serial data, parallel data Page356**

**Question No:179** (Marks:1) **Vu-Topper RM**  
The capability that allows the PLDs to be programmed after they have been installed on a circuit board is called \_\_\_\_\_  
**In-System Programming (ISP) Page194**

**Question No:180** (Marks:1) **Vu-Topper RM**  
Following Is the circuit diagram of mono-stable device which gate will be replaced by the red colored rectangle in the circuit.  
**XNOR Page262**

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:181** (Marks:1) **Vu-Topper RM**

In \_\_\_\_\_ outputs depend only on the combination of current state and inputs.

**Mealy machine Page332**

**Question No:182** (Marks:1) **Vu-Topper RM**

In the following statement Z PIN 20 ISTYPE „reg.invert“;

**Active-low Registered Mode output**

**Question No:183** (Marks:1) **Vu-Topper RM**

A Nibble consists of \_\_\_\_\_ bits

**4 Page394**

**Question No:184** (Marks:1) **Vu-Topper RM**

The process of converting the analogue signal into a digital representation (code) is known as \_\_\_\_\_

**Quantization Page445**

**Question No:185** (Marks:1) **Vu-Topper RM**

If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a \_\_\_\_\_.

0

**1 Page417**

**Question No:186** (Marks:1) **Vu-Topper RM**

A 4- bit UP/DOWN counter is in DOWN mode and in the 1010 state. on the next clock pulse, to what state does the counter go?

**1001**

1011

0011

1100

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:187**

**(Marks:1)**

**Vu-Topper RM**

A standard interface for programming the In-System PLD consists of  
2 wire,

**4 wire 194**

8 wire,

16 wire

**Question No:188**

**(Marks:1)**

**Vu-Topper RM**

In designing any synchronous counter a modulus number is used which  
determine the number of..... used in a counter.....

Registers

**Flip Flops**

Counters

Latches

**Question No:189**

**(Marks:1)**

**Vu-Topper RM**

A positive edge-triggered flip-flop changes its state when \_.

Enable input (EN) is set

Preset input (PRE) is set

**Low-to-high transition of clock**

High-to-low transition of clock

**Question No:190**

**(Marks:1)**

**Vu-Topper RM**

The asynchronous inputs are normally labeled \_\_\_\_\_ and \_\_\_\_\_,  
and are normally active \_\_\_\_\_ inputs.

**PRE, CLR, LOW**

ON, OFF, HIGH

START, STOP, LOW

SET, RESET, HIGH

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:191** (Marks:1) **Vu-Topper RM**

Assume a J-K flip-flop has 1s on the J and K inputs. The next clock pulse will cause the output to \_\_\_\_\_.

set

reset

latch

**Toggle**

**Question No:192** (Marks:1) **Vu-Topper RM**

In synchronous systems, the exact times at which any output can change state are determined by a signal commonly called the \_\_\_\_\_.

traffic

D

flip-flop

**Clock**

**Question No:193** (Marks:1) **Vu-Topper RM**

Which is not an example of a truncated modulus?

**8**

9

11

15

**Question No:194** (Marks:1) **Vu-Topper RM**

Bi-stable devices remain in either of their \_\_\_\_\_ states unless the inputs force the device to switch its state Select correct option:

Ten

Eight

Three

**Two Page255**

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:195** (Marks:1) **Vu-Topper RM**

In Synchronous systems, the output of all the digital circuits changes when an enable signal is applied instead of the clock signal.

Select correct option:

True

**False Page228**

**Question No:196** (Marks:1) **Vu-Topper RM**

\_\_\_\_\_ flip-flops are obsolete now.

Select correct option:

Edge-triggered

**Master-Slave Page257**

T-Flipflop

D-Flipflop

**Question No:197** (Marks:1) **Vu-Topper RM**

A mono-stable device only has a single stable state-----

**True Page262**

False

**Question No:198** (Marks:1) **Vu-Topper RM**

If the S and R inputs of the gated S-R latch are connected together using a \_\_\_\_\_ gate then there is only a single input to the latch. The input is represented by D instead of S or R (A gated D-Latch)

Select correct option:

AND

OR

**NOT Page226**

XOR

**For More Help Vu- Topper RM Contact What's app 03224021365**

**Question No:199**

**(Marks:1)**

**Vu-Topper RM**

When an eight bit serial in/serial out shift register is used for a 24 micro seconds time delay, the clock frequenct must be Select correct option:

41.67 KHz

**333 KHz**

125 KHz

8 MHz

**Question No:200**

**(Marks:1)**

**Vu-Topper RM**

A modulus-14 counter has fourteen states requiring\_\_\_\_\_

**14 Flip Flops**

14 Registers

4 Flip Flops

4 Registers

**Question No:201**

**(Marks:1)**

**Vu-Topper RM**

Karnaugh map is used in designing Select correct option:

a clock

a counter

an UP/DOWN counter

**All of the above**

***Free Of Cost All Study Helping Material Is Available.!***

***>>> Provide By Vu-Toper Team <<<***

***Contact On What's app #03224021365***