FINALTERM EXAMINATION
Spring 2010
CS302- Digital Logic Design

Time: 90 min
Marks: 58

Question No: 1 (Marks: 1) - Please choose one

A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

- ► 1
- ► 2
- ► 4
- ► 8

Question No: 2 (Marks: 1) - Please choose one

A frequency counter _____

- ► Counts pulse width
- ► Counts no. of clock pulses in 1 second
- ► Counts high and low range of given clock pulse
- ► None of given options

Question No: 3 (Marks: 1) - Please choose one

In a sequential circuit the next state is determined by _____ and _____

- ► State variable, current state
- ► Current state, flip-flop output
- ► Current state and external input
- ► Input and clock signal applied

Question No: 4 (Marks: 1) - Please choose one

The divide-by-60 counter in digital clock is implemented by using two cascading counters:

- ► Mod-6, Mod-10
- ► Mod-50, Mod-10
- ► Mod-10, Mod-50
- ► Mod-50, Mod-6

Question No: 5 (Marks: 1) - Please choose one

In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

- ► True
- ► False

Question No: 6 (Marks: 1) - Please choose one

Flip flops are also called _____

- ► Bi-stable dualvibrators
- ► Bi-stable transformer
- ► Bi-stable multivibrators
- ► Bi-stable singlevibrators

Question No: 7 (Marks: 1) - Please choose one

The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

- ► Set-up time
- ► Hold time
- ► Pulse Interval time
- ► Pulse Stability time (PST)

Question No: 8 (Marks: 1) - Please choose one

74HC163 has two enable input pins which are _____ and _____

- ► ENP, ENT
- ► ENI, ENC
- ► ENP, ENC
- ► ENT, ENI

Question No: 9 (Marks: 1) - Please choose one

_____ is said to occur when multiple internal variables change due to change in one input variable

- ► Clock Skew
- ► Race condition
- ► Hold delay
- ► Hold and Wait

Question No: 10 (Marks: 1) - Please choose one

Given the state diagram of an up/down counter, we can find _____

- ► The next state of a given present state
- ► The previous state of a given present state
- ► Both the next and previous states of a given state
- ► The state diagram shows only the inputs/outputs of a given states

Question No: 11 (Marks: 1) - Please choose one

The _____ input overrides the _____ input

- ► Asynchronous, synchronous
- ► Synchronous, asynchronous
- ► Preset input (PRE), Clear input (CLR)
- ► Clear input (CLR), Preset input (PRE)

Question No: 12 (Marks: 1) - Please choose one

A logic circuit with an output $X = \overline{A}BC + A\overline{B}$ consists of _____.

- ► two AND gates, two OR gates, two inverters
- ► three AND gates, two OR gates, one inverter
- ► two AND gates, one OR gate, two inverters
- ► two AND gates, one OR gate

Question No: 13 (Marks: 1) - Please choose one

A decade counter is _____.

- ► Mod-3 counter
- ► Mod-5 counter
- ► Mod-8 counter

► Mod-10 counter

Question No: 14 (Marks: 1) - Please choose one

In asynchronous transmission when the transmission line is idle, _____

► It is set to logic low
► It is set to logic high
► Remains in previous state
► State of transmission line is not used to start transmission

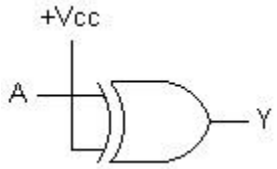
Question No: 15 (Marks: 1) - Please choose one

A Nibble consists of _____ bits

► 2
► 4
► 8
► 16

Question No: 16 (Marks: 1) - Please choose one

The output of this circuit is always _____.



► 1
► 0
► A
► $\overline{A}$

Question No: 17 (Marks: 1) - Please choose one

Excess-8 code assigns _____ to "-8"

► 1110
► 1100
► 1000
► 0000

Question No: 18 (Marks: 1) - Please choose one

The voltage gain of the Inverting Amplifier is given by the relation _____

► $V_{out} / V_{in} = - R_f / R_i$
► $V_{out} / R_f = - V_{in} / R_i$
► $R_f / V_{in} = - R_i / V_{out}$
► $R_f / V_{in} = R_i / V_{out}$

Question No: 19 (Marks: 1) - Please choose one

LUT is acronym for _____

► Look Up Table
► Local User Terminal
► Least Upper Time Period
► None of given options

Question No: 20 (Marks: 1) - Please choose one

DRAM stands for _____

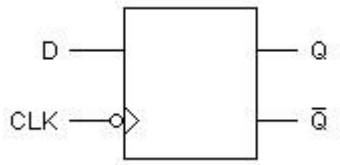
- ▶ Dynamic RAM
- ▶ Data RAM
- ▶ Demoduler RAM
- ▶ None of given options

Question No: 21 (Marks: 1) - Please choose one

The three fundamental gates are _____

- ▶ AND, NAND, XOR
- ▶ OR, AND, NAND
- ▶ NOT, NOR, XOR
- ▶ NOT, OR, AND

Question No: 22 (Marks: 1) - Please choose one



Which of the following statement is true regarding above block diagram ?

- ▶ Triggering takes place on the negative-going edge of the CLK pulse
- ▶ Triggering takes place on the positive-going edge of the CLK pulse
- ▶ Triggering can take place anytime during the HIGH level of the CLK waveform
- ▶ Triggering can take place anytime during the LOW level of the CLK waveform

Question No: 23 (Marks: 1) - Please choose one

The total amount of memory that is supported by any digital system depends upon _____

- ▶ The organization of memory
- ▶ The structure of memory
- ▶ The size of decoding unit
- ▶ The size of the address bus of the microprocessor

Question No: 24 (Marks: 1) - Please choose one

The expression F=A+B+C describes the operation of three bits _____ Gate.

- ▶ OR
- ▶ AND
- ▶ NOT
- ▶ NAND

Question No: 25 (Marks: 1) - Please choose one

Stack is an acronym for_____

- ▶ FIFO memory
- ▶ LIFO memory
- ▶ Flash Memory
- ▶ Bust Flash Memory

Question No: 26 (Marks: 1) - Please choose one

Addition of two octal numbers “36” and “71” results in _____

► 213
► 123
► 127
► 345

Question No: 27 (Marks: 2)
Define quantization process.

Question No: 28 (Marks: 2)

Explain the difference between 1-to-4 Demultiplexer and 2-to-4 Binary Decoder?

Question No: 29 (Marks: 2)

A general Sequential circuit consists of a combinational circuit and a memory element. How this memory element is implemented

Question No: 30 (Marks: 2)

Suppose a 2 bit up-counter, having states "A, B, C, D". Write down GOTO statements to show how present states change to next states.

Question No: 31 (Marks: 3)

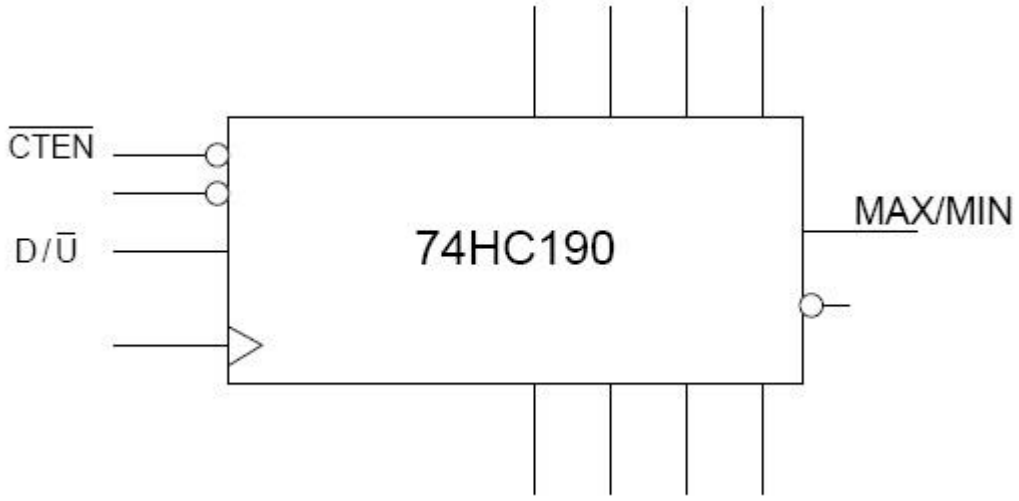
Name three Operations that can be performed on FLASH Memory

Question No: 32 (Marks: 3)

Explain Rotate Right Operation of shift register with the help of diagram.

Question No: 33 (Marks: 3)

You are given the block diagram of 74HC190 integrated circuit up/down counter, explain the function of labeled inputs/outputs.



Question No: 34 (Marks: 5)

Draw the state diagram of 3-bit up-down counter, use an external input X, when X sets to logic 1, the counter counts downwards, otherwise upward.

Question No: 35 (Marks: 5)

Differentiate between synchronous and asynchronous RAM.

Question No: 36 (Marks: 5)

Explain Memory Select or Enable Signals

FINALTERM EXAMINATION
Spring 2010
CS302- Digital Logic Design (Session - 4)

Time: 90 min
Marks: 58

Question No: 1 (Marks: 1) - Please choose one
The ANSI/IEEE Standard 754 defines a _____Single-Precision Floating Point format for binary numbers.

- 8-bit
- 16-bit
- **32-bit**
- 64-bit

Question No: 2 (Marks: 1) - Please choose one
The decimal "17" in BCD will be represented as _____

- 11101
- 11011
- **10111**
- 11110

Question No: 3 (Marks: 1) - Please choose one
The basic building block for a logical circuit is _____

- A Flip-Flop
- **A Logical Gate**
- An Adder
- None of given options

Question No: 4 (Marks: 1) - Please choose one
The output of the expression F=A.B.C will be Logic _____ when A=1, B=0, C=1.

- Undefined
- One
- **Zero**
- No Output as input is invalid.

Question No: 5 (Marks: 1) - Please choose one
_____ is invalid number of cells in a single group formed by the adjacent cells in K-map

- 2
- 8
- **12**
- 16

Question No: 6 (Marks: 1) - Please choose one
The PROM consists of a fixed non-programmable _____ Gate array configured as a decoder.

- **AND**

► OR
► NOT
► XOR

Question No: 7 (Marks: 1) - Please choose one

_____ is one of the examples of synchronous inputs.

► **J-K input**
► EN input
► Preset input (PRE)
► Clear Input (CLR)

Question No: 8 (Marks: 1) - Please choose one

_____ is one of the examples of asynchronous inputs.

► J-K input
► S-R input
► **D input**
► Clear Input (CLR)

Question No: 9 (Marks: 1) - Please choose one

The _____ input overrides the _____ input

► **Asynchronous, synchronous**
► Synchronous, asynchronous
► Preset input (PRE), Clear input (CLR)
► Clear input (CLR), Preset input (PRE)

Question No: 10 (Marks: 1) - Please choose one

_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.

► Race condition
► **Clock Skew**
► Ripple Effect
► None of given options

Question No: 11 (Marks: 1) - Please choose one

Consider an up/down counter that counts between 0 and 15, if external input(X) is "0" the counter counts upward (0000 to 1111) and if external input (X) is "1" the counter counts downward (1111 to 0000), now suppose that the present state is "1100" and X=1, the next state of the counter will be _____

► 0000
► **1101**
► 1011
► 1111

Question No: 12 (Marks: 1) - Please choose one

In a state diagram, the transition from a current state to the next state is determined by

► **Current state and the inputs**
► Current state and outputs
► Previous state and inputs
► Previous state and outputs

Question No: 13 (Marks: 1) - Please choose one

_____ is used to minimize the possible no. of states of a circuit.

► **State assignment**
► State reduction
► Next state table
► State diagram

Question No: 14 (Marks: 1) - Please choose one

_____ is used to simplify the circuit that determines the next state.

► **State diagram**
► Next state table
► State reduction
► State assignment

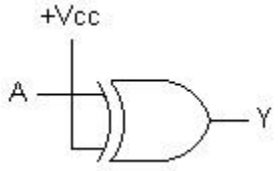
Question No: 15 (Marks: 1) - Please choose one

The best state assignment tends to _____.

► Maximizes the number of state variables that don't change in a group of related states
► **Minimizes the number of state variables that don't change in a group of related states**
► Minimize the equivalent states
► None of given options

Question No: 16 (Marks: 1) - Please choose one

The output of this circuit is always _____.



► **1**
► 0
► A
►

Question No: 17 (Marks: 1) - Please choose one

A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

► 1
► 2
► 4
► **8**

Question No: 18 (Marks: 1) - Please choose one

5-bit Johnson counter sequences through ____ states

► 7
► 10
► 32
► **25**

Question No: 19 (Marks: 1) - Please choose one

Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)

- 1100
- 0011
- **0000**
- 1111

Question No: 20 (Marks: 1) - Please choose one

The address from which the data is read, is provided by _____

- Depends on circuitry
- None of given options
- RAM
- **Microprocessor**

Question No: 21 (Marks: 1) - Please choose one

FIFO is an acronym for _____

- **First In, First Out**
- Fly in, Fly Out
- Fast in, Fast Out
- None of given options

Question No: 22 (Marks: 1) - Please choose one

LUT is acronym for _____

- **Look Up Table**
- Local User Terminal
- Least Upper Time Period
- None of given options

Question No: 23 (Marks: 1) - Please choose one

The voltage gain of the Inverting Amplifier is given by the relation _____

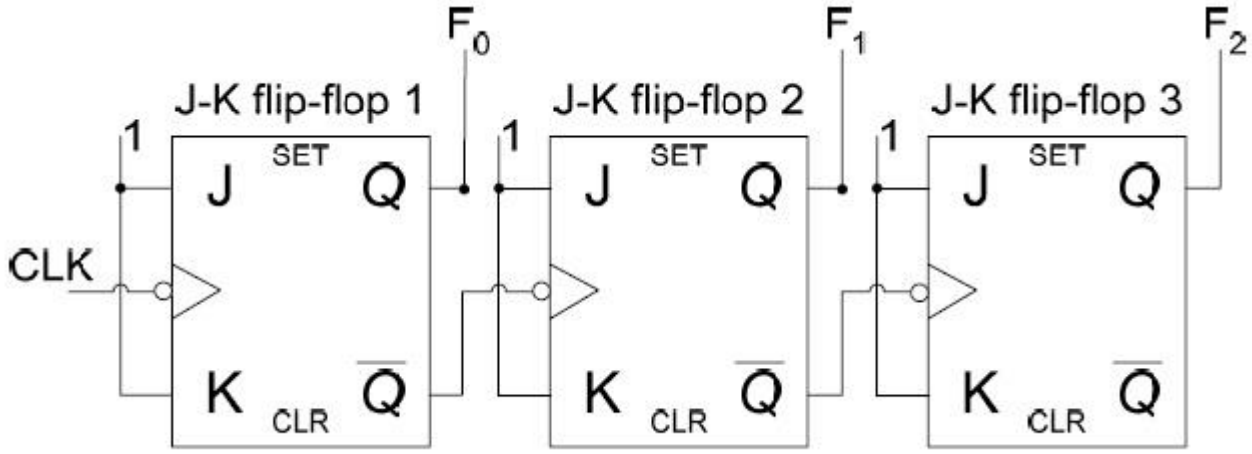
- **$V_{out} / V_{in} = - R_f / R_i$**
- $V_{out} / R_f = - V_{in} / R_i$
- $R_f / V_{in} = - R_i / V_{out}$
- $R_f / V_{in} = R_i / V_{out}$

Question No: 24 (Marks: 1) - Please choose one

_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

- Resolution
- **Accuracy**
- Quantization
- Missing Code

Question No: 25 (Marks: 1) - Please choose one



Above is the circuit diagram of _____.

- Asynchronous up-counter
- Asynchronous down-counter
- **Synchronous up-counter**
- Synchronous down-counter

Question No: 26 (Marks: 1) - Please choose one

The sequence of states that are implemented by a n-bit Johnson counter is

- n+2 (n plus 2)
- **2n (n multiplied by 2)**
- 2^n (2 raise to power n)
- n^2 (n raise to power 2)

Question No: 27 (Marks: 2)

Draw the Truth-Table of NOR based S-R Latch

input		output
S	**R**	**Q_{T+1}**
0	**0**	**Q_T**
0	**1**	**0**
1	**0**	**1**
1	**1**	**INVALID**

Question No: 28 (Marks: 2)

Two state assignments are given in the table below. Identify which state assignment is best and why?

States	State assignment 1	State assignment 2
A	**00**	**00**

B	**01**	**01**
C	**11**	**10**
D	**10**	**11**

Ans:
State assignment 2 is best assignment… it Minimizes the number of state variables that don't change in a group of related states

. **Question No: 29 (Marks: 2)**

Write down at least two functions of a register.

Ans:

1. **Registers are operating as a coherent unit to hold and generate data.**
2. **registers functions also include configuration and start-up of certain features, especially during initialization, bufferstorage e.g. video memory for graphics cards, input/output (I/O) of different kinds,**

Question No: 30 (Marks: 2)

Define quantization process.

Ans:
The process by which we can convert an analogue signal into digital signal (code) is known as quantization process.

Question No: 31 (Marks: 3)

How can we calculate the frequency of an unknown signal?

Ans:
The frequency of a particular event is accomplished by counting the number of times that event occurs within a specific time interval, then dividing the count by the length of the time interval.

Question No: 32 (Marks: 3)

Given the following statement used in PLD programming:
Y PIN 23 ISTYPE 'com';
Explain what does this statement mean?

Ans:
The Y variable is a 'Combinational' output available directly from the AND-OR gate array output. The active-low or active-high output of the Registered Mode can also be

specified in the declaration statement

Question No: 33 (Marks: 3)

Explain dynamic RAM in your own words.

Ans:

Dram use latch to store a single bit of information. The main drawback of it id the discharge of capacitor over a period of time. Here four gates are used in making a single latch. In terms of transistors, 4 to 6 transistors are required to implement a single storage cell. In order to build memories with higher densities, a single transistor is used to store a binary value. A single transistor can not store a binary value however it is used to charge and discharge a capacitor. The capacitor can not retain the charge, therefore it has to be periodically charged

Through a refresh cycle.

Question No: 34 (Marks: 5)

You are given the Next-state table of a moor machine, using this information draw the state diagram of the machine.

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	1	1	1	1	1
1	1	1	0	0	1
0	0	1	0	1	0
0	1	0	1	0	0
1	0	0	1	1	0
1	1	0	0	1	1

Question No: 35 (Marks: 5)

Explain Memory Select or Enable Signals

Memory Select or Enable Signal:

There are more than one memory chips to store program

Information in daily use computers. read or write operation is carried out on a single addressable location instantaneously .

The unique location is accessed in one of the several memory chips, so single memory chips is selected before a read or write operation can be carried out. All memory chips have a chip enable or chip select signal which has to be activated before the memory can be accessed.

Question No: 36 (Marks: 5)

Performance characteristics of D/A converters are determined by five parameters. Name them.

Ans:

Performances characteristics of D/A converters are determined by five parameters

are as follow:

1. **Accuracy**
2. **Setting time**
3. **Monotonicity**
4. **Linearity**
5. **Resolution**

FINALTERM EXAMINATION
Spring 2010
CS302- Digital Logic Design (Session - 1)

Time: 90 min
arks: 58

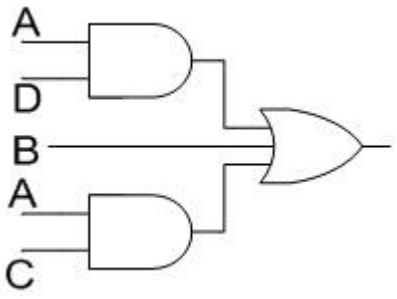
Question No: 1 (Marks: 1) - Please choose one

"A + B = B + A" is _____

- ► Demorgan's Law
- ► Distributive Law
- ► Commutative Law
- ► Associative Law

Question No: 2 (Marks: 1) - Please choose one

The diagram given below represents _____



- ► Demorgans law
- ► Associative law
- ► Product of sum form
- ► Sum of product form

Question No: 3 (Marks: 1) - Please choose one

Following is standard POS expression

$(A+\bar{B}+C+\bar{D})(A+\bar{B}+C+D)(A+B+\bar{C}+\bar{D})(A+B+C+\bar{D})(A+\bar{B}+\bar{C}+D)$

- ► True
- ► False

Question No: 4 (Marks: 1) - Please choose one

An alternate method of implementing Comparators which allows the Comparators to be easily cascaded without the need for extra logic gates is _____

- ► Using a single comparator
- ► Using Iterative Circuit based Comparators
- ► Connecting comparators in vertical hierarchy
- ► Extra logic gates are always required.

Question No: 5 (Marks: 1) - Please choose one

Demultiplexer is also called

- ► Data selector
- ► Data router
- ► Data distributor
- ► Data encoder

Question No: 6 (Marks: 1) - Please choose one

The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____

- ► Doesn't have an invalid state
- ► Sets to clear when both J = 0 and K = 0
- ► It does not show transition on change in pulse
- ► It does not accept asynchronous inputs

Question No: 7 (Marks: 1) - Please choose one

A positive edge-triggered flip-flop changes its state when _____

- ► Low-to-high transition of clock
- ► High-to-low transition of clock
- ► Enable input (EN) is set
- ► Preset input (PRE) is set

Question No: 8 (Marks: 1) - Please choose one

A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is

- ► 10 mW
- ► 25 mW
- ► 64 mW
- ► 1024

Question No: 9 (Marks: 1) - Please choose one

_____ counters as the name indicates are not triggered simultaneously.

- ► Asynchronous
- ► Synchronous
- ► Positive-Edge triggered
- ► Negative-Edge triggered

Question No: 10 (Marks: 1) - Please choose one

74HC163 has two enable input pins which are _____ and _____

- ► ENP, ENT
- ► ENI, ENC
- ► ENP, ENC
- ► ENT, ENI

Question No: 11 (Marks: 1) - Please choose one

The divide-by-60 counter in digital clock is implemented by using two cascading

counters:

- ► Mod-6, Mod-10
- ► Mod-50, Mod-10
- ► Mod-10, Mod-50
- ► Mod-50, Mod-6

Question No: 12 (Marks: 1) - Please choose one

In a state diagram, the transition from a current state to the next state is determined by

- ► Current state and the inputs
- ► Current state and outputs
- ► Previous state and inputs
- ► Previous state and outputs

Question No: 13 (Marks: 1) - Please choose one

A synchronous decade counter will have _____ flip-flops

- ► 3
- ► 4
- ► 7
- ► 10

Question No: 14 (Marks: 1) - Please choose one

_____ is used to minimize the possible no. of states of a circuit.

- ► State assignment
- ► State reduction
- ► Next state table
- ► State diagram

Question No: 15 (Marks: 1) - Please choose one

A multiplexer with a register circuit converts _____

- ► Serial data to parallel
- ► Parallel data to serial
- ► Serial data to serial
- ► Parallel data to parallel

Question No: 16 (Marks: 1) - Please choose one

The alternate solution for a demultiplexer-register combination circuit is _____

- ► Parallel in / Serial out shift register
- ► Serial in / Parallel out shift register
- ► Parallel in / Parallel out shift register
- ► Serial in / Serial Out shift register

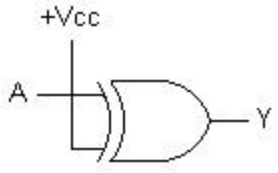
Question No: 17 (Marks: 1) - Please choose one

A GAL is essentially a _____.

- ► Non-reprogrammable PAL
- ► PAL that is programmed only by the manufacturer
- ► Very large PAL
- ► Reprogrammable PAL

Question No: 18 (Marks: 1) - Please choose one

The output of this circuit is always _____.



- 1
- 0
- A
-

Question No: 19 (Marks: 1) - Please choose one
DRAM stands for _____

- **Dynamic RAM**
- **Data RAM**
- **Demoduler RAM**
- **None of given options**

Question No: 20 (Marks: 1) - Please choose one
in _____, all the columns in the same row are either read or written.

- Sequential Access
- MOS Access
- FAST Mode Page Access
- None of given options

Question No: 21 (Marks: 1) - Please choose one
FIFO is an acronym for _____

- First In, First Out
- Fly in, Fly Out
- Fast in, Fast Out
- None of given options

Question No: 22 (Marks: 1) - Please choose one
In order to synchronize two devices that consume and produce data at different rates, we can use _____

- Read Only Memory
- Fist In First Out Memory
- Flash Memory
- Fast Page Access Mode Memory

Question No: 23 (Marks: 1) - Please choose one
A frequency counter _____

- Counts pulse width

- ► Counts no. of clock pulses in 1 second
- ► Counts high and low range of given clock pulse
- ► None of given options

Question No: 24 (Marks: 1) - Please choose one

The sequence of states that are implemented by a n-bit Johnson counter is

- ► n+2 (n plus 2)
- ► 2n (n multiplied by 2)
- ► 2^n (2 raise to power n)
- ► n^2 (n raise to power 2)

Question No: 25 (Marks: 1) - Please choose one

Stack is an acronym for _____

- ► FIFO memory
- ► LIFO memory
- ► Flash Memory
- ► Bust Flash Memory

Question No: 26 (Marks: 1) - Please choose one

The 4-bit 2's complement representation of "+5" is _____

- ► 1010
- ► 1110
- ► 1011
- ► 0101

Question No: 27 (Marks: 2)

Explain the erase operation in context of Flash Memory.

Question No: 28 (Marks: 2)

Explain the difference between 1-to-4 Demultiplexer and 2-to-4 Binary Decoder?

Question No: 29 (Marks: 2)

Some of the counters (e.g. 74HC163) are called pre-set counters. why?

Question No: 30 (Marks: 2)

How many bytes will be there in 32 K x 8 memory?

Question No: 31 (Marks: 3)
Differentiate between truth table and next-state table

Question No: 32 (Marks: 3)
Name the three types of errors Analogue to Digital converters exhibit during their conversion operation.

Question No: 33 (Marks: 3)
How can a serial in/parallel out register be used as a serial in/serial out register?

Question No: 34 (Marks: 5)
Explain the implementation of First In First Out (FIFO) Memory by using RAM.

Question No: 35 (Marks: 5)
Explain memory read operation with the help of an example

Question No: 36 (Marks: 5)
Explain the next-state table with the help of a table for any sequential circuit