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Question No: 1 (Marks: 1) - Please choose one

A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

- ► 1
- ► 2
- ► 4
- ► **8 (Page 356) rep**

Question No: 2 (Marks: 1) - Please choose one

A frequency counter _____

- ► Counts pulse width
- ► **Counts no. of clock pulses in 1 second (Page 301)**
- ► Counts high and low range of given clock pulse
- ► None of given options

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Question No: 3 (Marks: 1) - Please choose one
In a sequential circuit the next state is determined by _____ and _____

- ► State variable, current state
- ► Current state, flip-flop output
- ► Current state and external input
- ► **Input and clock signal applied (Page 305)**

Question No: 4 (Marks: 1) - Please choose one
The divide-by-60 counter in digital clock is implemented by using two cascading counters:

- ► **Mod-6, Mod-10 (Page 229) rep**
- ► Mod-50, Mod-10
- ► Mod-10, Mod-50
- ► Mod-50, Mod-6

Question No: 5 (Marks: 1) - Please choose one
In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained.

- ► **True (Page 221) rep**
- ► False

Question No: 6 (Marks: 1) - Please choose one
Flip flops are also called _____

- ► Bi-stable dualvibrators
- ► Bi-stable transformer
- ► **Bi-stable multivibrators (Page 228)**
- ► Bi-stable singlevibrators

Question No: 7 (Marks: 1) - Please choose one
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

- ► Set-up time
- ► **Hold time (Page 242) rep**
- ► Pulse Interval time
- ► Pulse Stability time (PST)

Question No: 8 (Marks: 1) - Please choose one
74HC163 has two enable input pins which are _____ and _____

- ► **ENP, ENT (Page 285)**
- ► ENI, ENC
- ► ENP, ENC
- ► ENT, ENI

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Question No: 9 (Marks: 1) - Please choose one

_____ is said to occur when multiple internal variables change due to change in one input variable

- Clock Skew
- **Race condition (Page 267)**
- Hold delay
- Hold and Wait

Question No: 10 (Marks: 1) - Please choose one

Given the state diagram of an up/down counter, we can find _____

- **The next state of a given present state (Page 371)**
- The previous state of a given present state
- Both the next and previous states of a given state
- The state diagram shows only the inputs/outputs of a given states

Question No: 11 (Marks: 1) - Please choose one

The _____ input overrides the _____ input

- **Asynchronous, synchronous (Page 369) rep**
- Synchronous, asynchronous
- Preset input (PRE), Clear input (CLR)
- Clear input (CLR), Preset input (PRE)

Question No: 12 (Marks: 1) - Please choose one

A logic circuit with an output $X = \overline{A}BC + A\overline{B}$ consists of _____.

- two AND gates, two OR gates, two inverters
- three AND gates, two OR gates, one inverter
- **two AND gates, one OR gate, two inverters (Lecture 8)**
- two AND gates, one OR gate

Question No: 13 (Marks: 1) - Please choose one

A decade counter is _____.

- Mod-3 counter
- Mod-5 counter
- Mod-8 counter
- **Mod-10 counter (Page 274)**

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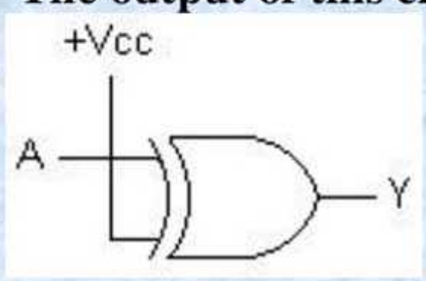
Question No: 14 (Marks: 1) - Please choose one
In asynchronous transmission when the transmission line is idle, _____

- ► It is set to logic low
- ► **It is set to logic high (Page 356) rep**
- ► Remains in previous state
- ► State of transmission line is not used to start transmission

Question No: 15 (Marks: 1) - Please choose one
A Nibble consists of _____ bits

- ► 2
- ► **4 (Page 394)**
- ► 8
- ► 16

Question No: 16 (Marks: 1) - Please choose one
The output of this circuit is always _____.



- ► 1
- ► 0
- ► **A Click here for detail rep**
- ► $\overline{A}$

Question No: 17 (Marks: 1) - Please choose one
Excess-8 code assigns _____ to "-8"

- ► 1110
- ► 1100
- ► 1000
- ► **0000 (Page 34) rep**

Question No: 18 (Marks: 1) - Please choose one
The voltage gain of the Inverting Amplifier is given by the relation _____

- ► **$V_{out} / V_{in} = - R_f / R_i$ (Page 446)**
- ► $V_{out} / R_f = - V_{in} / R_i$
- ► $R_f / V_{in} = - R_i / V_{out}$
- ► $R_f / V_{in} = R_i / V_{out}$

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Question No: 19 (Marks: 1) - Please choose one
LUT is acronym for _____

- **Look Up Table (Page 439) rep**
- Local User Terminal
- Least Upper Time Period
- None of given options

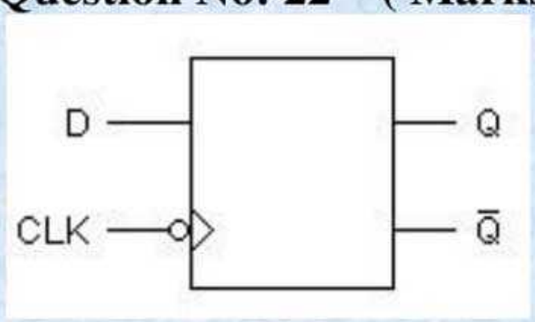
Question No: 20 (Marks: 1) - Please choose one
DRAM stands for _____

- **Dynamic RAM (Page 407)**
- Data RAM
- Demoduler RAM
- None of given options

Question No: 21 (Marks: 1) - Please choose one
The three fundamental gates are _____

- AND, NAND, XOR
- OR, AND, NAND
- NOT, NOR, XOR
- **NOT, OR, AND (Page 40)**

Question No: 22 (Marks: 1) - Please choose one



Which of the following statement is true regarding above block diagram?

- Triggering takes place on the negative-going edge of the CLK pulse
- Triggering takes place on the positive-going edge of the CLK pulse
- Triggering can take place anytime during the HIGH level of the CLK waveform
- Triggering can take place anytime during the LOW level of the CLK waveform

Question No: 23 (Marks: 1) - Please choose one
The total amount of memory that is supported by any digital system depends upon _____

- The organization of memory
- The structure of memory
- The size of decoding unit
- **The size of the address bus of the microprocessor (Page 430) rep**

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Question No: 24 (Marks: 1) - Please choose one
The expression F=A+B+C describes the operation of three bits _____ Gate.

- **OR (Page 42)**
- AND
- NOT
- NAND

Question No: 25 (Marks: 1) - Please choose one
Stack is an acronym for_____

- FIFO memory
- **LIFO memory (Page 429) rep**
- Flash Memory
- Bust Flash Memory

Question No: 26 (Marks: 1) - Please choose one
Addition of two octal numbers "36" and "71" results in _____

- 213
- 123
- **127**
- 345

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Question No: 1 (Marks: 1) - Please choose one
The storage cell in SRAM is
- a flip –flop
- **a capacitor (Page 407)**
- a fuse
- a magnetic domain

Question No: 2 (Marks: 1) - Please choose one
What is the difference between a D latch and a D flip-flop?
- The D latch has a clock input.
- The D flip-flop has an enable input.
- The D latch is used for faster operation.
- **The D flip-flop has a clock input.** Click here for detail

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Question No: 3 (Marks: 1) - Please choose one
For a positive edge-triggered J-K flip-flop with both J and K HIGH, the outputs will_____ if the clock goes HIGH.
► **toggle** **Click here for detail**
► set
► reset
► not change

Question No: 4 (Marks: 1) - Please choose one
The OR gate performs Boolean _____.
► multiplication
► subtraction
► division
► **addition (Page 42)**

Question No: 5 (Marks: 1) - Please choose one
If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be
► **set (Page 219)**
► reset
► invalid
► clear

5. Determine the values of A, B, C, and D that make the sum term A(bar) + B+C(bar)+D equal to zero.
► A = 1, B = 0, C = 0, D = 0
► **A = 1, B = 0, C = 1, D = 0 (Lecture 8)**
► A = 0, B = 1, C = 0, D = 0
► A = 1, B = 0, C = 1, D = 1

Question No: 6 (Marks: 1) - Please choose one
The power dissipation, *P*D, of a logic gate is the product of the
► **dc supply voltage and the peak current** **Click here for detail**
► dc supply voltage and the average supply current
► ac supply voltage and the peak current
► ac supply voltage and the average supply current

Question No: 7 (Marks: 1) - Please choose one
A Karnaugh map is similar to a truth table because it presents all the possible values of input variables and the resulting output of each value.
► **True** **Click here for detail**
► False

Question No: 8 (Marks: 1) - Please choose one
NOR Gate can be used to perform the operation of AND, OR and NOT Gate
► **True (Page 50)**
► False

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Question No: 9 (Marks: 1) - Please choose one
Using multiplexer as parallel to serial converter requires _____ connected to the multiplexer
►**A parallel to serial converter circuit (Page 244)**
►A counter circuit
►A BCD to Decimal decoder
►A 2-to-8 bit decoder

Question No: 10 (Marks: 1) - Please choose one
The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms
►4
►**8 (Page 89)**
►12
►16

Question No: 11 (Marks: 1) - Please choose one
In designing any counter the transition from a current state to the next sate is determined by
►**Current state and inputs (Page 332)**
►Only inputs
►Only current state
►current state and outputs

Question No: 12 (Marks: 1) - Please choose one
Sum term (Max term) is implemented using _____ gates
►**OR (Page 78)**
►AND
►NOT
►OR-AND

Question No: 13 (Marks: 1) - Please choose one
Given the state diagram of an up/down counter, we can find _____
► **The next state of a given present state (Page 371) rep**
► The previous state of a given present state
► Both the next and previous states of a given state
► The state diagram shows only the inputs/outputs of a given states

Question No: 14 (Marks: 1) - Please choose one
AT T0 THE VALUE STORED IN A 4-BIT LEFT SHIFT WAS "1". WHAT WILL BE THE VALUE OF REGISTER AFTER THREE CLOCK PULSES?
►2
►4
►6
►**8 (not sure)**

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Question No: 15 (Marks: 1) - Please choose one
WHEN BOTH THE INPUTS OF EDGE-TRIGGERED J-K FLOP-FLOP ARE SET TO LOGIC ZERO _____
►THE FLOP-FLOP IS TRIGGERED
►Q=0 AND Q'=1
►**Q=1 AND Q'=0 (Page 233)**
►**THE OUTPUT OF FLIP-FLOP REMAINS UNCHANGED**

Question No: 16 (Marks: 1) - Please choose one
If S=1 and R=0, then Q(t+1) = _____ for positive edge triggered flip-flop
►0
►**1 (Page 230)**
►Invalid
►Input is invalid

If S=1 and R=1, then Q(t+1) = _____ for negative edge triggered flip-flop
► 0
► 1
► **Invalid (Page 233)**
► Input is invalid

Question No: 17 (Marks: 1) - Please choose one
The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.
►Set-up time
►**Hold time (Page 242) rep**
►Pulse Interval time
►Pulse Stability time (PST)

Question No: 18 (Marks: 1) - Please choose one
We have a digital circuit. Different parts of circuit operate at different clock frequencies (4MHZ, 2MHZ and 1MHZ), but we have a single clock source having a fix clock frequency (4MHZ), we can get help by _____
►Using S-R Flop-Flop
►D-flipflop
►**J-K flip-flop (Page 252)**
►T-Flip-Flop

Question No: 19 (Marks: 1) - Please choose one
A counter is implemented using three (3) flip-flops, possibly it will have _____ maximum output status.
►3
►7
►**8 (Page 272)**
►15

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Question No: 20 (Marks: 1) - Please choose one
In _____ Q output of the last flip-flop of the shift register is connected to the data input of the first flip-flop of the shift register.
►Moore machine
►Meally machine
►Johnson counter
►Ring counter (Page 355)

Question No: 21 (Marks: 1) - Please choose one
The _____ of a ROM is the time it takes for the data to appear at the Data Output of the ROM chip after an address is applied at the address input lines
►Write Time
►Recycle Time
►Refresh Time
►Access Time (Page 417)

Question No: 22 (Marks: 1) - Please choose one
Bi-stable devices remain in either of their _____ states unless the inputs force the device to switch its state
►Ten
►Eight
►Three
►Two (Page 262)

Question No: 23 (Marks: 1) - Please choose one
_____occurs when the same clock signal arrives at different times at different clock inputs due to propagation delay.
►Race condition
►Clock Skew (Page 226) rep
►Ripple Effect
►None of given options

Question No: 24 (Marks: 1) - Please choose one
The alternate solution for a multiplexer and a register circuit is _____
►Parallel in / Serial out shift register (Page 356)
►Serial in / Parallel out shift register
►Parallel in / Parallel out shift register
►Serial in / Serial Out shift register

Question No: 25 (Marks: 1) - Please choose one
Stack is an acronym for _____
► FIFO memory
► LIFO memory (Page 429) rep
► Flash Memory
► Bust Flash Memory

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Question No: 26 (Marks: 1) - Please choose one
A full-adder has a Cin = 0. What are the sum (<PRIVATE "TYPE=PICT;ALT=sigma">) and the carry (Cout) when A = 1 and B = 1?
► = 0, Cout = 0
► = 0, Cout = 1 (Page 135)
► = 1, Cout = 0
► = 1, Cout = 1

Question No: 27 (Marks: 1) - Please choose one
THE GLITCHES DUE TO RACE CONDITION CAN BE AVOIDED BY USING A _____
►GATED FLIP-FLOPS
►PULSE TRIGGERED FLIP-FLOPS
►POSITIVE-EDGE TRIGGERED FLIP-FLOPS
►NEGATIVE-EDGE TRIGGERED FLIP-FLOPS (Page 267)

Question No: 28 (Marks: 1) - Please choose one
The design and implementation of synchronous counters start from _____

► Truth table
► k-map
► state table
► state diagram (Page 319)

Question No: 29 (Marks: 1) - Please choose one
THE HOURS COUNTER IS IMPLEMENTED USING _____
►ONLY A SINGLE MOD-12 COUNTER IS REQUIRED
►MOD-10 AND MOD-6 COUNTERS
►MOD-10 AND MOD-2 COUNTERS
►A SINGLE DECADE COUNTER AND A FLIP-FLOP (Page 299)

Question No: 30 (Marks: 1) - Please choose one
Given the state diagram of an up/down counter, we can find _____
► The next state of a given present state (Page 371) rep
► The previous state of a given present state
► Both the next and previous states of a given state
► The state diagram shows only the inputs/outputs of a given states

Question No: 31 (Marks: 1) - Please choose one
LUT is acronym for _____
► Look Up Table (Page 439) rep
► Local User Terminal
► Least Upper Time Period
► None of given options

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Question No: 32 (Marks: 1) - Please choose one

_____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

- ► Resolution
- ► **Accuracy (Page 460) rep**
- ► Quantization
- ► Missing Code

Question No: 33 (Marks: 1) - Please choose one

_____ is used to simplify the circuit that determines the next state.

- ►State diagram
- ►**Next state table**
- ►State reduction
- ►**State assignment (Page 335) rep**

Question No: 34 (Marks: 1) - Please choose one

The high density FLASH memory cell is implemented using _____

- ►**1 floating-gate MOS transistor (Page 419)**
- ►2 floating-gate MOS transistors
- ►4 floating-gate MOS transistors
- ►6 floating-gate MOS transistors

Question No: 35 (Marks: 1) - Please choose one

Q2 :=Q1 OR X OR Q3

The above ABEL expression will be

- ►Q2:= Q1 $ X $ Q3
- ►**Q2:= Q1 # X # Q3 (Page 210)**
- ►Q2:= Q1 & X & Q3
- ►Q2:= Q1 ! X ! Q3

Question No: 36 (Marks: 1) - Please choose one

Generally, the Power dissipation of _____ devices remains constant throughout their operation.

- ►**TTL (Page 65)**
- ►CMOS 3.5 series
- ►CMOS 5 Series
- ►Power dissipation of all circuits increases with time.

Question No: 37 (Marks: 1) - Please choose one

When the control line in tri-state buffer is high the buffer operates like a _____gate

- ►AND
- ►OR
- ►**NOT (Page 196)**
- ►XOR

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Question No: 38 (Marks: 1) - Please choose one

3.3 v CMOS series is characterized by _____ and _____as compared to the 5 v CMOS series.

►Low switching speeds, high power dissipation

►Fast switching speeds, high power dissipation

►**Fast switching speeds, very low power dissipation (Page 61)**

►Low switching speeds, very low power dissipation

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