1.. In FALCON A Program Counter (PC) and Instruction Register (IR) are of _____ bits

a) 32-bits
b) 24-bits
c) 16-bits
d) 64-bits

2. The multiplexer----------is used to decide which value is transferred to be written back to the register file.

a) MP2
b) MP3
c) MP4
d) MP5

3.) Which of the following condition is evaluated when executing the branch instruction "brzr R2, R1"?

a) If(R2==0)
b) If(R1 >0)
c) If(R1==0)
d) If(R1 < 0)

4. In case of SRC processor, bits---------of IR (instruction register) are reserved for the opcode.

a) 0 to 4
b) 11 to 15

c) 27 to 31
d) 59 to 63

5. Which of the given RTL description is used to represent "load instruction register" (ldr) instruction?

a) (op<4..0>=6): R[ra] ← rel
b) (op<4..0>=2): R[ra] ← M [rel]
c) (op<4..0>=2): M[disp] ← R [ra]
d) (op<4..0>=2): M[rel] ← R [ra]

6. -------- Instruction is used to divide a register value by immediate value in FALCON-E processor.

a) div
b) idiv
c) divi
d) divim

7. Which type of exceptions rise during the process of decoding and executing the instruction?

a) Program Exceptions
b) Hardware Exceptions
c) Non-mask able Exceptions
d) Interrupts (External Exceptions)

8. In a non-pipelined machine, there would be one instruction processed after an average of _____ cycles.

a) 1
b) 3
c) 5
d) 7

9. The instruction fetch procedure generally takes _____ time step(s).

a) One
b) Two
c) Four
d) Three

10. The third stage of the Pipelined version of SRC is;

a) Memory access
b) ALU operation
c) Instruction Fetch
d) Register writes

11. Which one of the followings is the correct RTL description for sign extension of an 8-bit constant?

a) (8αIR<7> ©IR<8.. 0>)
b) (8αIR<7> ©IR<7.. 0>)
c) (8αIR<8> ©IR<8.. 1>)
d) (8αIR<8> ©IR<7.. 0>)

12. _____ usually involves calculating the target address and evaluating a condition.

a) Load/Store instructions
b) Pipelined SRC
c) Branch Instructions
d) ALU instructions

13. From the given stages of pipelining, which one is used for loading an instruction from the memory for execution?

a) Memory Access
b) ALU Operation
c) Fetch Instruction
d) Fetch Operand

14. _____ hazard occurs when attempting to access the same resource in different ways at the same time

a) Data
b) Branch
c) Structural
d) Instruction

15. In the 3-bus Implementation for the SRC, all the special purpose as well as the general purpose registers have _____ read port(s) _____ write port(s).

a) two, two
b) two, one
c) one, two
d) three, one

16. Which field of machine language instruction is the "type of operation" that is to be performed.

a) Op-code(or the operation code)
b) CPU register
c) Memory Cells
d) I/O Location

17. Which of the following control signal is NOT activated during instruction fetch operation?

a) PCout
b) LC
c) LMAR

d) Cout

18. In case of FALCON-A---------- instruction are present which are not present in SRC processor.

a) create and destroy
b) in and out
c) open and close
d) read and write

19. ---------- provides a temporary storage for the address of memory location to be accessed.

a) MAR
b) MBR
c) PC
d) LPC

20. Which of the following register is used to enable the tri-stable buffers with the MBR?

a) MBRout
b) MARout
c) LMBR
d) INC4

21. What functionality is performed by the instruction "str R8, 34" of SRC?

a) It will load the register R8 with the contents of the memory location M[PC+34]
b) It will load the register R8 with the contents of the memory location M[34]
c) It will store the register R8 contents to the memory location M[PC+34]
d) It will store the register R8 contents to the memory location M[34]

22. Program Counter(PC) holds the memory address of:

a) Previous Instruction
b) Current Instruction
c) Next Instruction
d) Previous and Current Instruction

23. What is the working of Processor Status Word (PSW)?

a) To hold the current status of the processor
b) To hold the current address of the process
c) To hold the instruction that the computer is currently processing
d) To hold the address of the next instruction in memory that is to be executed

24. mul is the example of a(n)---------- operation.

a) Logic
b) Shift
c) Arithmetic
d) Data transfer

25. Control Signal for RTL "IR< ---MBR" will be---------

a) MBRout,LIR
b) PC< --C
c) PC< --MBR
d) PC< --IR

26. Which of the following control signals is used to copy the contents of "in" bus on the "out" bus so

a) MRead
b) MIR
c) C=B
d) LMAR

27. Which of the following is responsible for generating signals for external events?

a) Interrupt generator
b) Exception generator
c) "CON" control signal
d) Control unit signals generator

28. Which one of the following control signals allows the value of register rc to be read?

a) LCON
b) RBE
c) RCE
d) RCON

29. Program counter (PC) and Instruction register (IR) are normally 16-Bit registers, however in SRC, these are _____.

a) 16-Bit
b) 32-Bit
c) 64-Bit
d) 31-Bit

30. _____hazard occurs when an instruction attempts to access some data value that has not yet been updated by the previous instruction.

a) Data
b) Branch
c) Structural
d) Instruction

31. What does the instruction"ldr R3, 58" of SRC do?

•

a) It will load the register R3 with the contents of the memory location M[PC+58]
b) It will load the register R3 with the relative address itself(PC+58)
c) It will store register R3 contents to the memory location M[PC+58]
d) It will store the value of register R3 at the relative address itself(PC+58)

32. The status register of the 68000 has -------- condition codes.

a) 2
b) 3
c) 5
d) 8

33. Which of the instruction is used to load register from memory using relative address?

a) ld instruction
b) ldr instruction
c) lar instruction
d) str instruction

34. For the ------ type instruction, we require a register to hold the data that is to be loaded from the memory, or stored back to the memory.

a) Jump
b) Control
c) load/store
d) Branch

35. In a processor, ---------- is responsible for the synchronization of internal as well external events.

a) Memory Unit
b) Data Unit
c) Arithmetic & Logic Unit
d) Control Unit

36. In CPU design, ---------- creates or forms the interface between the data path and control unit.

a) Buses
b) ALU
c) Control signal
d) Cache

37. In Falcon-A processor, first 5 most significant bits from the IR are fed to a _____ decoder.

a) 11-to-15
b) 5-to-31
c) 5-to-10
d) 5-to-32

38. The Memory Buffer Register (MBR) has a _____ connection with both the memory sub-system and the registers/ALSU.

a) bi-directional
b) uni-directional
c) tri-directional
d) zero-directional

39. The SRC uses a hazard detection unit. The hazard can be resolved using either pipeline stalls or by _____.

a) Data forwarding
b) Data compressing
c) Instruction handling
d) Instruction forwarding

40. The _____ control signal is used to enable the tri-state buffers with the MBR.

a) LMBR
b) MARout
c) MBRout
d) LMAR

41. jump [ra+c2] is an _____ instruction

a) Unconditional jump
b) Arithmetic and logic
c) Conditional jump
d) Shift

42. MC68000 has a 32-bit program counter but only the least significant _____ bits are used,

a) 16
b) 20
c) 24
d) 8

43. Which operator is used to 'name' registers, or part of registers, in the Register Transfer Language?

a) A.:=
b) B. %
c) C. @
d) D. &

44. A _____ is a computer program used to aid indetecting errors in a program.

a) Linker
b) Compiler
c) Assembler
d) Debugger

45. RTL statements separated by _____ are always executed in same clock pulse.

a) Hash (#)
b) Colon (:)
c) Comma (,)
d) Semi-colon (;)

46. In "DIV R3" instruction of EAGLE, the register _____ is used as both source operand and destination operand.

a) R0
b) R2
c) R1
d) R3

47. Which of the following branch instructions has a condition which is always executed?

a) jmi
b) jump
c) jz
d) jpl

48. Which of the following directives is used in FALSIM to define a variable?

a) .dd
b) .dw
c) .org
d) .equ

49. In Falcon-A processor, the size of each I/O port is _____.

a) 8 bits
b) 16 bits
c) 256 bytes
d) 8 bytes

50. Which of the following instruction is considered most important in a pipelined EAGLE architecture?

a) INIT
b) NOP
c) HALT
d) RESET

51. The size of data bus of MC68000 processor is _____.

a) 8 bits
b) 16 bits
c) 32 bits
d) 64 bits

52. In Type-1 instruction, bits _____ are reserved for the op-code.

a) bits 1 through 5
b) bits 0 through 4
c) bits 0 through 8
d) bits 11 through 15

53. Program counter (PC) holds the memory address of _____?

a) Next instruction Page 104
b) Current Instruction
c) Previous Instruction
d) Previous and Current Instruction

54. Which type of instructions help in changing the flow of the program as and when required?

a) Control
b) Arithmetic
c) Data transfer
d) Floating point

55. Which one of the following is a bi-stable device, capable of storing one bit of Information?

a) Diplexer
b) Decoder
c) Flip-flop
d) Multiplexer

56. The SPARC architecture defines a _____ that allows for multiple address spaces.

a) Memory Logic Unit (MLU)
b) Memory Shifting Unit (MSU)
c) Memory Mapping Unit (MMU)
d) Memory Arithmetic Unit (MAU)

57. The multiplexer---------- is used to decide which value is transferred to be written back to the register file.

a) MP2
b) MP3
c) MP3
d) MP5

58. Which one of the following control signals causes the data from the bus to be read into the register MAR.

a) MARout
b) MARin
c) LMAR
d) None of the given

59. The instruction "PUSH A" is an example of ----------

a) 0-address instruction
b) 1-address instruction
c) 2-address instruction
d) 3-address instruction

60. Which of the following is NOT an advantage of using register-to-register data transfers?

a) It is faster
b) It is simpler
c) It is most compact
d) It is easier to pipeline

61. ---------- hazard occurs when attempting to access same resource in different ways at the same time.

a) Branch
b) Data
c) Structural
d) Instruction

62. VLIW Stands for----------

a) Variable Length Instruction Word
b) Very Long Instruction Word
c) Very Long Instruction Width
d) Variable Length Instruction Width

63. In SRC, the general-purpose register file includes---------- registers, each 32 bit wide.

a) 6 Registers R0 to R15
b) 24 Registers R0 to R23
c) 32 Registers R0 to R31
d) 64 Registers R0 to R63

64. How can we refer to an instruction register (IR), of 16 bits (numbered 0 to 15) using RTL.

a) IR<16..0>
b) IR<15..0>
c) IR<16..1>
d) IR<15..1>

65. Which one of the following portions of an instruction represents the operation to be performed?

a) Address
b) Instruction code
c) Opcode
d) Operand

66. Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?

a) Processor-Memory-Switch level (PMS level)
b) Instruction Set Level
c) Register Transfer Level
d) None of the given

67. Which one of the following circuit design levels is called the gate level?

a) Logic Design Level

b) Circuit Level
c) Mask Level
d) None of the given

68. The CPU includes three types of instructions, which have different operands and will need different representations. Which one of the instructions requires two source registers?

a) Jump and branch format instructions
b) Immediate format instructions
c) Register format instructions
d) All of the above

69. The instruction ----------will load the register R3 with the contents of the memory location M [PC+56]

a) Add R3, 56
b) lar R3, 56
c) ldr R3, 56
d) str R3, 56

70. An "assembler" that runs on one processor and translates an assembly language program written for another processor into the machine language of the other processor is called a ----------

a) compiler
b) cross assembler
c) debugger
d) linker

71. Which instruction is used to store register to memory using relative address.

a) ld instruction
b) ldr instruction
c) lar instruction
d) str instruction

72. Which of the following statements is/are true about RISC processors' claimed advantages over CISC processors?

(a) Keeping regularly accessed variables in registers as opposed to keeping them in memory facilitates faster execution.

(b) RISC CPUs outperform CISC CPU's in procedural programming environments.

(c) Instruction pipelining has helped RISC CPU's to attain a target of 1 cycle per instruction.

(d) It is easier to maintain the "family concept" in RISC CPU.

a) (a), (b) &(c)
b) (b), (c) & (e)
c) (c), (d) & (e)
d) (a), (c) & (d)

73. Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?

a) Processor-Memory-Switch level (PMS level)
b) Instruction Set Level
c) Register Transfer Level
d) None of the given

74. In which one of the following techniques, the time a processor spends waiting for instructions to be fetched from memory is minimize

a) Perfecting
b) Pipelining
c) Superscalar operation
d) Speedup

75. Computer system performance is usually measured by the ----------

a) Time to execute a program or program mix
b) The speed with which it executes programs
c) Processor's utilization in solving the problems
d) Instructions that can be carried out simultaneously

76. Among the two approaches available to design a control unit, hardware approach is relatively---------- as compared to micro-programming.

a) Slow
b) Fast
c) Average
d) Better

77. ---------- is defined as the number of instructions processed per second.

a) Memory access
b) Throughput
c) ALU operation
d) Latency

78. ---------- is an example of Miscellaneous instruction:

a) Shift
b) Store
c) Halt
d) Cell

79. Which one of the following operations is NOT performed by using miscellaneous instructions?

a) Clearing all registers
b) Stopping the processor
c) NOP

d) Returning from a procedure

80. RISC stands for?

a. Registers internal system cache
b. Reduced instruction set computer
c. Registers instruction set computer
d. Reduced internal system computers

81. The SPARC architecture defines a ---------- that allows for multiple address spaces.

a) Memory Location Unit(MLU)
b) Memory Mapping Unit(MMU)
c) Memory Shifting Unit (MSU)
d) Memory Arithmetic Unit (MAU)

82. A collection of all possible machine language commands that a computer can understand and execute is called _____.

a) Opcodes
b) Bytecodes
c) Mnemonics
d) Instruction Set

83. The syntax of the instruction 'branch and link if zero' is

a) brlzr ra, rb, rc
b) brzr ra, rb, rc
c) brnz ra, rb, rc
d) brinz ra, rb, rc

84. Which one of the following register holds the instruction that is being executed?

a) Accumulator
b) Address Mask
c) Program Counter
d) Instruction Register

85. _____ is defined as the time required to process a single instruction.

a) Latency Page 217
b) Throughput
c) ALU operation
d) Memory access

86. CISC Stands for?

a) Complex internal system computer
b) Computer instruction set compiler
c) Complex instruction system compiler
d) Complex Instruction Set Computers

87. Which one of the following is the memory organization of FALCON-E processor?

a) 28 * 8 bits
b) 216 * 8 bits
c) 232 * 8 bits
d) 264 * 8 bits

88. Prefetching can be considered a primitive form of----------

a) Multi-processing
b) Self-execution
c) Exception
d) Pipelining

89. _____ controller controls the sequence of the flow of microinstructions.

a) Multiplexer
b) Microprogram
c) ALU
d) None of the given

90. Flip-flop is a _____device, capable of storing one bit of Information

a) Bi-stable
b) Unit-stable
c) Stable
d) Storage

91. Execution time of a program with respect to the processor is calculated as:

a) Execution Time = IC x CPI x MIPS
b) Execution Time = IC x CPI x T
c) Execution Time = CPI x T x MFLOPS
d) Execution Time = IC x T

92. Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?

a) Processor-Memory-Switch level (PMS level)
b) Instruction Set Level
c) Register Transfer Level
d) None of the given

93. Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A and source register B) from the following example. ADD R1, R2, R3

a) Opcode= R1, DR=ADD, SA=R2, SB=R3
b) Opcode= ADD, DR=R1, SA=R2, SB=R3

c) Opcode= R2, DR=ADD, SA=R1, SB=R3
d) Opcode= ADD, DR=R3, SA=R2, SB=R1

94. Which of the following condition is evaluated when executing the branch instruction "brzr R2, R1"?

a) If(R2==0)
b) If(R1 >0)
c) If(R1==0)
d) If(R1 < 0)

95. In case of FALCON-A---------- instruction are present which are not present in SRC processor.

a) create and destroy
b) in and out
c) open and close
d) read and write

96. Which of the following register is used to enable the tri-stable buffers with the MBR?

a) MBRout
b) MARout
c) LMBR
d) INC4

97. mul is the example of a(n)---------- operation.

a) Logic
b) Shift
c) Arithmetic
d) Data transfer

98. VLIW Stands for----------

a) Variable Length Instruction Word
b) Very Long Instruction Word
c) Very Long Instruction Width
d) Variable Length Instruction Width

99. In SRC, the general-purpose register file includes---------- registers, each 32 bit wide.

a) 6 Registers R0 to R15
b) 24 Registers R0 to R23
c) 32 Registers R0 to R31
d) 64 Registers R0 to R63

100. What does the word 'D' in the 'D-flip-Flop' stands for?

a) Data
b) Digital
c) Dynamic
d) Double

101. Which of the following can be defined as an address of the operand in a computer type instruction or the target address in a branch type instruction?

A. Base address
B. Binary address
C. Effective address
D. All of the given

102. Computer system performance is usually measured by the ----------

a) Time to execute a program or program mix
b) The speed with which it executes programs
c) Processor's utilization in solving the problems

d) Instructions that can be carried out simultaneously

103. In FALCON-A ISA, which of the following opcodes is used to perform "No Operation"?

a) 20
b) 21
c) 22
d) 23

104. Which of the followings is not an example of super-scalar processors?

a) PowerPC601
b) IAPX88
c) Intel P6
d) DEC Alpha 21164

105. What does the instruction "idr R3, 58" of SRC do?

a) It will load register R3 with the contents of the memory location M[PC+58]
b) It will load register R3 with the relative address itself (PC+58)
c) It will store register R3 contents to the memory location M[PC+58]
d) It will store the value of register R3 at the relative address itself (PC+58)

106. Which of the following EAGLE instructions is used to initialize all the registers by setting them to 0?

a) NOP
b) HALT
c) INIT
d) RESET

107. Which temporary register is loaded with either a register value from the register file or a constant from the instruction?

a) Y3
b) X3
c) Z4
d) Z5

108. A computer belongs to which of the following subset of the systems?

a) Mechanical system
b) Electrical system
c) Optical system
d) Magnetic system

109. Which of the following operations is NOT performed by using miscellaneous instruction?

a) Clearing all registers
b) Stopping the processor
c) NOP
d) Returning from a procedure

110. which it was originally developed.

a) Backward compatibility
b) Data migration
c) Reverse engineering
d) Upward compatibility

111. Which of the following is example of direct indirect addressing mode?

a) M[R6]
b) M[R5]
c) M[R1+25]

d) M[[R5] + [R6]]

112. Computer system performance is usually measured by the ----------

a) Time to execute a program or program mix
b) The speed in which it executes programs
c) Processor's utilization in solving the problems
d) Instructions that can be carried out simultaneously

113. Which of the the given below measures is/are used for comparison of performance of various machine?

a) Execution time
b) MFLOPS
c) MIPS
d) All of the given

114. What functionality is performed by the by the instruction "lar R3, 36" performed.

a) It will load the register R3 with the contents of memory location M[PC+36]
b) It will load the register R3 with the relative address itself (PC+36)
c) It will store the register R3 contents of memory location M[PC+36]
d) It will left rotate the value of R3 36 times and will store the value in R3

115. Which type of instructions load data from memory into registers, or store data from registers into memory and transfer data between different kinds of special-purpose registers?

Data transfer

116. What does the RTL expression [M(1234)] means?

The contents of memory whose address is 1234.

117. Which one of the following languages presents a simple, human oriented language to specify the operations, register communication and timing of the steps that take place within a CPU to carry out higher level (user programmable) instructions?

RTL (Register Transfer Language)

118. An instruction that specifies one operand in memory and one operand in a register would be known as a _____ address instruction.

1-1/2

119. In this figure, the constant value specified by the immediate field is added to the register value, and the resultant is the index of memory location that is referred i.e. Effective Address = A + (content of R) . Identify the addressing mode.

Displacement

120. In MC68000, only the last _____ bits of 32-bit program counter (PC) register are used to store memory addresses.

The last 24 bits of the 32-bit Program

121. he instruction shifti R1, R2, 20 is an example of which of the following addressing modes?

Immediate

122. Which of the following measure can be best used for calculating the performance of computation intensive application

MFLOPS

123. _____ instruction is used to evaluate logical exclusive or in FALCON-E processor

Xor, xori

124. Which of the following RTL description is used to represent all general purpose register of SRC?

R[0..31]<31..0>;

125. Which of the following RTL description is used to represent the target register of Falcon-A instruction

Ra<2..0>:=IR<10..8>

126. Which of the following bits of SRC instruction are used to hold a second operand, conditional test, or a shift count register?

The bits 16 through 12

127. A stack based machine is also called _____.

0-address machine

128. _____ instruction is used to store register contents to memory

St

129. Which of the given RTL description is used to represent branch and bank (brl) instruction?

Cond : (PC <- R [rb]))

130. Which of the given RTL description is used to represent store register relative (str) instruction?

(op<4..0>=4):M[rel]<-R[ra]

131. Which of the given RTL description is used to represent conditional branch (br) instruction?

(op<4..0>=8): (cond : PC<- R[rb]),

132. Which of the given RTL description is used to represent load relative address (Iar) instruction?

(op<4..0=6):R[ra]<-rel

133. In a simple RISC computer the size of each register is _____.

32 bits

134. A _____ is a device that provides a shared data path to a number of devices that are connected to it.

Bus

Best of Luck