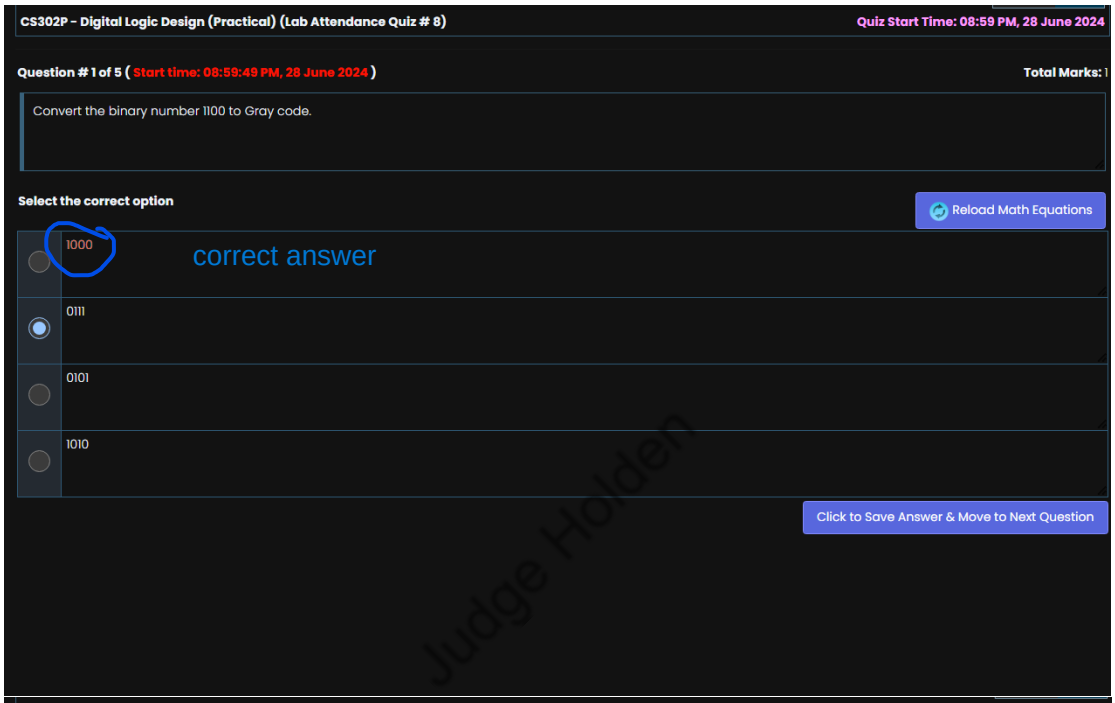
(Virtual University)

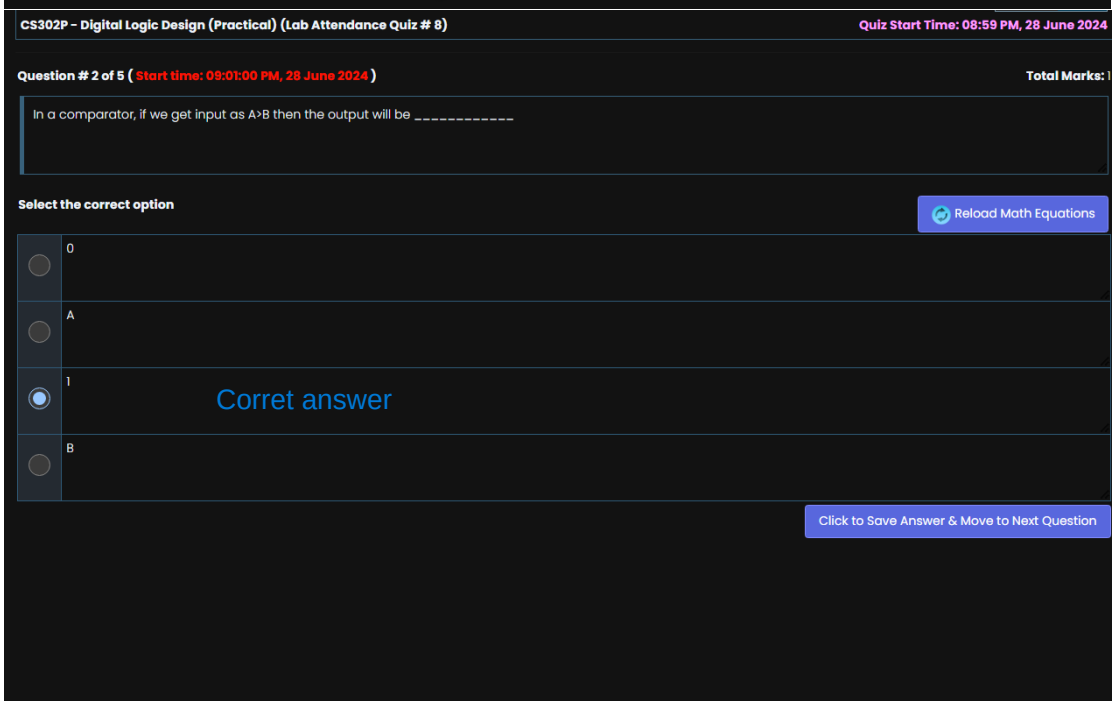
Spring 2024

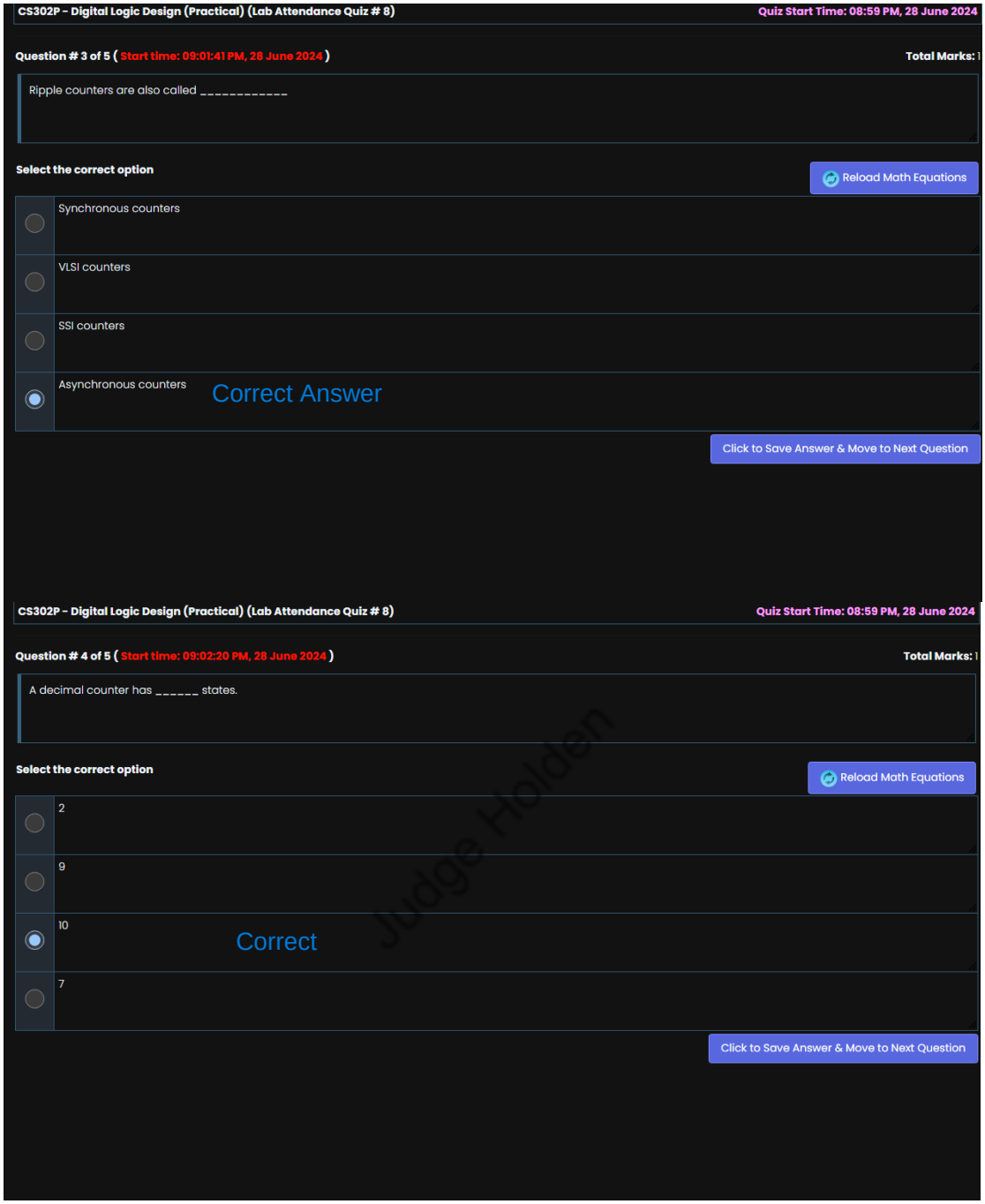
CS201(Introduction to Programming) Final Term MCQ's 2024

Made by Default.

Warning: There is a chance that there are some wrong answers. All students are told to cross check these answers for better understanding of these concepts which will ultimately help you for the preparation of the Final Term Papers.






CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 8)
Quiz Start Time: 08:59 PM, 28 June 2024
Question # 3 of 5 (Start time: 09:01:41 PM, 28 June 2024)
Total Marks:
Ripple counters are also called _____
Select the correct option
Reload Math Equations
Synchronous counters
VLSI counters
SSI counters
Asynchronous counters
Correct Answer
Click to Save Answer & Move to Next Question
CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 8)
Quiz Start Time: 08:59 PM, 28 June 2024
Question # 4 of 5 (Start time: 09:02:20 PM, 28 June 2024)
Total Marks:
A decimal counter has _____ states.
Select the correct option
Reload Math Equations
2
9
10
Correct
7
Click to Save Answer & Move to Next Question
Judge Holden

CS302P – Digital Logic Design (Practical) (Lab Attendance Quiz # 8) — **Quiz Start Time: 08:59 PM, 28 June 2024**

Question # 5 of 5 (Start time: 09:02:49 PM, 28 June 2024) — **Total Marks:** 1

What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops?

Select the correct option

Reload Math Equations

- (●) 0 to $2^n - 1$ — Correct
- ( ) 0 to 2^n
- ( ) 0 to 2^{n+1}
- ( ) 0 to $2^n + 1$

Click to Save Answer & Move to Next Question

CS302P – Digital Logic Design (Practical) (Lab Attendance Quiz # 9) — **Quiz Start Time: 10:18 AM, 05 July 2024**

Question # 1 of 5 (Start time: 10:18:37 AM, 05 July 2024) — **Total Marks:** 1

Convert the Gray code 1011 to binary.

Select the correct option

Reload Math Equations

- ( ) 0111
- ( ) 1010
- (●) 1101 — Correct
- ( ) 1011

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 9) Quiz Start Time: 10:18 AM, 05 July 2024

Question # 2 of 5 (Start time: 10:19:16 AM, 05 July 2024) Total Marks: 1

Comparators are used in _____

Select the correct option

Reload Math Equations

Correct answer is all of these
you can check from google

- (•) Motherboard
- ( ) CPU
- ( ) Hard Drive
- ( ) Memory

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 9) Quiz Start Time: 10:18 AM, 05 July 2024

Question # 3 of 5 (Start time: 10:20:06 AM, 05 July 2024) Total Marks: 1

Which of the following is an invalid BCD code?

Select the correct option

Reload Math Equations

- ( ) 0101
- ( ) 0011
- (•) 1101
- ( ) 1001

Click to Save Answer & Move to Next Question

CS302P – Digital Logic Design (Practical) (Lab Attendance Quiz # 9) Quiz Start Time: 10:18 AM, 05 July 2024

Question # 4 of 5 (Start time: 10:20:51 AM, 05 July 2024) **Total Marks:** 1

Why do we use Gray Code?

Select the correct option

Reload Math Equations

- To count the number or bit changes
- Error Correction
- Invert the code
- Error Detection

correct

Click to Save Answer & Move to Next Question

CS302P – Digital Logic Design (Practical) (Lab Attendance Quiz # 9) Quiz Start Time: 10:18 AM, 05 July 2024

Question # 5 of 5 (Start time: 10:22:16 AM, 05 July 2024) **Total Marks:** 1

In a comparator, if we get input as A>B then the output will be _____

Select the correct option

Reload Math Equations

- 1

correct

- B
- 0
- A

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 (Graded)) Quiz Start Time: 11:15 AM, 25 June 2024

Question # 2 of 10 (Start time: 11:15:57 AM, 25 June 2024) **Total Marks:** 1

In a full adder circuit having inputs **A = 1, B =1, Cin = 0**, the outputs **S** and **Cout** will be _____.

Select the correct option

Reload Math Equations

- S = 1, Cout = 0
- S = 0, Cout = 0
- S = 1, Cout = 1
- S = 0, Cout = 1 — Correct

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 (Graded)) Quiz Start Time: 11:15 AM, 25 June 2024

Question # 3 of 10 (Start time: 11:16:31 AM, 25 June 2024) **Total Marks:** 1

Which of the following gates is used for parity generation for a binary data string?

Select the correct option

Reload Math Equations

- NOR
- XOR — Correct
- AND
- OR

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 (Graded)) Quiz Start Time: 11:15 AM, 25 June 2024

Question # 5 of 10 (Start time: 11:17:41 AM, 25 June 2024) Total Marks: 1

Don't care conditions can be used for simplifying Boolean expressions in _____.

Select the correct option

Reload Math Equations

- Latches
- Registers
- Terms
- K-maps

Correct

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Semester Quiz # 03 (Graded)) Quiz Start Time: 11:15 AM, 25 June 2024

Question # 6 of 10 (Start time: 11:18:06 AM, 25 June 2024) Total Marks: 1

When implementing a half adder by using gates, which of the following gates is used to return carry bit as an output?

Select the correct option

Reload Math Equations

- XOR
- OR
- NAND
- AND

CORRECT

Click to Save Answer & Move to Next Question

CS302P – Digital Logic Design (Practical) (Semester Quiz # 03 (Graded)) Quiz Start Time: 11:15 AM, 25 June 2024

Question # 7 of 10 (Start time: 11:18:38 AM, 25 June 2024) **Total Marks:** 1

To build a full adder using gates, how many gates are required?

Select the correct option

Reload Math Equations

- (•) 2 AND gates, 2 XOR gates, 1 OR gate — Correct
- ( ) 1 AND gate, 2 OR gates, 1 XOR gate
- ( ) 2 AND gates, 2 OR gates, 2 XOR gates
- ( ) 2 AND gates, 3 OR gates, 1 XOR gates

Click to Save Answer & Move to Next Question

CS302P – Digital Logic Design (Practical) (Semester Quiz # 03 (Graded)) Quiz Start Time: 11:15 AM, 25 June 2024

Question # 8 of 10 (Start time: 11:19:14 AM, 25 June 2024) **Total Marks:** 1

The K-map based Boolean reduction is based on the following Unifying Theorem: A + A' = 1.

Select the correct option

Reload Math Equations

- ( ) Force
- ( ) Non Impact
- (•) Complementarity — Correct
- ( ) Impact

Click to Save Answer & Move to Next Question

CS302P – Digital Logic Design (Practical) (Semester Quiz # 03 (Graded)) Quiz Start Time: 11:15 AM, 25 June 2024

Question # 9 of 10 (Start time: 11:19:47 AM, 25 June 2024) **Total Marks:** 1

A half adder can be built by using the combination of _____ and _____ gates.

Select the correct option

Reload Math Equations

- OR, XOR
- AND, NOT
- AND, OR
- AND, XOR

CORRECT

Click to Save Answer & Move to Next Question

CS302P – Digital Logic Design (Practical) (Semester Quiz # 03 (Graded)) Quiz Start Time: 11:15 AM, 25 June 2024

Question # 10 of 10 (Start time: 11:20:23 AM, 25 June 2024) **Total Marks:** 1

How many select lines would be required for an 8x1 multiplexer?

Select the correct option

Reload Math Equations

- 3

Correct

- 8
- 1
- 2

Click to Save Answer & Move to Next Question

CS302P – Digital Logic Design (Practical) (Semester Quiz # 04 (Graded)) Quiz Start Time: 01:05 PM, 02 July 2024

Question # 1 of 10 (Start time: 01:05:54 PM, 02 July 2024) **Total Marks:** 1

When implementing a half adder by using gates, which of the following gates is used to give Sum (S) as an output?

Select the correct option Reload Math Equations

- NOR
- OR
- AND
- XOR

Correct

Click to Save Answer & Move to Next Question

CS302P – Digital Logic Design (Practical) (Semester Quiz # 04 (Graded)) Quiz Start Time: 01:05 PM, 02 July 2024

Question # 2 of 10 (Start time: 01:06:20 PM, 02 July 2024) **Total Marks:** 1

Convert the binary number 1100 to Gray code.

Select the correct option Reload Math Equations

- 0101
- 1010

correct

- 1000
- 0111

Click to Save Answer & Move to Next Question

CS302P – Digital Logic Design (Practical) (Semester Quiz # 04 (Graded)) Quiz Start Time: 01:05 PM, 02 July 2024

Question # 3 of 10 (Start time: 01:07:06 PM, 02 July 2024) Total Marks: 1

Which of the following symbols is used to represent XOR operation?

Select the correct option

Reload Math Equations

- x
- ⊕ correct
- +
- ^

Click to Save Answer & Move to Next Question

CS302P – Digital Logic Design (Practical) (Semester Quiz # 04 (Graded)) Quiz Start Time: 01:05 PM, 02 July 2024

Question # 4 of 10 (Start time: 01:07:37 PM, 02 July 2024) Total Marks: 1

There are _____ cells in a 5-variable K-map.

Select the correct option

Reload Math Equations

- 64
- 24
- 16
- 32 correct

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04 (Graded)) Quiz Start Time: 01:05 PM, 02 July 2024

Question # 5 of 10 (Start time: 01:08:05 PM, 02 July 2024) **Total Marks:** 1

The parallel outputs of a counter circuit represent the _____

Select the correct option

Reload Math Equations

- Clock frequency
- Clock count
- Counter modulus
- Parallel data word

correct

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04 (Graded)) Quiz Start Time: 01:05 PM, 02 July 2024

Question # 6 of 10 (Start time: 01:08:34 PM, 02 July 2024) **Total Marks:** 1

Which of the following expressions represents **S** output in a full adder?

Select the correct option

Reload Math Equations

- $(A + B) \times C_{in}$
- $(A \times C_{in}) \oplus B$
- $(A \times B) \oplus C_{in}$
- $A \oplus B \oplus C_{in}$

correct

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04 (Graded)) Quiz Start Time: 01:05 PM, 02 July 2024

Question # 8 of 10 (Start time: 01:10:14 PM, 02 July 2024) Total Marks: 1

There are _____ cells in a 4-variable K-map.

Select the correct option

Reload Math Equations

- 8
- 20
- 24
- 16 corrct

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Semester Quiz # 04 (Graded)) Quiz Start Time: 01:05 PM, 02 July 2024

Question # 9 of 10 (Start time: 01:10:44 PM, 02 July 2024) Total Marks: 1

Don't care conditions can be used for simplifying Boolean expressions in _____.

Select the correct option

Reload Math Equations

- K-maps correct
- Registers
- Latches
- Terms

Click to Save Answer & Move to Next Question

CS302P – Digital Logic Design (Practical) (Semester Quiz # 04 (Graded))

Quiz Start Time: 01:05 PM, 02 July 2024

Question # 10 of 10 (Start time: 01:11:09 PM, 02 July 2024)

Total Marks: 1

Which of the following gates is used for parity generation for a binary data string?

Select the correct option

Reload Math Equations

- OR
- XOR (correct)
- NOR
- AND

Click to Save Answer & Move to Next Question

CS302P – Digital Logic Design (Practical) (Lab Attendance Quiz # 9)

Quiz Start Time: 02:04 PM, 05 July 2024

Question # 2 of 5 (Start time: 02:04:22 PM, 05 July 2024)

Total Marks: 1

Reflected Binary Code is also known as _____ code.

Select the correct option

Reload Math Equations

- Gray Code (correct)
- Excess-3
- ASCII
- BCD

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 9) Quiz Start Time: 02:04 PM, 05 July 2024

Question # 3 of 5 (Start time: 02:04:54 PM, 05 July 2024) **Total Marks:** 1

Convert the binary number 1100 to Gray code.

Select the correct option Reload Math Equations

- (●) 1010 correct
- ( ) 1000
- ( ) 0101
- ( ) 0111

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 9) Quiz Start Time: 02:04 PM, 05 July 2024

Question # 4 of 5 (Start time: 02:05:32 PM, 05 July 2024) **Total Marks:** 1

Which one is a basic comparator?

Select the correct option Reload Math Equations

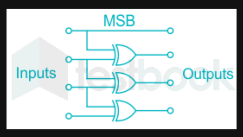
- (●) XOR Correct
- ( ) NAND
- ( ) AND
- ( ) OR

Click to Save Answer & Move to Next Question

CS302P - Digital Logic Design (Practical) (Lab Attendance Quiz # 9) **Quiz Start Time: 02:04 PM, 05 July 2024**

Question # 5 of 5 (Start time: 02:06:11 PM, 05 July 2024) **Total Marks: 1**

Following diagram is of _____ code conversion.



Select the correct option

Reload Math Equations

- BCD
- Gray
- Excess-3
- ASCII

Click to Save Answer & Move to Next Question