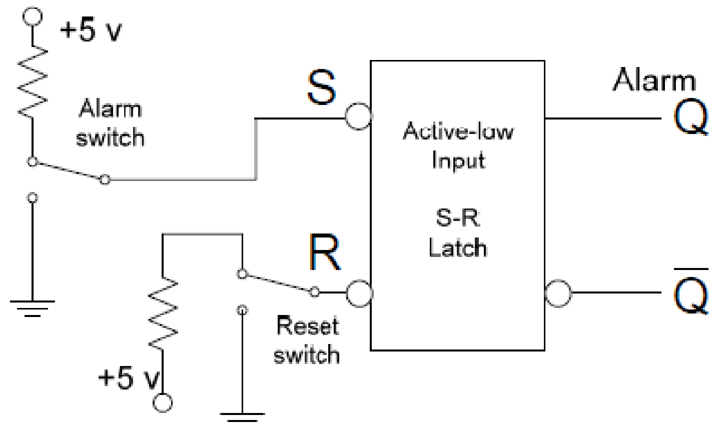

Figure 23.1c The switch connected through an S-R latch

The circuit diagram in figure 23.1c shows a burglar alarm circuit. The

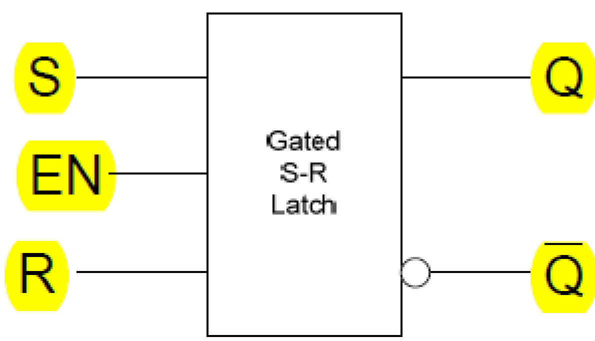

Figure 23.3 Logic Symbol of a Gated S-R Latch

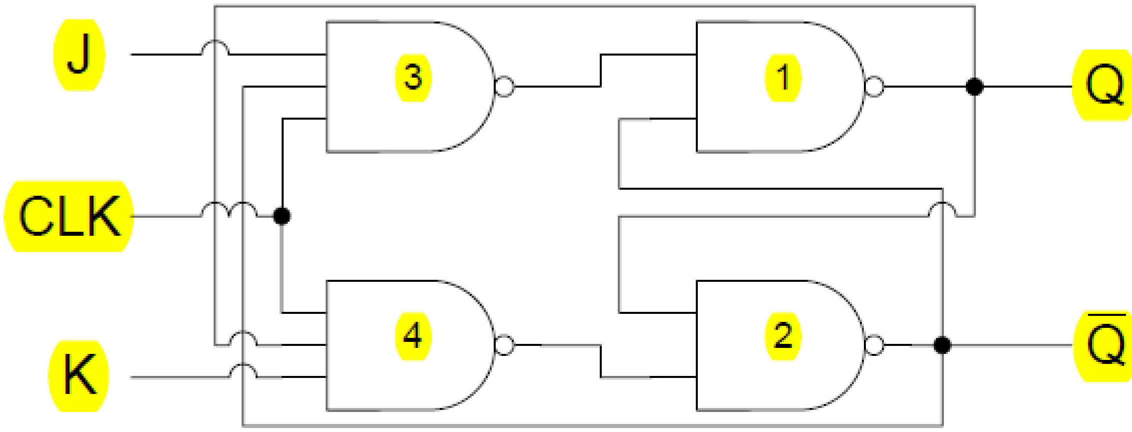

Figure 23.14 Edge-triggered J-K flip-flop

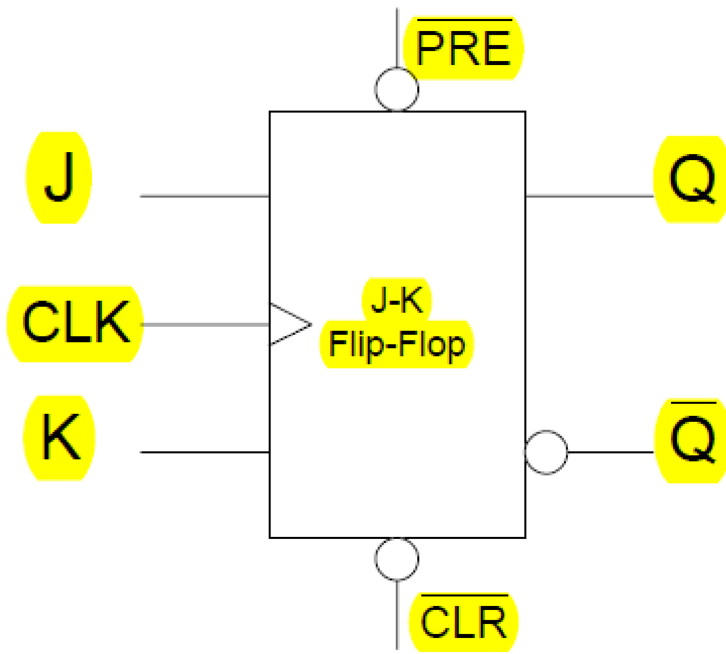

Figure 23.18 Logic Symbol of a J-K flip-flop with Asynchronous inputs

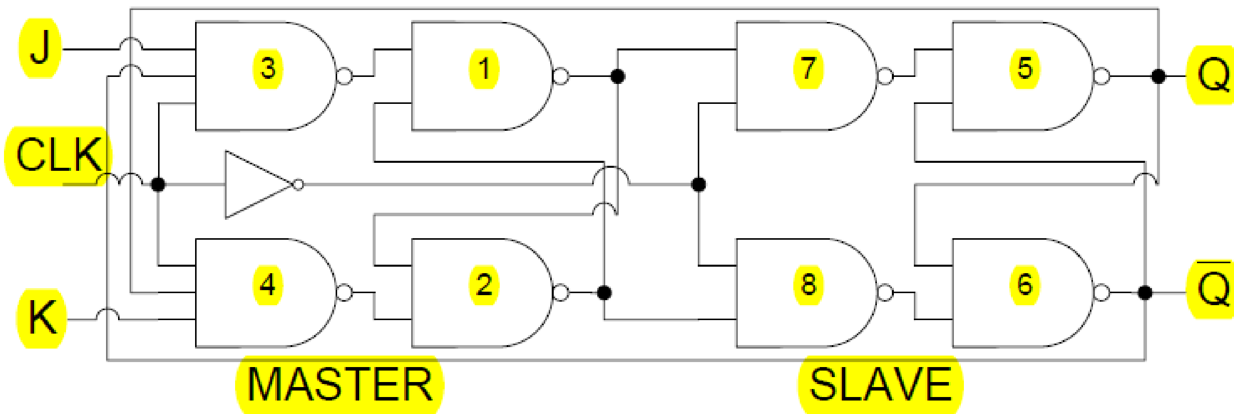

Figure 23.11 Master-Slave flip-flop

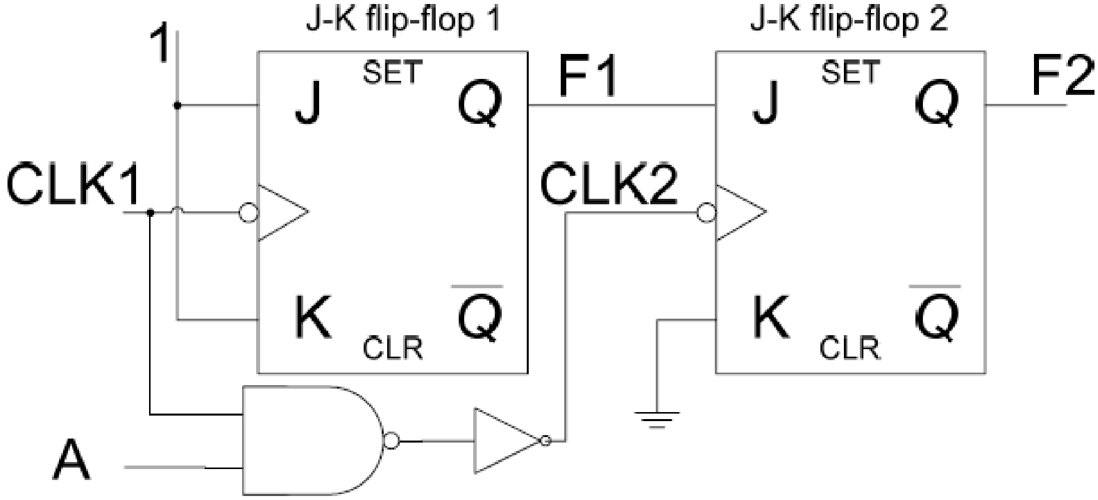

Figure 26.2a Flip-flop circuit with potential timing problem due to Clock Skew

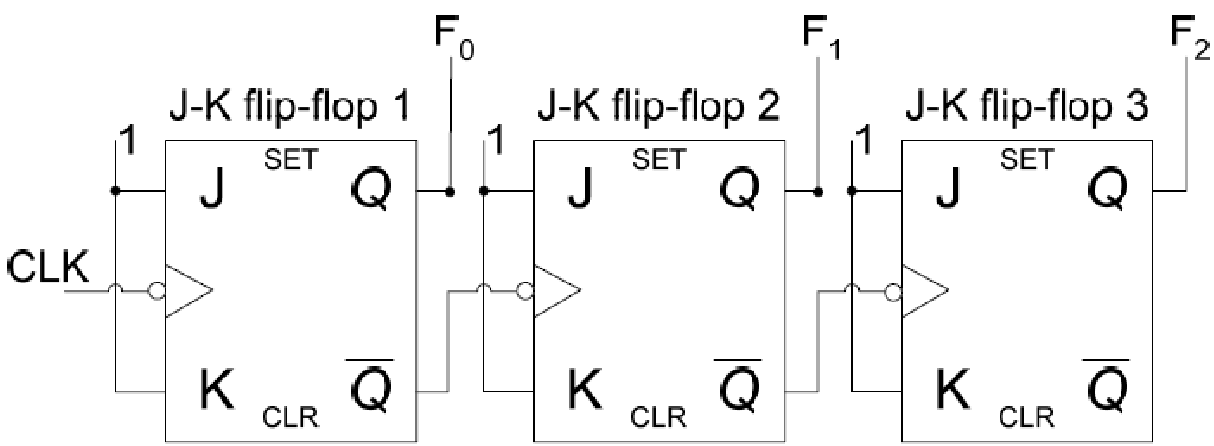

Figure 27.1a 3-bit Asynchronous Down-Counter

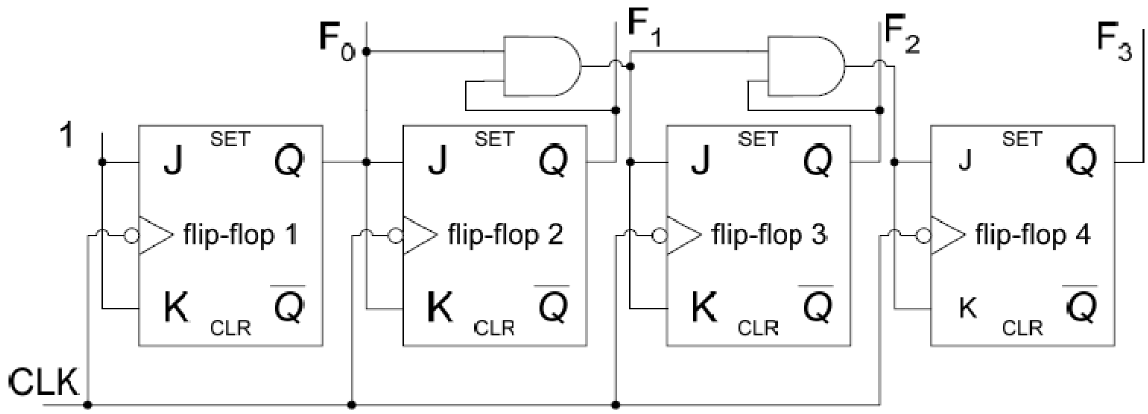

Figure 27.5 4-bit Synchronous Binary Counter

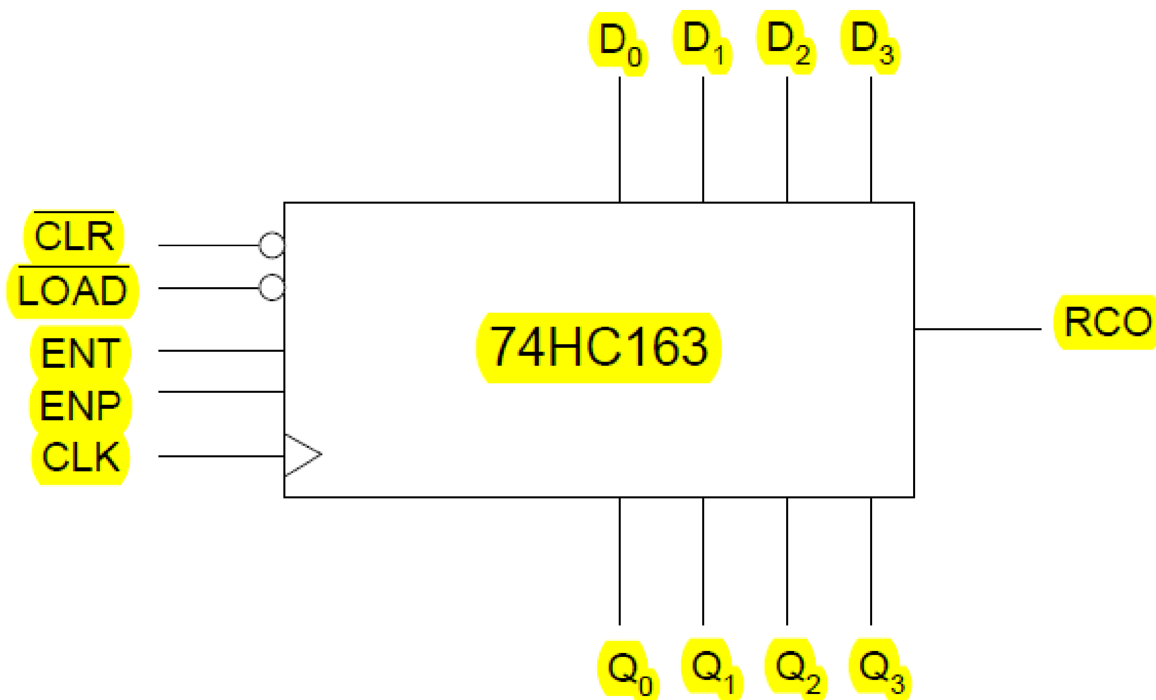

Figure 28.2a 74HC163 4-bit Synchronous Counter

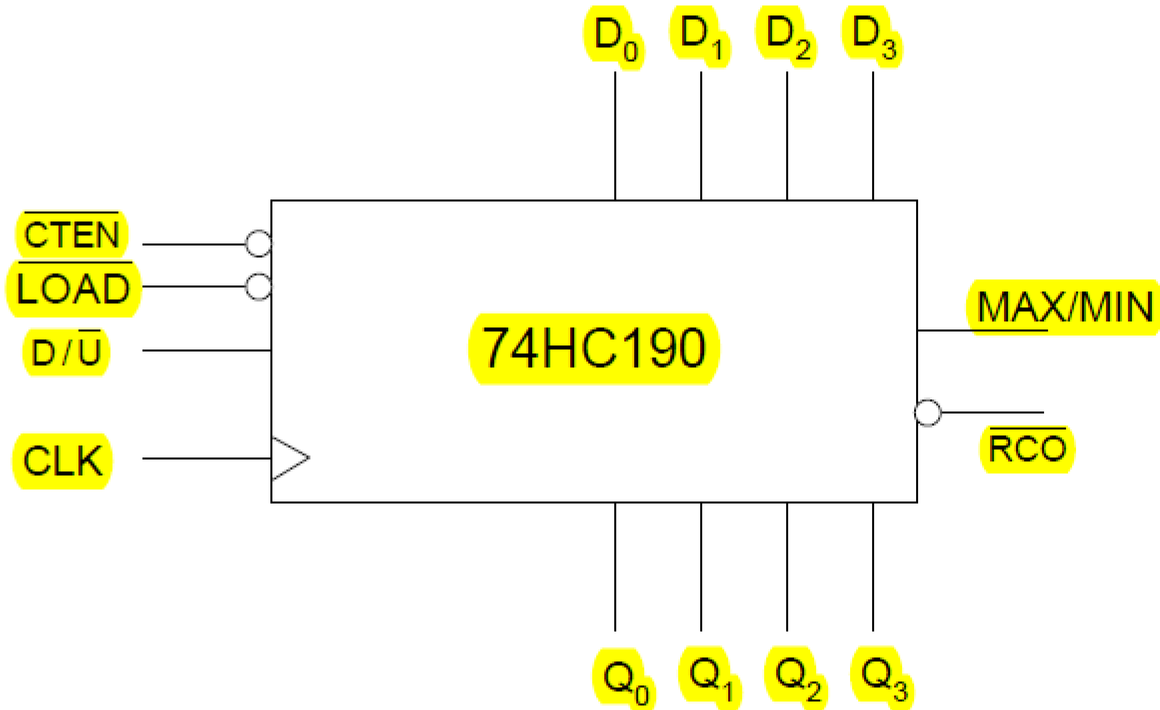

Figure 29.3 74HC190 4-bit Synchronous Up/Down Counter

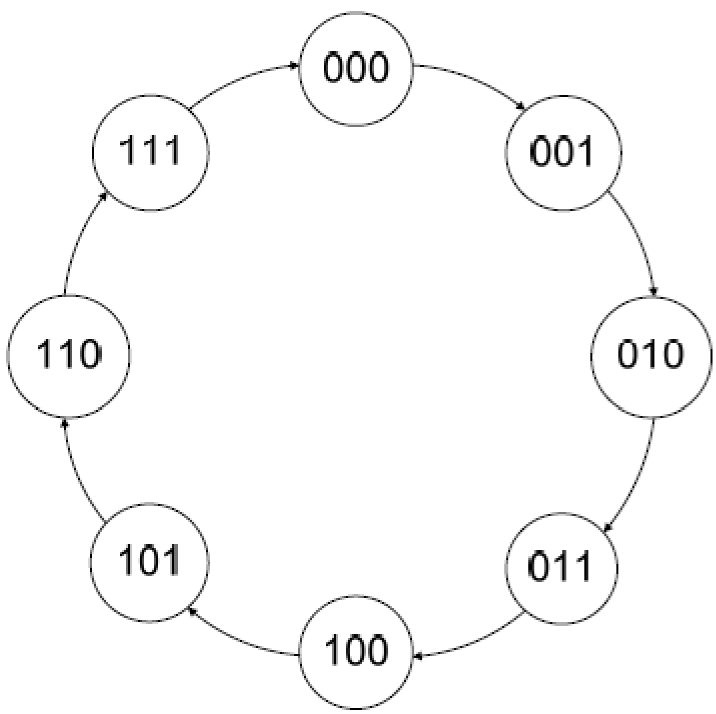

Figure 28.3 State diagram of a 3-bit Up-Counter

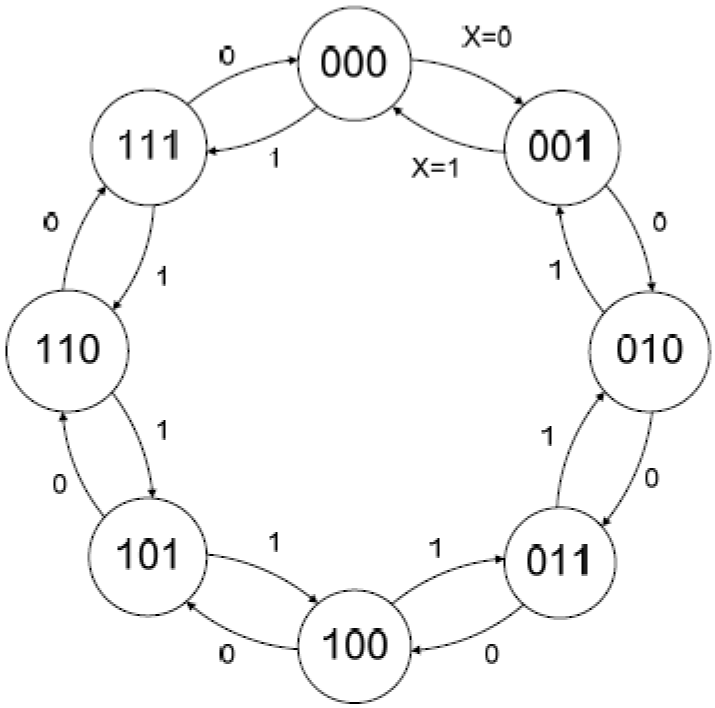

Figure 28.5 State diagram of a 3-bit Up-Counter

Sequential Circuit Implementation

The implementation of the 3-bit synchronous counter based on S-R flip-flops is shown. Figure 31.2

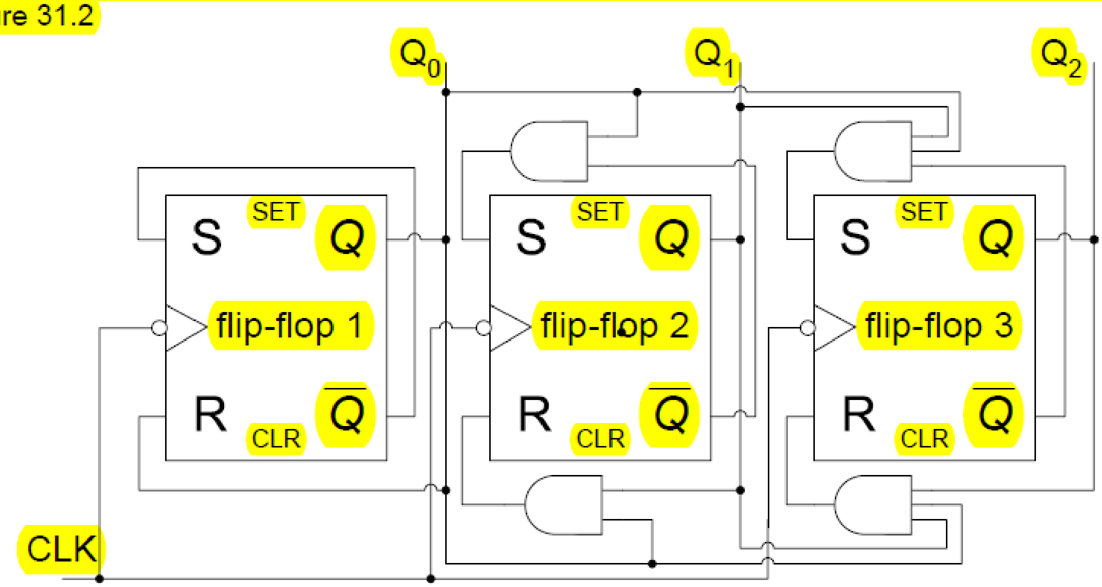

Figure 31.2a S-R flip-flop based implementation of 3-bit Synchronous Counter

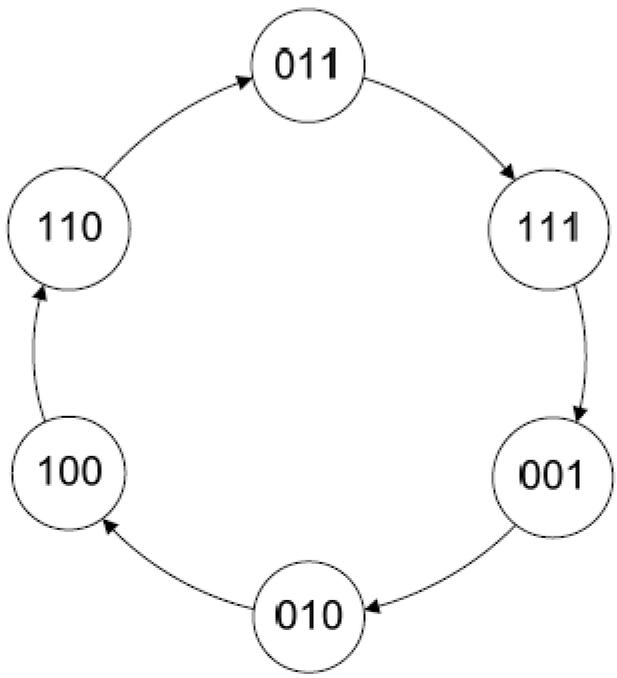

Figure 33.1 State diagram of a Moore Machine

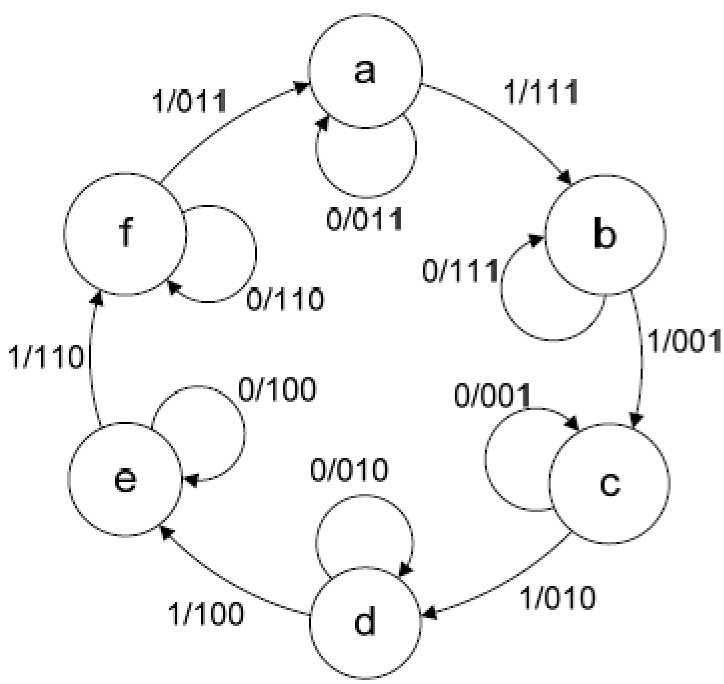

Figure 33.3 State diagram of a Mealy Machine

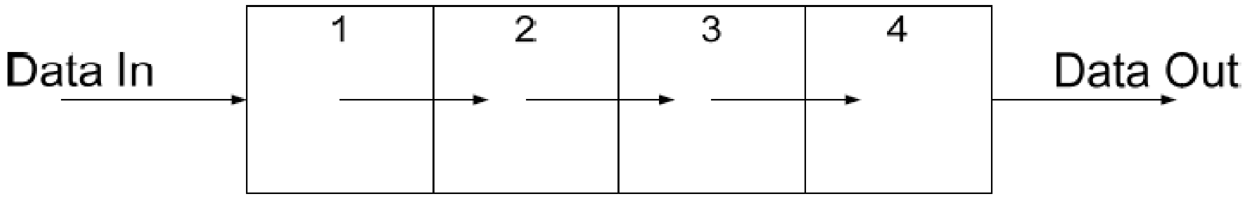

Figure 34.1 Serial In/Serial Right/Serial Out Operation

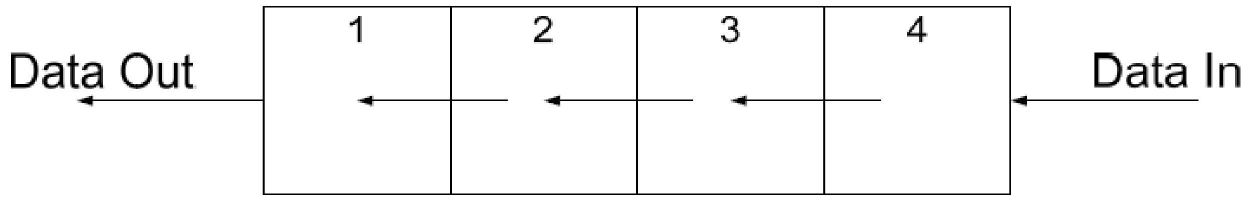

Figure 34.2 Serial In/Serial Left/Serial Out Operation

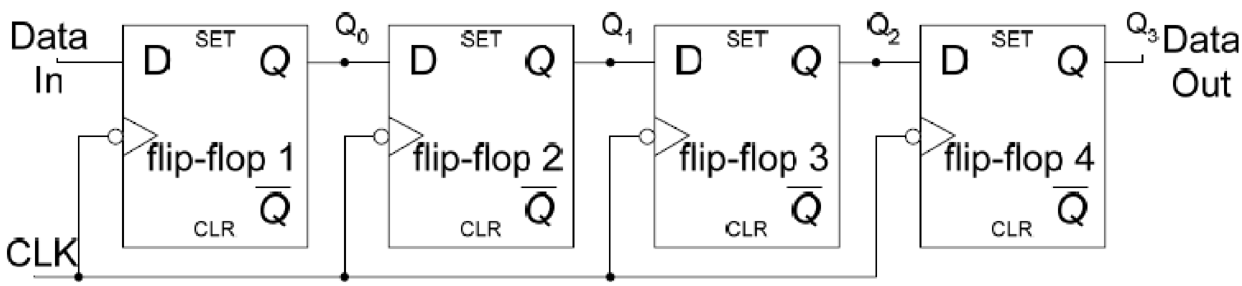

Figure 34.3a Serial In/Shift Right/Serial Out Register

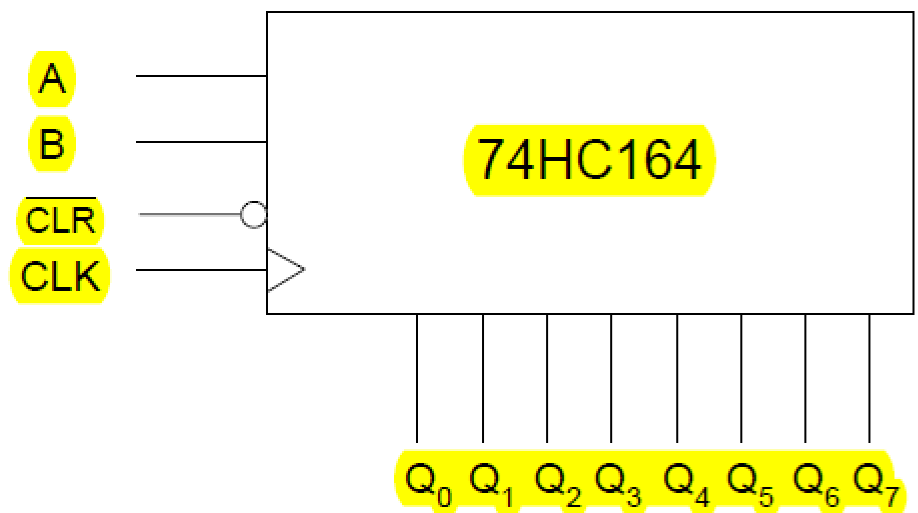

Figure 34.6a 74HC164, 8-bit Serial In/Parallel Out Shift Register

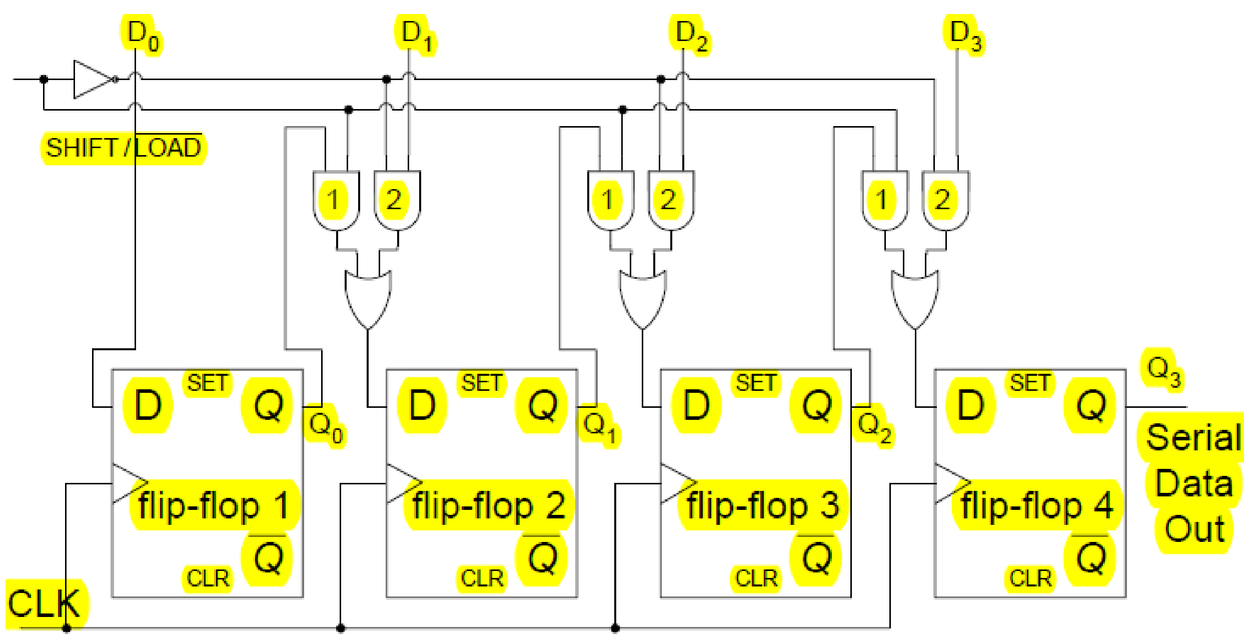

Figure 34.8 4-bit Parallel In/Serial Out Shift register

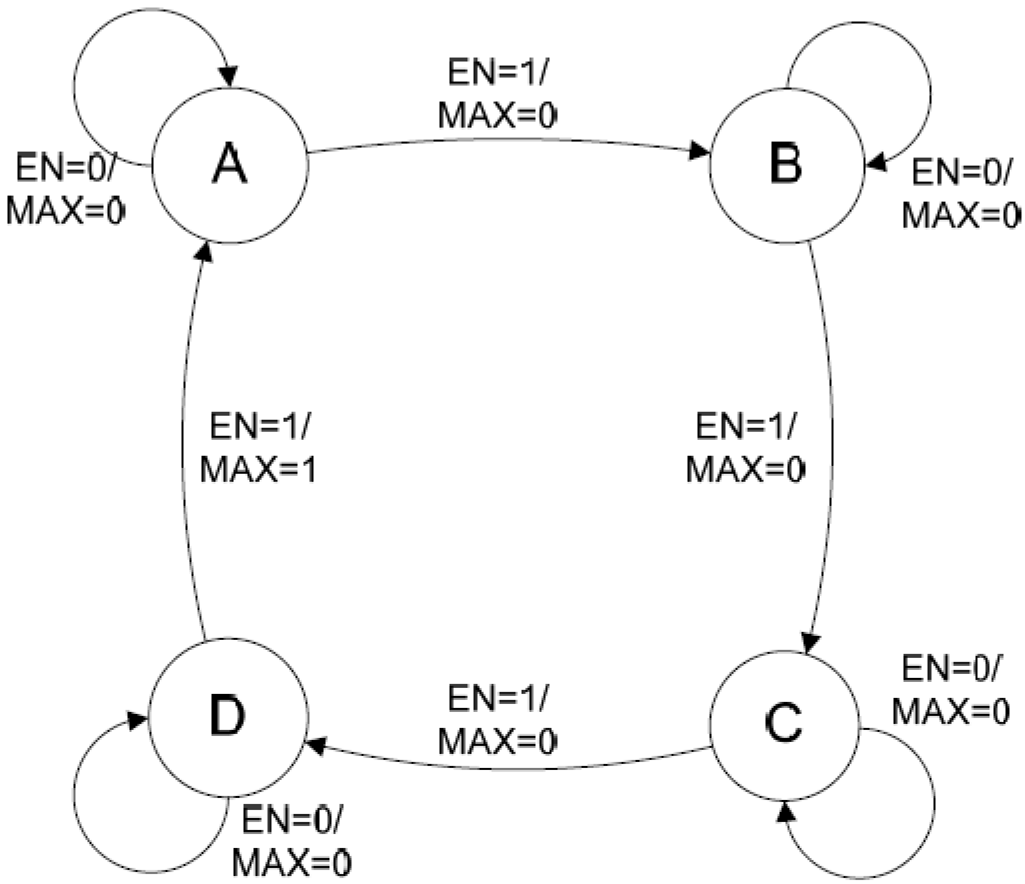

Figure 38.4 State Diagram of a Mealy Machine

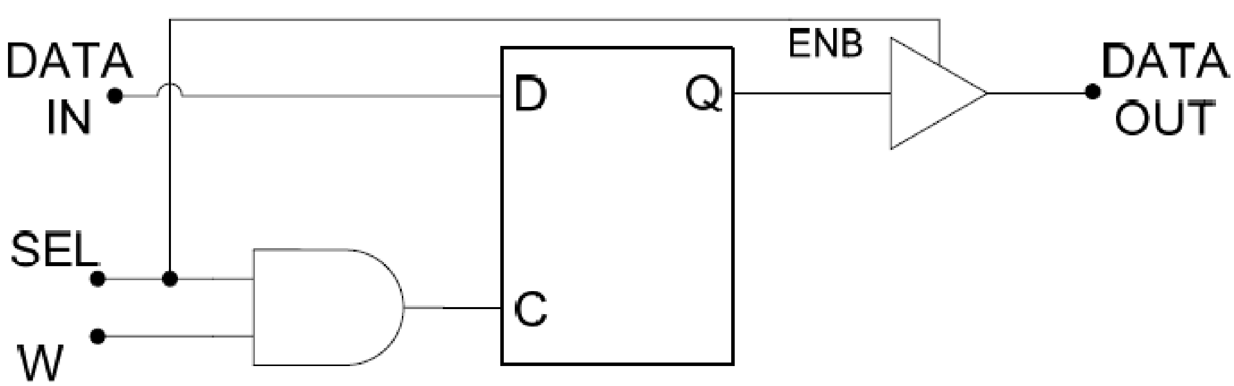

Figure 39.6 Circuit diagram of a Static Memory Cell based on a flip-flop

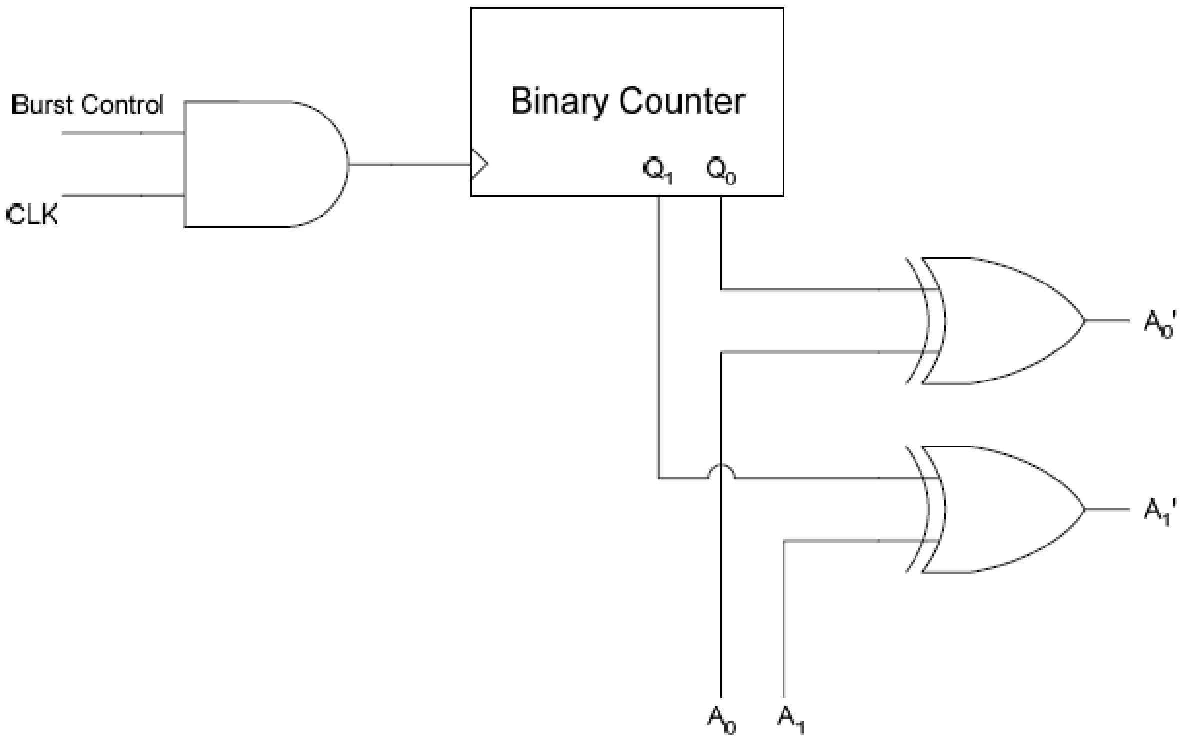

Figure 40.6 Burst Logic Circuit

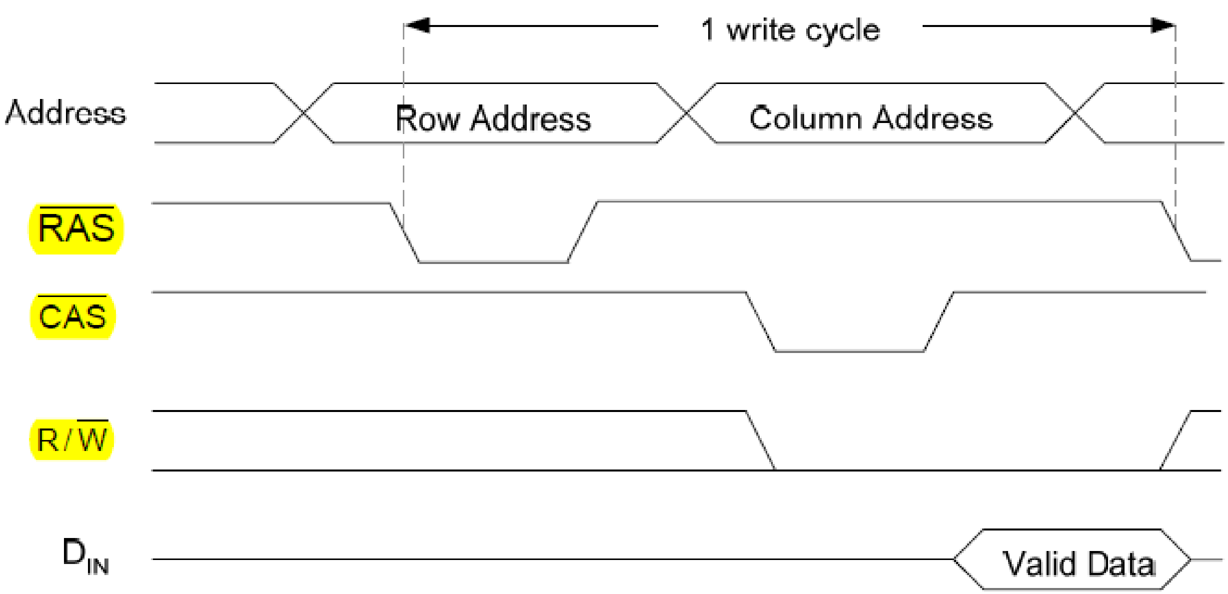

Figure 41.1b DRAM Write Cycle

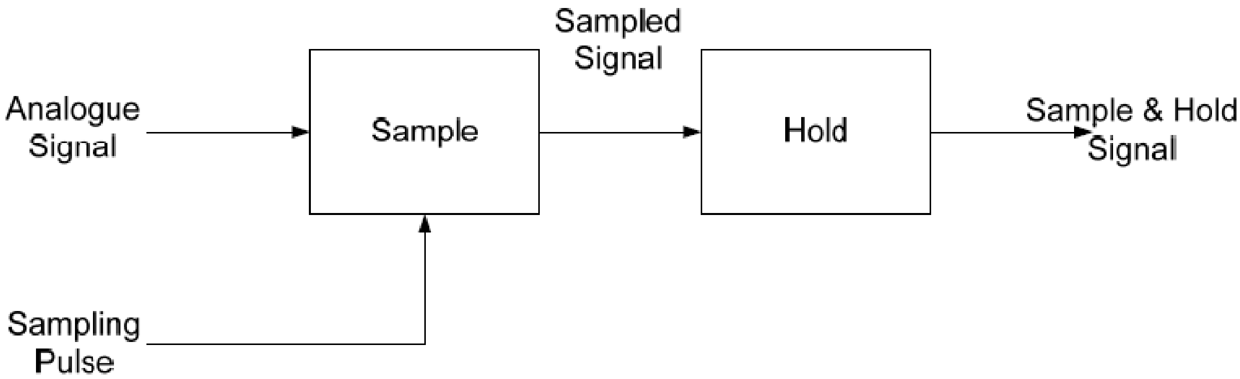

Figure 44.3b Sample and Hold Circuit

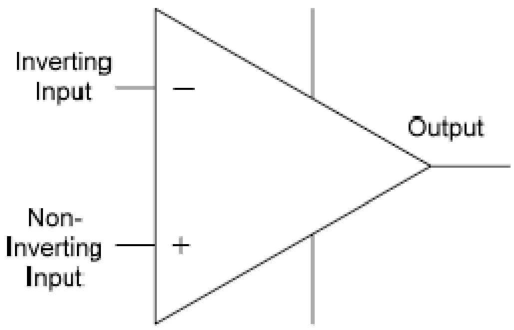

Figure 44.6a Op-Amp

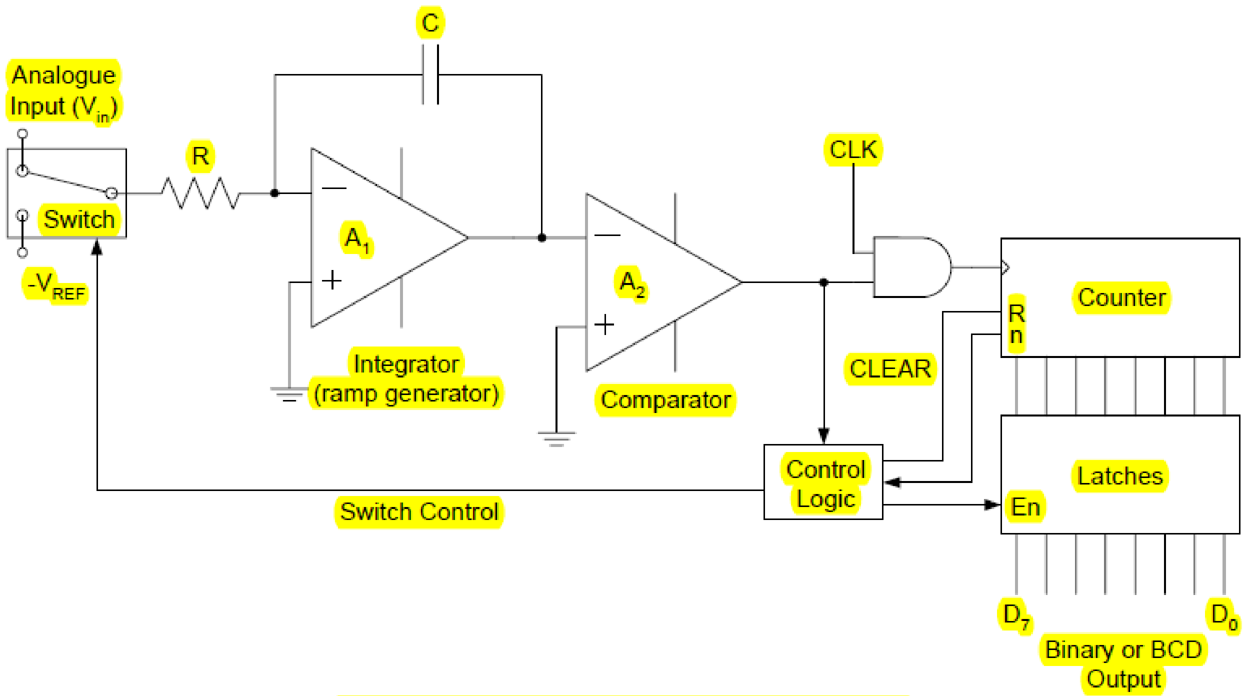

Figure 44.10 Dual-Slope A/D Converter

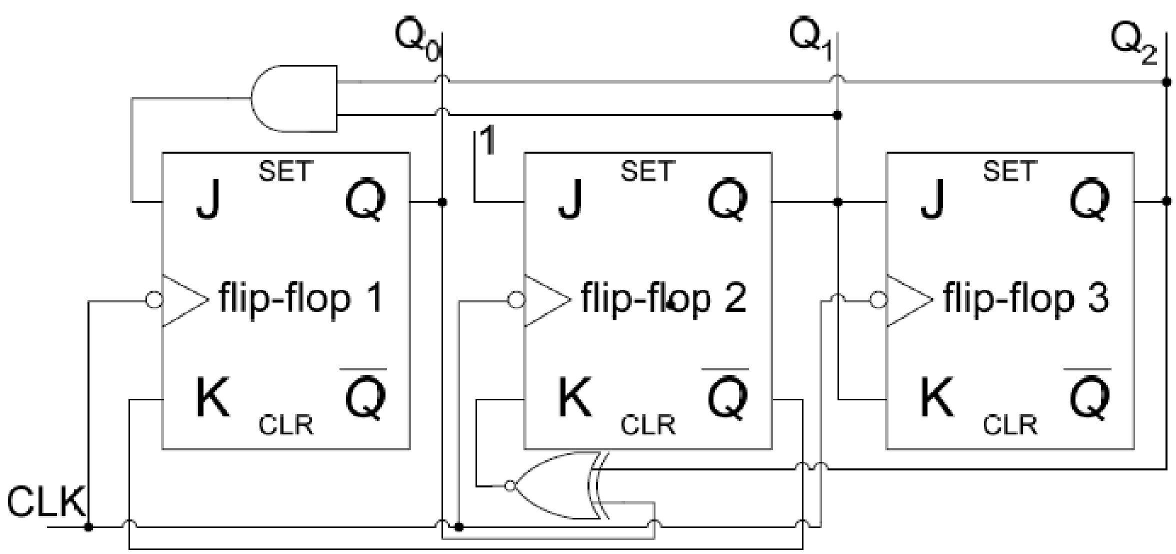

Figure 33.2a Implementation of the Moore Machine

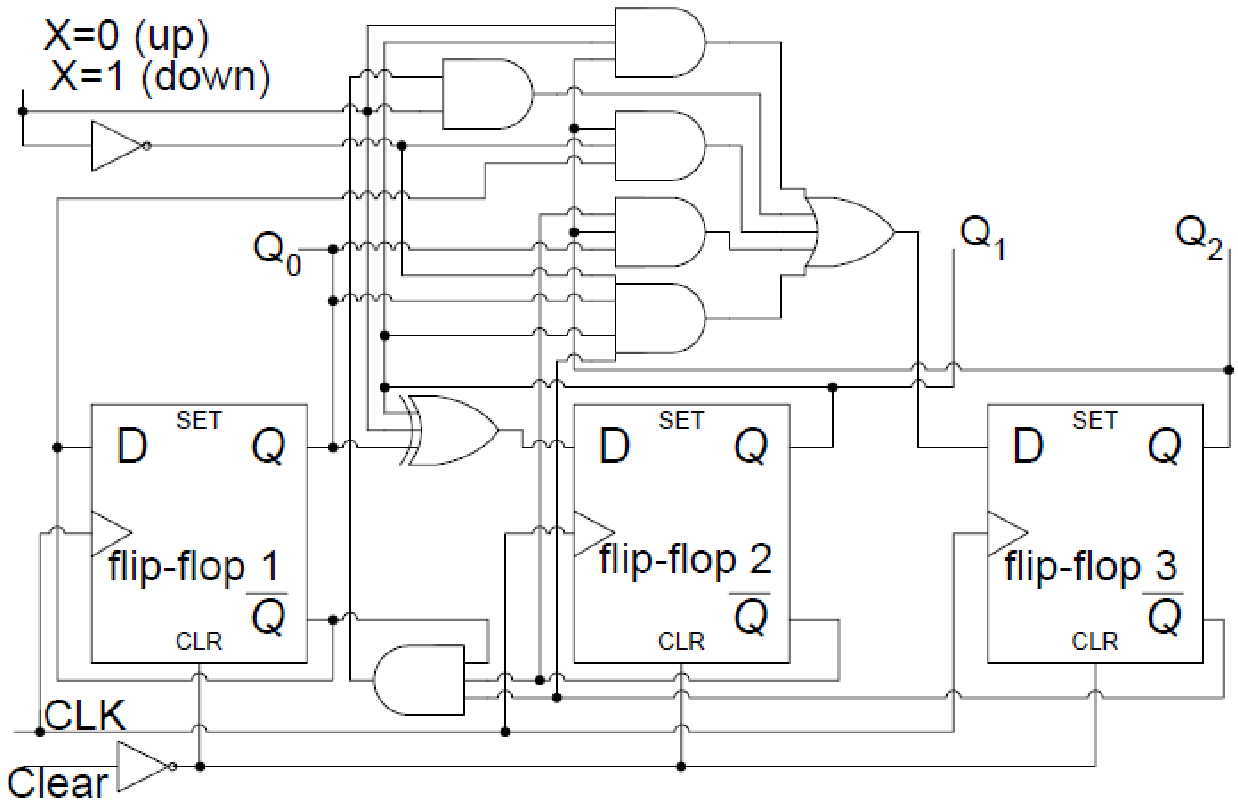

Figure 36.1 3-bit Up/Down Counter

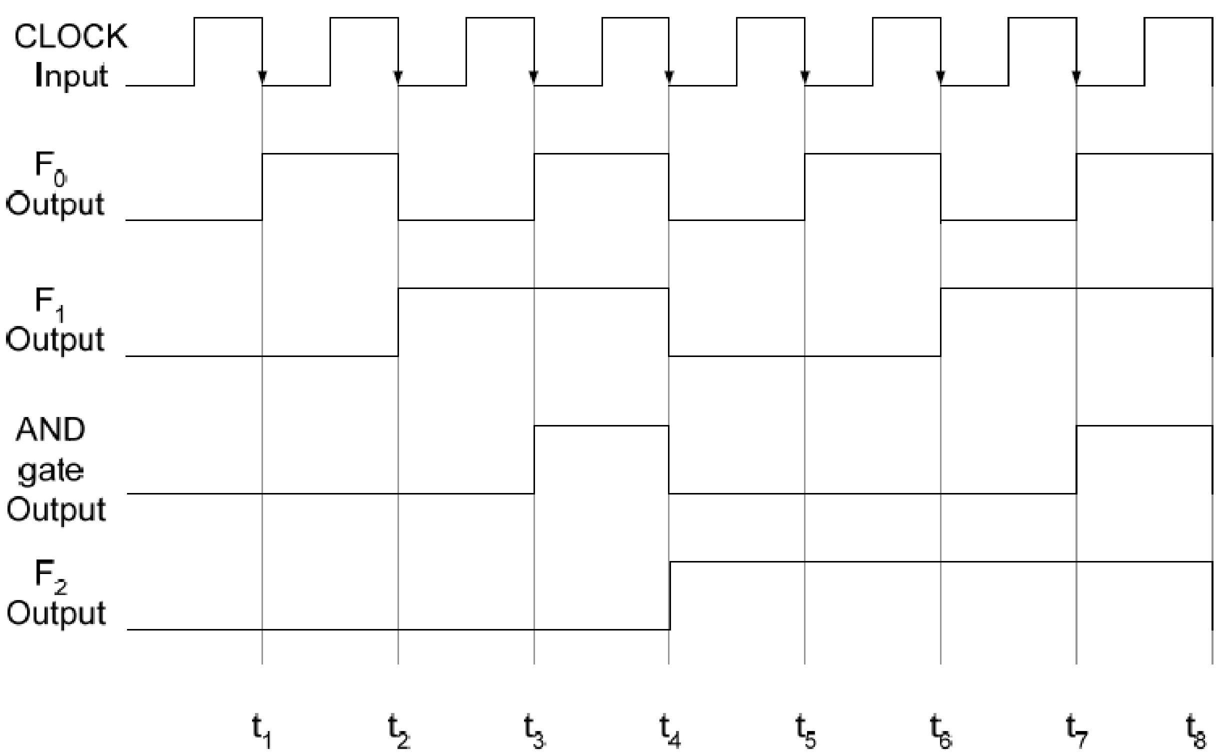

Figure 27.4b Timing diagram of a 3-bit Synchronous Counter

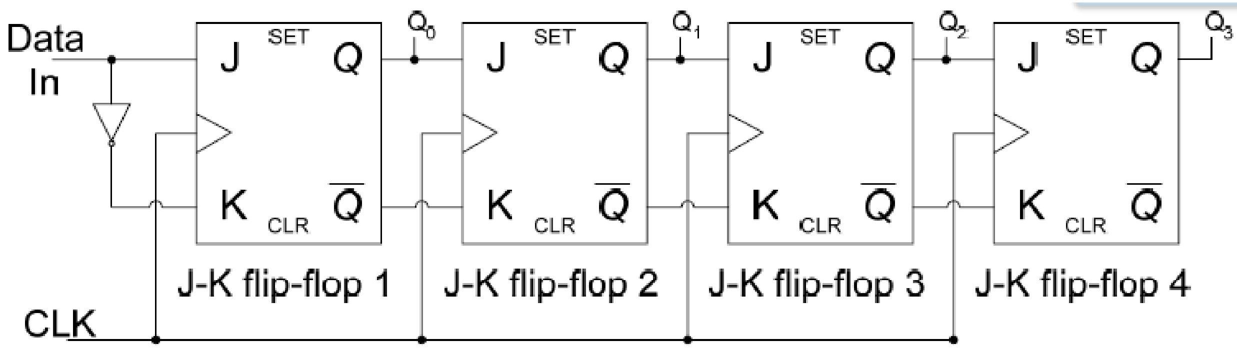

Figure 24.14a 4-bit right shift register