For any of the instructions that are a part of the instruction set of the SRC, there are certain _____required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.

- ▶Register
- **▶Control signals (Page 171)**
- ▶Memory
- ▶None of the given

FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC _____wide.

- ▶8-bits
- ▶16-bits
- **▶32-bits (Page 157)**
- ▶64-bits

What is the instruction length of the FALCON-A processor?

- ▶8-bits
- **▶16-bits (Page 134)**
- ▶32-bits
- ▶64-bits

_____control signals enable the input to the PC for receiving a value that is currently on the internal processor bus.

- **▶LPC (Page 172)**

▶INC4

▶LC

▶I

Which one of the following is a bi-stable device, capable of storing one bit of information?

▶Decoder

▶Flip-Flop (Page 76)

▶Multiplexer

▶Diplexer

Which instruction is used to store register to memory using relative address?

▶ld instruction

▶ldr instruction

▶lar instruction

▶str instruction (Page 48)

Which field of the machine language instruction is the "type of operation" that is to be performed?

▶Op-code (Page 33)

▶CPU registers

▶Momory cells

▶I/O locations

The instruction _____ will load the register R3 with the contenets of the m\emory location M [PC+56]

▶Add R3, 56

▶lar R3, 56

▶ldr R3, 56 (Page 56)

▶str R3, 56

_____ operation is required to change the processor‟s state to a known, defined value.

▶Change

▶Reset (Page 194)

▶Update

▶None of the given

which type of instructions help in changing the flow of the program as and when required?

▶Arithmetic

▶Control (Page 137)

▶Data transfer

▶Floating point

Which one of the following registers holds the address of the next instruction to be executed?

▶Accumulator

▶Address Mask

▶Instruction Register

▶Program Counter (Page 151)

Which one of the following is the memory organization of EAGLE processor?

- **▶8-bits (Page 112)**
- ▶16-bits
- ▶32-bit
- ▶64-bits

The external interface of FALCON-A consists of a _____address bus and _____a data bus.

- ▶8-bit. 8-bit
- **▶16-bit. 16-bit** Click here for detail
- ▶16-bit. 24-bit
- ▶16-bit. 32-bit

What is the instruction length of the SRC processor?

- ▶ 8 bits
- ▶ 16 bits
- **▶ 32 bits (Page 134)**
- ▶ 64 bits

Which one of the following is the memory organization of FALCON-E processor?

- ▶ 28 * 8 bits
- ▶ 216 * 8 bits
- **▶ 232 * 8 bits (Page 124)**
- ▶ 264 * 8 bits

"If P = 1, then load the contents of register R1 into register R2". This statement can be written in RTL as:

- ▶ R1 ¬ R2
- ▶ P: R1 ¬ R2
- ▶ **P: R2 ¬ R1 (not confirms) click here for detail**
- ▶ P: R2 ¬ R1, P: R1 ¬ R2

The instruction ----------will load the register R3 with the contents of the memory location M [PC+56]

- ▶Add R3, 56
- ▶lar R3, 56
- ▶**ldr R3, 56 (Page 47) rep**
- ▶str R3, 56

--------are faster than cache memory

- ▶ Accumulator register
- ▶ **CPU registers (Page 33)**
- ▶ I/O devices
- ▶ ROM

P: R3 ¬ R5 MAR ¬ IR These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?

- ▶ Arrow ¬

- Colon :
- **Comma , (Page 69)**
- Parentheses ()

Prefetching can be considered a primitive form of----------

- **Pipelining (Page 42)**
- Multi-processing
- Self-execution
- Exception

The processor must have a way of saving information about its state or context so that it can be restored upon return from the ----------

- **Exception**
- Function
- Stack
- Thread

Which one of the following circuit design levels is called the gate level?

- **Logic Design Level (Page 22)**
- Circuit Level
- Mask Level
- None of the given

_____ enable the input to the PC for receiving a value that is currently on the internal processor bus.

- **LPC (Page 172) rep**

- INC4
- LC
- Cout

_____ operation is required to change the processor‟s state to a known, defined value.

- Change
- **Reset (Page 194) rep**
- Update
- None of the given

There are _____ types of reset operations in SRC

- **Two (Page 195)**
- Three
- Four
- Five

_____ controller controls the sequence of the flow of microinstructions.

- Multiplexer
- **Microprogram (Page 225)**
- ALU
- None of the given

FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is _____ wide.

- 8-bits

- 24-bits
- **32-bits (Page 157) REP**
- 64-bits

Which one of the following register holds the instruction that is being executed?

- Accumulator
- Address Mask
- **Instruction Register (Page 152)**
- Program Counter

The code size of 2-address instruction is _____.

- 5 bytes
- **7 bytes (Page 36)**
- 3 bytes
- 2 bytes

The data movement instructions _____ data within the machine and to or from input/output devices.

- Store
- Load
- **Move**
- None of Above

Register-register instructions use _____ memory operands out of a total of 3 operands

- 1

► 3

► **0 (Page 37)**

► 2

_____all memory systems are dumb, in that they respond to only two commands: read or write.

► **Virtually Computer Systems Design And Architecture, 2/E Rep**

► Logically

► Physically

► None of Above

Flip-flop is a _____device, capable of storing one bit of Information

► **Bi-stable (Page 76)**

► Unit-stable

► Stable

► Storage

Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?

► **Processor-Memory-Switch level (PMS level) (Page 22)**

► Instruction Set Level

► Register Transfer Level

► None of the given

Which of the instruction is used to load register from memory using a relative address?

- ▶ ld instruction
- ▶ **ldr instruction (Page 47)**
- ▶ lar instruction
- ▶ str instruction

For the _____ type instructions, we require a register to hold the data that is to be loaded from the memory, or stored back to the memory

- ▶ Jump
- ▶ Control
- ▶ **load/store (Page 89)**
- ▶ None of the given

The CPU includes three types of instructions, which have different operands and will need different representations. Which one of the instructions requires two source registers?

- ▶ Jump and branch format instructions
- ▶ Immediate format instructions
- ▶ **Register format instructions**

What is the size of the memory space that is available to FALCON-A processor?

- ▶ 2^8 bytes
- ▶ **2^16 bytes (Page 90)**
- ▶ 2^32 bytes

▶2^64 bytes

How can we refer to an instruction register (IR), of 16 bits (numbered 0 to 15) using RTL?

▶IR<16..0>

▶IR<15..0> (Page 105)

▶IR<16..1>

▶IR<15..1>

Which one of the following portions of an instruction represents the operation to be performed?

▶Address

▶Instruction code

▶Opcode

▶Operand (Page 134)

Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A and source register B) from the following example. ADD R1, R2, R3

▶Opcode= R1, DR=ADD, SA=R2, SB=R3

▶Opcode= ADD, DR=R1, SA=R2, SB=R3 (Page 34)

▶Opcode= R2, DR=ADD, SA=R1, SB=R3

▶Opcode= ADD, DR=R3, SA=R2, SB=R1

What does the word „D" in the „D-flip-Flop" stands for?

▶Data

▶Digital

▶Dynamic

▶Double

Which one of the following is the code size and the Number of memory bytes respectively for a 2-address instruction?

▶4 bytes, 7 bytes

▶7 bytes, 16 bytes (Page 36)

▶10 bytes, 19 bytes

▶13 bytes, 22 bytes

Which of the following can be defined as an address of the operand in a computer type instruction or the target address in a branch type instruction?

▶Base address

▶Binary address

▶Effective address

▶All of the given

Which one of the following is/are the features of Register Transfer Language?

a) It is a symbolic language

b) It is describing the internal organization of digital computers

c) It is an elementary operation performed (during one clock pulse), on the information stored in one or more registers.

d) It is high level language

▶ **(b) only**

► **(a) & (b) only**

► (a) ,(b) & (d)

► (b),(c) & (d)

Motorola MC68000 is an example of ---------microprocessor.

► **CISC (Page 148)**

► RISC

► SRC

► FALCON

Which one of the following registers holds the instruction that is being executed?

► Accumulator

► Address Mask

► **Instruction Register (Page 152) rep**

► Program Counter

The external interface of FALCON-A consists of a _____ data bus.

► 8-bit

► **16-bit (Page 167)**

► 24-bit

► 32-bit

In which one of the following techniques, the time a processor spends waiting for instructions to be fetched from memory is minimized?

► **Perfecting Click here for detail**

▶Pipelining

▶Superscalar operation

▶Speedup

----------is the ability of application software to operate on models of equipment newer than the model for which it was originally developed.

▶Backward compatibility

▶Data migration

▶Reverse engineering

▶Upward compatibility

_____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.

▶INC4

▶LPC

▶PCout (Page 172)

▶LC

Which one of the following registers stores a previously calculated value or a value loaded from the main memory?

▶Accumulator

▶Address Mask

▶Instruction Register

▶Program Counter

Computer system performance is usually measured by the ----------

▶**Time to execute a program or program mix**

▶The speed with which it executes programs

▶Processor‟s utilization in solving the problems

▶Instructions that can be carried out simultaneously

Which one of the following register(s) that is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?

▶Instruction Register

▶Memory address register

▶Memory Buffer Register

▶**Registers A and C (Page 152)**

---------- performs the data operations as commanded by the program instructions.

▶Control

▶**Data path**

▶Structural RTL

▶Timing

Which one of the following register(s) contain(s) the address of the place the CPU wants to work with in the main memory and is/are directly connected to the RAM chips on the motherboard?

▶Instruction Register

▶**Memory address register**

- Memory Buffer Register
- Registers A and C

Questions:

1- Two approaches for control unit.

Answer:- (Page 150)

Additionally, there are two different approaches to the control unit design; it can be either hard-wired or micro-programmed

2- What is micro program?

Answer:- (Page 222)

A collection of microinstructions is called a microprogram. These microprograms generate the sequence of necessary control signals required to process an instruction. These microprograms are stored in a memory called the control store.

3- structural RTL for mov ra, rb

4- Structural RTL and explanation for instruction fetch.

Answer:- (Page 152)

The instruction fetch procedure takes three time steps as shown in the table. During the first time step, T0, address of the instruction is moved to the Memory Address Register (MAR) and value of PC is incremented. In
T1 the instruction is brought from the memory into the Memory Buffer Register (MBR), and the incremented PC is updated. In the third and final timestep of the instruction fetch phase, the instruction from the memory buffer register is written into the IR for execution. What follows the instruction fetch phase, is the instruction execution phase. The number of timing steps taken by the execution phase generally depends on the type and function of instruction. The more complex the instruction and its implementation, the more timing steps it will require completing execution. In the following discussion, we will take a look at various types of instructions, related timing steps requirements and data path implementations of these in terms of the structural RTL.

5. Which register holds the address of the next instruction to be executed in the processor? (2 Marks)

Answer:- (Page 28)

The program counter (PC) that holds the address of the next instruction in memory that is to be executed.

6. What do you know about Machine Exception? (2 Marks)

Answer:- (Page 197)

• Anything that interrupts the normal flow of execution of instructions in the processor is called an exception.

• Exceptions may be generated by an external or internal event such as a mouse click or an attempt to divide by zero etc.

• External exceptions or interrupts are generally asynchronous (do not depend on the system clock) while internal exceptions are synchronous (paced by internal clock)

7. How exception may be generated write the difference between external and internal exceptions? (3marks)

Answer:- (Page 197)

External exceptions or interrupts are generally asynchronous (do not depend on the system clock) while internal exceptions are synchronous (paced by internal clock)

8. Write the structure RTL description for mov instruction (3 Marks)

Answer:- (Page 164)

In mov instruction the data in register rb, which is the source register, is to be moved in the register ra, which is the destination register. In first three steps, mov instruction is fetched. In step T3 the contents of register rb are placed in buffer register C through the ALSU unit while in step T4 the buffer register C transfers the data to register ra through internal uni-bus.

9. Write the structure RTL description for shift instruction? (5 Marks)

Answer:- (Page 157)

Shift instructions are rather complicated in the sense that they require extra hardware to hold and decrement the count. For an ALSU that can perform only single bit shifts, the data must be repeatedly cycled through the ALSU and the count decremented until it reaches zero. This approach presents some timing problems, which can be overcome by employing multiple-bit shifts using a barrel shifter.

10 - Write a structural RTL for Shift instruction for Uni-Bus data path implementation.

shiftr ra, rb, c1 [5 Marks]

11 - Write down one Advantage and Disadvantage of Microprogramming? [3 Marks]

Answer:-

Advantages Great sophistication in the user instruction set can be achieved for relatively low cost. Adding new instructions is cheap.

Disadvantages For a simple machine, the extra hardware needed for the control store and sequencer may be more complex than hardwiring.

12 - Difference between Memory Address Register and Memory Buffer Register? [2 Marks]

Answer:- (Page 151)

MAR

The Memory Address Register takes input from the ALSU as the address of the memory location to be accessed and transfers the memory contents on that location onto the memory sub-system.

MBR

The Memory Buffer Register has a bi-directional connection with both the memory sub-system and the registers and ALSU. It holds the data during its transmission to and from memory.

13. Which register holds the address of the next instruction to b executed in the processor? 2 marks

14. How exception may b generated write the difference between external and internal exceptions? 3 marks

15. Write the two ways to increase the number of instruction in a given time by the processor? Explain each one briefly? 5 marks

Answer:- (Page 219)

There are two ways to increase the number of instructions executed in a given time by a processor

Increasing the clock speed

• Increasing the clock speed is an IC design issue and depends on the advancements in chip technology.

• The computer architect or logic designer can not thus manipulate clock speeds to increase the throughput of the processor.

Increasing parallel execution of instructions

The computer architect cannot increase the clock speed of a microprocessor however he/she can increase the number of instructions processed per unit time. In pipelining we discussed that a number of instructions are executed in a staggered fashion, i.e. various instructions are simultaneously executing in different segments of the pipeline. Taking this concept a step further we have multiple data paths hence multiple pipelines can execute simultaneously.