

**Cs-302 Important Mid Term**  
**Mcq's Solution 100% Correct :**  
**Solve By Vu-Topper RM!!**

وَعَزُّ مَنْ تَشَاءُ وَتَذَلُّ مَنْ تَشَاءُ



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**0322-4021365**

**Question No:1** (Marks:1) **Vu-Topper RM**  
Combinational Logic is used for combinational circuits, where as Registered Logic is based on -----circuits.  
**Sequential circuits** 192

**Question No:2** (Marks:1) **Vu-Topper RM**  
A standard interface for programming the In-System PLD consists of  
**4-wire** 194

**Question No:3** (Marks:1) **Vu-Topper RM**  
The 4-bit ALU (74XX381) only has three function select inputs allowing only \_\_\_\_ different arithmetic and logic functions.  
**8** 147

**Question No:4** (Marks:1) **Vu-Topper RM**  
Which of the following is the MSI version of the Look-Ahead Carry Generator, which provides identical inputs and outputs except for the C4 output?  
**74XX182** 151

**Question No:5** (Marks:1) **Vu-Topper RM**  
The PROM consists of a fixed non-programmable \_\_\_\_\_ Gate array configured as a decoder.  
**AND** 182

**Question No:6** (Marks:1) **Vu-Topper RM**  
Each Octal Number digit can represent a \_\_\_\_\_ Binary Number  
**3-bit** 31

**Question No:7** (Marks:1) **Vu-Topper RM**  
The simplified expressions using either of the two K-maps are-----?  
**Identical** 89

**Question No:8** (Marks:1) **Vu-Topper RM**  
The \_\_\_\_\_ gate and \_\_\_\_\_ gate implementation connected at the B input of the 4-bit Adder  
**AND and OR** 146

**Question No:9** (Marks:1) **Vu-Topper RM**  
In 16-Input Multiplexer, the four outputs are connected together through a 4-input \_\_\_\_\_ gate.?  
**OR** 171

**Question No:10** (Marks:1) **Vu-Topper RM**  
\_\_\_\_\_ is invalid number of cells in a single group formed by the adjacent cells in K-map  
**12** G

**Question No:11** (Marks:1) **Vu-Topper RM**  
XOR is an abbreviation of\_\_\_\_\_  
**Exclusively-OR** G

**Question No:12** (Marks:1) **Vu-Topper RM**  
For a 3-to-8 decoder how many 2-to-4 decoders will be required?  
**Decoders** G

**Question No:13** (Marks:1) **Vu-Topper RM**  
The expression  $F=A.B.C$  describes the operation of three bits \_\_\_\_\_ Gate.  
**OR** G

**Question No:14** (Marks:1) **Vu-Topper RM**  
How many sets of AND-OR based circuit are used to allow complemented and un-complemented B input to be applied at the B inputs of the two 4-bit Adders?  
**Two** 146

**Question No:15** (Marks:1) **Vu-Topper RM**  
The product terms in Standard SOP are called\_\_\_\_\_  
**Minterms** 85

**Question No:16** (Marks:1) **Vu-Topper RM**  
“The complement of a product of variables is equal to the sum of the complements of the variables.” is known as:  
**Demorgan’s First Theorem** 74

**Question No:17** (Marks:1) **Vu-Topper RM**  
Basic function of a Comparator is to \_\_\_\_\_ two binary quantities.  
**Compare** 153

**Question No:18** (Marks:1) **Vu-Topper RM**  
The \_\_\_\_\_ output has the output of the OR gate connected through an XOR gate to the tri-state buffer.  
**Programmed Polarity** 186

**Question No:19** (Marks:1) **Vu-Topper RM**  
Power consumption in TTL is \_\_\_\_\_ as compared to CMOS.  
**Higher than** 61

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**Question No:20** (Marks:1) **Vu-Topper RM**  
enable input of the decoder when set to 1 disables the decoder and the multiplexers.

**G** 171

**Question No:21** (Marks:1) **Vu-Topper RM**  
A Karnaugh Map is organized in the form of a(an)\_\_\_\_\_.

**Array** 89

**Question No:22** (Marks:1) **Vu-Topper RM**  
Gate is used in circuits to generate the 1's Complement of a number by inverting all its bits.

**NOT** 44

**Question No:23** (Marks:1) **Vu-Topper RM**  
The OR Gate performs a Boolean\_\_\_\_\_function

**Addition**  
Subtraction

**Question No:24** (Marks:1) **Vu-Topper RM**  
The expression  $F=A+B+C$

**OR**  
AND

**Question No:25** (Marks:1) **Vu-Topper RM**  
In Caveman number system the value "2" is represented by symbol \_\_\_\_\_

**>** 11

**Question No:26** (Marks:1) **Vu-Topper RM**  
A SOP expression having a domain of 3 variables will have a truth table having \_\_\_\_\_ combinations of inputs and corresponding output values.

2  
**4**

**Question No:27** (Marks:1) **Vu-Topper RM**  
A standard SOP form has \_\_\_\_\_terms that have all the variables in the domain of the expression.

Sum  
**Product**

**Question No:28** (Marks:1) **Vu-Topper RM**  
Caveman number system is Base\_\_\_\_\_number

2  
**5**

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**Question No:29**

**(Marks:1)**

**Vu-Topper RM**

74ALS stands for \_\_\_\_\_

**Advanced Low-Power Schottky TTL**

Advanced Low-propagation Schottky TTL

**Question No:30**

**(Marks:1)**

**Vu-Topper RM**

The ANSI/IEEE Standard 754 defines a \_\_\_\_\_ Single-Precision Floating

Pointing format for binary numbers.

**32-bit**

64-bit

**Question No:31**

**(Marks:1)**

**Vu-Topper RM**

The output of an AND gate is one when

**All of the input are one**

Any of the input is one

**Question No:32**

**(Marks:1)**

**Vu-Topper RM**

Excess-8 code assigns \_\_\_\_\_ to “-8”

1000

**0000**

**Question No:33**

**(Marks:1)**

**Vu-Topper RM**

\_ is invalid number of cells in a single group formed by the adjacent cells in K-map

**12**

16

**Question No:34**

**(Marks:1)**

**Vu-Topper RM**

The cell marked 6 in 4-variable K-Map represent minterm 6 or the maxterm 6

having the following binary value of variables A, B, C and D.

A=1, B=0, C=0, D=1

**A=0, B=1, C=1, D=0**

**Question No:35**

**(Marks:1)**

**Vu-Topper RM**

The hexadecimal value “FD” is equivalent to binary value \_\_\_\_\_

11011111

**11111101**

**Question No:36**

**(Marks:1)**

**Vu-Topper RM**

The Extended ASCII Code (American Standard Code for Information

Interchange) is a \_\_\_\_\_ code

**7bit**

8bit

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**Question No:37** (Marks:1) **Vu-Topper RM**  
NOR Gate can be used to perform the operation of AND, OR and NOT Gate  
**True**  
False

**Question No:38** (Marks:1) **Vu-Topper RM**  
The 4-bit 2's complement representation of "-7" is \_\_\_\_\_  
**1001** 23

**Question No:39** (Marks:1) **Vu-Topper RM**  
The ABEL symbol for "OR" operation is  
**#**

**Question No:40** (Marks:1) **Vu-Topper RM**  
A standard SOP form has \_\_\_\_\_ terms that have all the variables in the domain of the expression.  
**Sum** 85

**Question No:41** (Marks:1) **Vu-Topper RM**  
How many data select lines are required for selecting eight inputs?  
**3**

**Question No:42** (Marks:1) **Vu-Topper RM**  
If two adjacent 1s are detected in the input, the output is set to high, input combinations will be  
**0011**

**Question No:43** (Marks:1) **Vu-Topper RM**  
The 4-variable Karnaugh Map (K-Map) has \_\_\_\_\_ rows and \_\_\_\_\_ columns  
**4,4**

**Question No:44** (Marks:1) **Vu-Topper RM**  
The boolean expression  $A + B' + C$  is  
**a sum term**

**Question No:45** (Marks:1) **Vu-Topper RM**  
the boolean expression  $AB'CD$  is  
**a product term**

**Question No:46** (Marks:1) **Vu-Topper RM**  
Don't care conditions are marked as \_\_\_\_\_ in the output column of the function table  
**X**

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**Question No:47** (Marks:1) **Vu-Topper RM**  
An example of SOP expression is **both (a) and (b)**

**Question No:48** (Marks:1) **Vu-Topper RM**  
For a Standard SOP expression, a \_\_\_\_\_ is placed in the cell corresponding to the product term (Minterm) present in the expression.  
**1**

**Question No:49** (Marks:1) **Vu-Topper RM**  
Multiplexers are also known as \_\_\_\_\_.  
**Data Selectors**

**Question No:50** (Marks:1) **Vu-Topper RM**  
Sum term (Max term) is implemented using \_\_\_\_\_ gates  
**OR**

**Question No:51** (Marks:1) **Vu-Topper RM**  
The number "1259" may belong to \_\_\_\_\_ number system.  
**Binary or Hexadecimal system**

**Question No:52** (Marks:1) **Vu-Topper RM**  
If two numbers in BCD representation generate an invalid BCD number then the binary \_\_\_\_\_ is added to the result  
**1111**

**Question No:53** (Marks:1) **Vu-Topper RM**  
"1101" in signed representation is equivalent to \_\_\_\_\_  
**13**

**Question No:54** (Marks:1) **Vu-Topper RM**  
TTL based devices work with a dc supply of \_\_\_\_\_ Volts  
**+5**

**Question No:55** (Marks:1) **Vu-Topper RM**  
In decimal value "275" the weight of the digit "7" is \_\_\_\_\_  
**100**

**Question No:56** (Marks:1) **Vu-Topper RM**  
The decimal "10" will have an octal equivalent \_\_\_\_\_  
**9 5**

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**Question No:57** (Marks:1) **Vu-Topper RM**  
Caveman number system is Base \_\_\_\_\_ number system  
**5**

**Question No:58** (Marks:1) **Vu-Topper RM**  
How many bits must each word have in one-to-four line de-multiplexer to be implemented using a memory?  
**1 bits**

**Question No:59** (Marks:1) **Vu-Topper RM**  
The total amount of memory is depends upon \_\_\_\_\_  
**The size of the address bus of the microprocessor**

**Question No:60** (Marks:1) **Vu-Topper RM**  
\_\_\_\_\_ can be determined the Instability condition.  
**logic diagram**

**Question No:61** (Marks:1) **Vu-Topper RM**  
If we add an inverter at the output of AND gate, what function is produced?  
**NAND**

**Question No:62** (Marks:1) **Vu-Topper RM**  
Which is also known as coincidence detector?  
**AND gate**

**Question No:63** (Marks:1) **Vu-Topper RM**  
Transition table include \_\_\_\_\_  
**squares**

**Question No:64** (Marks:1) **Vu-Topper RM**  
For every possible combination of logical states in the inputs, which table shows the logical state of a digital circuit output?  
**Truth table**

**Question No:65** (Marks:1) **Vu-Topper RM**  
Stack is an acronym for \_\_\_\_\_  
**LIFO memory**

**Question No:66** (Marks:1) **Vu-Topper RM**  
When an Asynchronous sequential circuit changes two or more binary states variables a Condition occurs called \_\_\_\_\_  
**Race condition**

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**Question No:67** (Marks:1) **Vu-Topper RM**  
positive OR gate is also a negative  
**AND gate**

**Question No:68** (Marks:1) **Vu-Topper RM**  
Time delay device is memory element of \_\_\_\_\_  
**asynchronous circuits**

**Question No:69** (Marks:1) **Vu-Topper RM**  
Boolean algebra is also called  
a) arithmetic algebra  
b) switching algebra  
c) **Both A & B**

**Question No:70** (Marks:1) **Vu-Topper RM**  
Boolean function must be brought into \_\_\_\_\_ To perform product of max  
terms  
**OR terms**

**Question No:71** (Marks:1) **Vu-Topper RM**  
The binary number 10101 is equivalent to the decimal number \_\_\_\_\_.  
**21**

**Question No:72** (Marks:1) **Vu-Topper RM**  
The domain of expression  $ABCD + AB + CD + B$  is—  
**B only**

**Question No:73** (Marks:1) **Vu-Topper RM**  
The Boolean expression  $A BC D$  is—  
**Sum term**

**Question No:74** (Marks:1) **Vu-Topper RM**  
The universal gate is \_\_\_\_\_.  
**NAND gate**

**Question No:75** (Marks:1) **Vu-Topper RM**  
According to boolean algebra absorption law, which of the following is correct?  
 **$xy+y=x$**

**Question No:76** (Marks:1) **Vu-Topper RM**  
A Boolean function may be transformed into  
**logical diagram**

- Question No:78** (Marks:1) **Vu-Topper RM**  
The inverter is \_\_\_\_\_  
**NOT gate**
- Question No:79** (Marks:1) **Vu-Topper RM**  
The resulting circuit of a NAND gate are connected together is \_\_\_\_\_  
**NOT gate**
- Question No:80** (Marks:1) **Vu-Topper RM**  
 $x*y = y*x$  is the  
**identity element**
- Question No:81** (Marks:1) **Vu-Topper RM**  
Minterms are also called  
**standard product**
- Question No:82** (Marks:1) **Vu-Topper RM**  
OR gate and \_\_\_\_\_ will form The NOR gate?  
**NOT gate**
- Question No:83** (Marks:1) **Vu-Topper RM**  
The NAND gate is AND gate followed by .....  
**NOT gate**
- Question No:84** (Marks:1) **Vu-Topper RM**  
Max terms are also called\_\_\_\_\_  
**standard sum**
- Question No:85** (Marks:1) **Vu-Topper RM**  
In Boolean algebra Multiplicative inverse is  
**a**
- Question No:86** (Marks:1) **Vu-Topper RM**  
By the repeated use of \_\_\_\_\_Digital circuit can be made  
**NAND gates**
- Question No:87** (Marks:1) **Vu-Topper RM**  
The only function of NOT gate is\_\_\_\_\_ of the following.  
**Invert input signal**
- Question No:88** (Marks:1) **Vu-Topper RM**  
Boolean algebra is defined as a set of\_\_\_\_\_  
**two values**

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**Question No:89** (Marks:1) **Vu-Topper RM**  
First operator precedence for evaluating Boolean expressions is  
**Parenthesis**

**Question No:90** (Marks:1) **Vu-Topper RM**  
The output is \_\_\_\_\_ When an input signal 1 is applied to a NOT gate  
**0**

**Question No:91** (Marks:1) **Vu-Topper RM**  
The bar sign (-) indicates \_\_\_\_\_ In Boolean algebra?  
**NOT operation**

**Question No:92** (Marks:1) **Vu-Topper RM**  
The value of n is \_\_\_\_\_ when the resolution of an n bit DAC with a maximum input of 5 V is 5 mV.  
**10**

**Question No:93** (Marks:1) **Vu-Topper RM**  
2's complement of binary number 0101 is \_\_\_\_\_  
**1011**

**Question No:94** (Marks:1) **Vu-Topper RM**  
An OR gate has 4 inputs. The output is ..... When One input is high and the other three are low.  
**High**

**Question No:95** (Marks:1) **Vu-Topper RM**  
To convert BCD to seven segments \_\_\_\_\_ device is used.  
**Decoder**

**Question No:96** (Marks:1) **Vu-Topper RM**  
Decimal number 10 is equal to binary number \_\_\_\_\_.  
**1010**

**Question No:97** (Marks:1) **Vu-Topper RM**  
In 2's complement representation the number 11100101 represents the decimal number \_\_\_\_\_.  
**-27**

**Question No:98** (Marks:1) **Vu-Topper RM**  
BCD input 1000 is fed to a 7 segment display through a BCD to 7 segment decoder/driver. The segments which will lit up are \_\_\_\_\_.  
**All**

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**Question No:99** (Marks:1) **Vu-Topper RM**  
A decade counter skips \_\_\_\_\_.  
**binary states 1010 to 1111**

**Question No:100** (Marks:1) **Vu-Topper RM**  
\_\_\_\_\_Number of States A ring counter with 5 flip flops will have?  
**5**

**Question No:101** (Marks:1) **Vu-Topper RM**  
Positive edge-triggered flip-flop changes its state when \_\_\_\_\_  
**Low-to-high transition of clock**

**Question No:102** (Marks:1) **Vu-Topper RM**  
If  $S=1$  and  $R=1$ , for negative edge triggered flip-flop then  $Q(t+1) =$  \_\_\_\_\_  
**Invalid**

**Question No:103** (Marks:1) **Vu-Topper RM**  
A 5-variable karnaugh map has  
**Thirty two cells**

**Question No:104** (Marks:1) **Vu-Topper RM**  
8-bit parallel data can be converted into serial data by using \_\_\_\_\_ multiplexer  
**8-to-1 ok 175**

**Question No:105** (Marks:1) **Vu-Topper RM**  
In asynchronous digital systems all the circuits change their state with respect to a common clock  
**False**

**Question No:106** (Marks:1) **Vu-Topper RM**  
Divide-by-32 counter can be achieved by using  
**Flip-Flop and DIV 16**

**Question No:107** (Marks:1) **Vu-Topper RM**  
The Synchronous counters are also known as Ripple Counters:  
**False ok**

**Question No:108** (Marks:1) **Vu-Topper RM**  
A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is  
**25 mW 235**

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**Question No:109** (Marks:1) **Vu-Topper RM**  
Which of the number is not a representative of hexadecimal system?  
"1001" correct

**Question No:110** (Marks:1) **Vu-Topper RM**  
High level Noise Margins (VNH) of CMOS 5 volt series circuits is \_\_\_\_\_  
0.9 V correct

**Question No:111** (Marks:1) **Vu-Topper RM**  
To get the answer "1" in Boolean addition of three variables, \_\_\_\_\_  
One of the variables must be 1 correct

**Question No:112** (Marks:1) **Vu-Topper RM**  
The 3-variable Karnaugh Map (K-Map) has \_\_\_\_\_ cells for min or max terms  
8 correct

**Question No:113** (Marks:1) **Vu-Topper RM**  
\_\_\_\_\_ is invalid number of cells in a single group formed by the adjacent cells in K-map  
2 correct

**Question No:114** (Marks:1) **Vu-Topper RM**  
Consider  $A=1, B=0, C=1$ . A, B and C represent the input of three bit NAND gate the output of the NAND gate will be \_\_\_\_\_  
Zero

**Question No:115** (Marks:1) **Vu-Topper RM**  
The Binary number 1011.101 has an Integer part represented by \_\_\_\_\_ and a fraction part \_\_\_\_\_ separated by a decimal point.  
1011, 101

**Question No:116** (Marks:1) **Vu-Topper RM**  
 $1011+101 =$  \_\_\_\_\_  
10000

**Question No:117** (Marks:1) **Vu-Topper RM**  
Adding two octal numbers "36" and "71" result in \_\_\_\_\_  
127

**Question No:118** (Marks:1) **Vu-Topper RM**  
The first Least Most digit in decimal number system has  
Has position 0 and weight equal to 1

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- Question No:119** (Marks:1) **Vu-Topper RM**  
Sum term (Max term) is implemented using \_\_\_\_\_ gates  
**OR**
- Question No:120** (Marks:1) **Vu-Topper RM**  
The OR Gate performs a Boolean \_\_\_\_\_ function  
**Add 42**
- Question No:121** (Marks:1) **Vu-Topper RM**  
Adding two octal numbers “36” and “71” result in \_\_\_\_\_  
**127**
- Question No:122** (Marks:1) **Vu-Topper RM**  
NOR Gate can be used to perform the operation of AND, OR and NOT Gate  
**TRUE**
- Question No:123** (Marks:1) **Vu-Topper RM**  
The three fundamental gates are \_\_\_\_\_  
**NOT, OR, AND**
- Question No:124** (Marks:1) **Vu-Topper RM**  
A SOP expression having a domain of 3 variables will have a truth table having \_\_\_\_\_ combinations of inputs and corresponding output values.  
**4 87**
- Question No:125** (Marks:1) **Vu-Topper RM**  
Which of the following is the octal equivalent of 28 decimal number?  
**34**
- Question No:126** (Marks:1) **Vu-Topper RM**  
The maximum decimal number that can be represented using the 64-bit unsigned representation is \_\_\_\_\_.  
 **$(2^{64})-1$**
- Question No:127** (Marks:1) **Vu-Topper RM**  
In a 4-variable K-map, a 2-variable product term is produced by \_\_\_\_\_  
**a 4-cell group of 1s**
- Question No:128** (Marks:1) **Vu-Topper RM**  
For a Standard SOP expression, a \_\_\_\_\_ is placed in the cell corresponding to the product term present in the expression.  
**1**

**Question No:129** (Marks:1) **Vu-Topper RM**  
The \_\_\_\_\_ input select/deselects both the decoders simultaneously.  
**Enable**

**Question No:130** (Marks:1) **Vu-Topper RM**  
NAND and \_\_\_\_\_ gates are known as Universal Gates.  
**NOR**

**Question No:131** (Marks:1) **Vu-Topper RM**  
The declaration section of ABEL generally includes the device declaration,  
\_\_\_\_\_ declarations and set declarations.  
**Pin**

**Question No:132** (Marks:1) **Vu-Topper RM**  
An SOP expression having a domain of 2 variables will have a truth table having  
\_\_\_\_\_ combinations of inputs and corresponding output values.  
**4**

**Question No:133** (Marks:1) **Vu-Topper RM**  
In the 32-bit Single Precision Floating formation, the exponent value  
\_\_\_\_\_ is reserved to represent 0 exponents.  
**0**

**Question No:134** (Marks:1) **Vu-Topper RM**  
CMOS technology is characterized by low power dissipation with \_\_\_\_\_  
switching speeds.  
**Slow**

**Question No:135** (Marks:1) **Vu-Topper RM**  
The complement of a variable is always  
**The inverse of the variable**

**Question No:136** (Marks:1) **Vu-Topper RM**  
 $A(B + C) = A.B + A.C$  is the expression of \_\_\_\_\_.  
**Distributive Law**

**Question No:137** (Marks:1) **Vu-Topper RM**  
If the number 2025 is represented in floating point, then exponent is  
\_\_\_\_\_.  
**3**

**Question No:138** (Marks:1) **Vu-Topper RM**  
Excess-8 code of -6 is \_\_\_\_\_.  
**0010**

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**Question No:139** (Marks:1) **Vu-Topper RM**  
To represent in digital value, the number of digit (0s and 1s) that represents a quantity is \_\_\_\_\_ to the range of values that are to be represented.  
**Proportional**

**Question No:140** (Marks:1) **Vu-Topper RM**  
Suppose we want to transmit the data “10001101” and an “Even-Parity” bit scheme is used to detect errors, the parity bit added to the data will be\_\_\_\_\_  
**Both “0” and “1” can be used**

**Question No:141** (Marks:1) **Vu-Topper RM**  
The carry propagation delay problem in parallel binary adder can be solved by \_\_\_\_\_.  
**Using two full adders**

**Question No:142** (Marks:1) **Vu-Topper RM**  
Two 2-input, 4-bit multiplexers 74X157 can be connected to implement a \_\_\_\_\_ multiplexer.  
**2-input, 8-bit**

**Question No:143** (Marks:1) **Vu-Topper RM**  
The octal equivalent of the following binary number is \_\_\_\_\_  
**117**

**Question No:144** (Marks:1) **Vu-Topper RM**  
A' is written is ABEL as \_\_\_\_\_.  
**!A**

**Question No:145** (Marks:1) **Vu-Topper RM**  
Which of the following is the hexadecimal equivalent of 28?  
**1C**

**Question No:146** (Marks:1) **Vu-Topper RM**  
High Level Noise Margins (VNH) of CMOS 5 volt series circuits is \_\_\_\_\_  
**0.9 V**

**Question No:147** (Marks:1) **Vu-Topper RM**  
Adjacent 1s detector circuit will have active high output for the input.  
**0011 123**

**Question No:148** (Marks:1) **Vu-Topper RM**  
Modern information techniques are relying more on \_\_\_\_\_ transmission.  
**Digital**

**For More Help Vu-Topper RM Contact What's app 03224021365**

**Question No:149** (Marks:1) **Vu-Topper RM**  
The \_\_\_\_\_ select input(s) of the two 4-input multiplexers are common in Dual 4-input multiplexer.  
**Two**

**Question No:150** (Marks:1) **Vu-Topper RM**  
How many data select lines are required for selecting eight inputs?  
**3**

**Question No:151** (Marks:1) **Vu-Topper RM**  
Select the mode of programming in which GAL 16V8 can be programmed.  
**All of the given option**

**Question No:152** (Marks:1) **Vu-Topper RM**  
\_\_\_\_\_ has the fastest switching speed and low power requirement.  
**Advanced low power Schottky**

**Question No:153** (Marks:1) **Vu-Topper RM**  
The PLA can be programmed to give an output of constant \_\_\_\_\_ or \_\_\_\_\_.  
**0.1**

**Question No:154** (Marks:1) **Vu-Topper RM**  
The minimum time for which the input signal has to be maintained at the input of flip-flop is called \_\_\_\_ of the flip-flop.  
**Hold time**

**Question No:155** (Marks:1) **Vu-Topper RM**  
A Divide-by-20 counter can be achieved by using  
**Flip-Flop and DIV 10**

**Question No:156** (Marks:1) **Vu-Topper RM**  
Each stage of Master-slave flip-flop works at \_\_\_\_ of the clock signal.  
**One half**

**Question No:157** (Marks:1) **Vu-Topper RM**  
In Master-Slave flip-flop the clock signal is connected to slave flip-flop using \_\_\_\_  
**NOT**

**Question No:158** (Marks:1) **Vu-Topper RM**  
A 4-bit binary UP/DOWN counter is in the binary state zero. The next state in the DOWN mode is \_\_\_\_  
**1111**

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**Question No:159** (Marks:1) **Vu-Topper RM**  
\_\_\_ is said to occur when multiple internal variables change due to change in one input variable  
**Race condition**

**Question No:160** (Marks:1) **Vu-Topper RM**  
The Synchronous counters are also known as Ripple Counters:  
**False**

**Question No:161** (Marks:1) **Vu-Topper RM**  
The minimum time required for the input logic levels to remain stable before the clock transition occurs is known as the \_\_\_  
**Set-up time**

**Question No:162** (Marks:1) **Vu-Topper RM**  
The n flip-flops store \_\_\_ states.  
 **$2^n$**

**Question No:163** (Marks:1) **Vu-Topper RM**  
When the \_\_\_ Hz sampling interval is selected, the signal at the output of the J-K flip-flop has a time period of \_\_\_  
**1,2**

**Question No:164** (Marks:1) **Vu-Topper RM**  
A positive edge-triggered flip-flop changes its state when \_\_\_  
**Low-to-high transition of clock**

**Question No:165** (Marks:1) **Vu-Topper RM**  
A decade counter is \_\_\_  
**Mod-10 counter**

**Question No:166** (Marks:1) **Vu-Topper RM**  
The look-ahead carry circuits \_\_\_\_\_  
**Reduce propagation delay**

**Question No:167** (Marks:1) **Vu-Topper RM**  
If two numbers in BCD representation generate an invalid BCD number then the binary \_\_\_ is added to the result  
**0110**

**Question No:168** (Marks:1) **Vu-Topper RM**  
Both the multiplexers are selected simultaneously when \_\_\_\_\_ is set to logic \_\_\_\_\_ in 2-inputs, 8-bit Multiplexer.  
**G, Low**

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**Question No:169** (Marks:1) **Vu-Topper RM**  
Function labels required to represent the input/output combinations for each segment in 7-segment display  
7

**Question No:170** (Marks:1) **Vu-Topper RM**  
Multiplexers are also known as \_\_\_\_\_  
Data selectors

**Question No:171** (Marks:1) **Vu-Topper RM**  
The PLA can be programmed to give an output of constant \_\_\_\_\_ or \_\_\_\_\_  
0, 1

**Question No:172** (Marks:1) **Vu-Topper RM**  
Cin is part of \_\_\_\_\_ Adder.  
Full

**Question No:173** (Marks:1) **Vu-Topper RM**  
The look-ahead carry circuits \_\_\_\_\_

**Question No:174** (Marks:1) **Vu-Topper RM**  
Reduce propagation delay

**Question No:175** (Marks:1) **Vu-Topper RM**  
Which of the following gates has the outputs 1 if and only if at least one input is 1?  
OR

**Question No:176** (Marks:1) **Vu-Topper RM**  
A SOP expression can be implemented by one \_\_\_\_\_ combination of gates.  
AND-OR

**Question No:177** (Marks:1) **Vu-Topper RM**  
The carry, instead of rippling through the 4-bits of the individual ALU circuit, has to propagate through \_\_\_\_\_ ALU units in 16-bit ALU.  
Four 150

**Question No:178** (Marks:1) **Vu-Topper RM**  
Digital circuits operate with \_\_\_\_\_ voltage value(s)  
2

**Question No:179** (Marks:1) **Vu-Topper RM**  
The \_\_\_\_\_ is the slowest and consumes more power.  
Standard TTL 61

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**Question No:180** (Marks:1) **Vu-Topper RM**  
The between expression  $X-AB+CD$  represents  
**Two ANDs ORed together**

**Question No:181** (Marks:1) **Vu-Topper RM**  
Which one of the following is NOT a valid rule of Boolean Algebra?  
 **$A=A'$  73**

**Question No:182** (Marks:1) **Vu-Topper RM**  
A 5-Variable Karnaugh map has  
**Thirty two cells**

**Question No:183** (Marks:1) **Vu-Topper RM**  
\_\_\_\_\_ is invalid number of cells in a single group formed by the adjacent cells K-map  
**12**

**Question No:184** (Marks:1) **Vu-Topper RM**  
In 32-bit Single –Precision floating point format representation the range of exponent value is from \_\_\_\_\_ to \_\_\_\_\_  
**+127 to -126**

**Question No:185** (Marks:1) **Vu-Topper RM**  
\_\_\_\_\_ has the fastest switching speed and low power requirements  
**Advanced low power Schottky**

**Question No:186** (Marks:1) **Vu-Topper RM**  
Which of the following is a volatile memory?  
**DRAM**

**Question No:187** (Marks:1) **Vu-Topper RM**  
\_\_\_\_\_ is used when the output is connected back to the input of the PAL or if the output pin is used as an input only.  
**Combinational Input**

**Question No:188** (Marks:1) **Vu-Topper RM**  
The AND Gate performs a logical \_\_\_\_\_ function.  
**multiplication 40**

**Question No:189** (Marks:1) **Vu-Topper RM**  
The Adjacent 1s Detector accepts 4-bit inputs. If \_\_\_\_\_ adjacent 1s are detected in the input, the output is set to high.  
**2 123**

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**Question No:190**

**(Marks:1)**

**Vu-Topper RM**

In 16-input multiplexer, the decoder inputs \_\_\_\_ and \_\_\_\_ enable one out of the four multiplexers.

**C and D 171**

**Question No:191**

**(Marks:1)**

**Vu-Topper RM**

In the keyboard encoder, how many times per second does the ring counter scan the key board?

**650 scans/second**

**Question No:192**

**(Marks:1)**

**Vu-Topper RM**

The FAST Model Page Access allows \_\_\_\_\_ memory read and access times when reading successive data values stored in consecutive locations on the same row.

**Faster**

**Question No:193**

**(Marks:1)**

**Vu-Topper RM**

GAL can be reprogrammed as instead of fuses E2CMOS logic is used which can be programmed to connect a \_\_\_\_\_ with a \_\_\_\_\_.

**row, column**

**Question No:194**

**(Marks:1)**

**Vu-Topper RM**

Which of the following Output Equations determines the output of the State Machine?

**MAX = Q0Q1EN**

**Question No:195**

**(Marks:1)**

**Vu-Topper RM**

The maximum value, represented by a single hexadecimal digit is \_\_\_\_\_.

**"F"**

**Question No:196**

**(Marks:1)**

**Vu-Topper RM**

If the voltage drop across the active load is 0 volts due to absence of current the comparator output is a \_\_\_\_\_.

**1**

**Question No:197**

**(Marks:1)**

**Vu-Topper RM**

The Static Ram (SRAM) is non-volatile and is not a \_\_\_\_\_ density memory as a latch is required to store a single bit of information.

**High**

**Question No:198**

**(Marks:1)**

**Vu-Topper RM**

Demorgan's two theorems prove the equivalency of the NAND and \_\_\_\_\_ gates and the NOR and \_\_\_\_\_ gates respectively.

**Negative-OR, Negative-AND**

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**Question No:199** (Marks:1) **Vu-Topper RM**  
Two signals \_\_\_\_\_ and \_\_\_\_\_ provide the timing inputs to the State Machine.  
**PTIME and QTIME**

**Question No:200** (Marks:1) **Vu-Topper RM**  
The 74HC163 is a 4-bit Synchronous counter, it has \_\_\_\_\_ data output pins.  
**4**

**Question No:201** (Marks:1) **Vu-Topper RM**  
PLDs have In-System Programming (ISP) capability that allows the \_\_\_ to be programmed after they have been installed on a circuit board.  
**PLDs 194**

**Question No:202** (Marks:1) **Vu-Topper RM**  
The CONSTATE.CLK = Clock is used to indicate that the \_\_\_\_\_ state variables change on a clock transition.  
**CONSTATE**

**Question No:203** (Marks:1) **Vu-Topper RM**  
Two types of memories namely the first in-first out (FIFO) memory and last in first out (LIFO) are implemented using \_\_\_\_\_.  
**Shift Registers**

**Question No:204** (Marks:1) **Vu-Topper RM**  
The normal data inputs to a flip-flop (D, S and R, J and K, T) are referred to as \_\_\_\_\_ inputs.  
**Synchronous**

**Question No:205** (Marks:1) **Vu-Topper RM**  
For a down counter that counts from (111 to 000), if current state is "101" the next state will be \_\_\_\_\_.  
**None of the given**

**Question No:206** (Marks:1) **Vu-Topper RM**  
The \_\_\_\_\_ gate and \_\_\_\_\_ gate implementation connected at the B input of the 4-bit Adder is used to allow Complemented or Un-Complemented B input to be connected to the Adder input.  
**XOR, NAND**

**Question No:207** (Marks:1) **Vu-Topper RM**  
The Synchronous SRAM also has a Burst feature which allows the Synchronous SRAM to read or write up to \_\_\_\_\_ location(s) using a single address.  
**Four**

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**Question No:208** (Marks:1) **Vu-Topper RM**  
In NAND based S-R latch, output of each \_\_\_\_\_ gate is connected to the input of the other \_\_\_\_\_ gate.  
**NAND, NAND**

**Question No:209** (Marks:1) **Vu-Topper RM**  
Implementing the Adjacent 1s detector circuit directly from the function table based on the SOP form requires \_\_\_\_\_ gates for the 8 product terms (minterms) with an 8-input OR gate.  
**8 AND**

**Question No:210** (Marks:1) **Vu-Topper RM**  
The \_\_\_\_\_ input overrides the \_\_\_\_\_ input.  
**Asynchronous, synchronous**

**Question No:211** (Marks:1) **Vu-Topper RM**  
A SOP expression can be implemented by an \_\_\_\_\_ combination of gates.  
**AND-OR**

**Question No:212** (Marks:1) **Vu-Topper RM**  
The 64-cell array organized as 8 x 8 cell array is considered  
**as an 8 byte memory**

**Question No:213** (Marks:1) **Vu-Topper RM**  
The terminal count of a 4-bit binary counter in the UP mode is \_\_\_\_\_.  
**1100**

**Question No:214** (Marks:1) **Vu-Topper RM**  
An Asynchronous Down-counter is implemented (Using J-K flip-flop) by connecting \_\_\_\_\_.  
**Q output of all flip-flops to clock input of next flip-flops**

**Question No:215** (Marks:1) **Vu-Topper RM**  
Memory is arranged in \_\_\_\_\_.  
**Two-dimensional manner**

**Question No:216** (Marks:1) **Vu-Topper RM**  
If two numbers in BCD representation generate an invalid BCD number then the binary \_\_\_\_\_ is added to the result.  
**1001**

**Question No:217** (Marks:1) **Vu-Topper RM**  
Subtractors also have output to check if 1 has been \_\_\_\_\_.  
**Primed**

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**Question No:218** (Marks:1) **Vu-Topper RM**

The Test Vector definition defines the test vectors for all the three counter inputs and \_\_\_\_\_ counter output/outputs.

**Three**

**Question No:219** (Marks:1) **Vu-Topper RM**

A multiplexer with a register circuit converts

**Parallel data to serial**

**Question No:220** (Marks:1) **Vu-Topper RM**

A decade counter can be implemented by truncating the counting sequence of a MOD-20 counter.

**True**

**Question No:221** (Marks:1) **Vu-Topper RM**

The n flip-flops store \_\_\_\_\_ states.

**2<sup>n</sup>**

**Question No:222** (Marks:1) **Vu-Topper RM**

The S-R latch has two inputs, therefore \_\_\_\_\_ different combinations of inputs can be applied to control the operation of the S-R latch.

**four**

**Question No:223** (Marks:1) **Vu-Topper RM**

Why demultiplexer is called a data distributor?

**Single input to Single Output**

**Question No:224** (Marks:1) **Vu-Topper RM**

When the transmission line is idle in an asynchronous transmission

**It is set to logic high**

**Question No:225** (Marks:1) **Vu-Topper RM**

UVERPROM is stands for

**Ultra-Violet**

**Question No:226** (Marks:1) **Vu-Topper RM**

In memory write cycle, the time for which the WE signal remains active is known as the \_\_\_\_\_.

**Write pulse width**

**Question No:227** (Marks:1) **Vu-Topper RM**

The outputs of SR latches in elevator state machine are feed back to the \_\_\_\_\_ gate array for connection to the D-flipflops.

**AND**

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**Question No:228** (Marks:1)

**Vu-Topper RM**

PALs tend to execute \_\_\_\_\_ logic.

**SOP**

**Question No:229** (Marks:1)

**Vu-Topper RM**

The ROM used by a computer is relatively \_\_\_\_\_ as it stores few bytes of code used to Boot the Computer system on power up.

**Small**

**Question No:230** (Marks:1)

**Vu-Topper RM**

Which signal must remain valid in memory write cycle after data is applied at the data input lines and must remain valid for a minimum time duration  $t_{WD}$ ?

**WE**

**Question No:231** (Marks:1)

**Vu-Topper RM**

You have to choose suitable option when your timer will reset by considering this given code:

`TRSTATE.CLK = clk;`

`TMRST: = (TRSTATE == NSY2) # (TRSTATE == EWY2);`

**NSY2 or EWY2**

**Question No:232** (Marks:1)

**Vu-Topper RM**

A NOR based S-R latch is implemented using \_\_\_\_\_ gates instead of \_\_\_\_\_ gates.

**NOR, NAND**

**Question No:233** (Marks:1)

**Vu-Topper RM**

Implementation of Latch is required almost \_\_\_\_\_ transistor.

**Six**

**Question No:234** (Marks:1)

**Vu-Topper RM**

In distributed mode, for a 1024 x 1024 DRAM memory and a refresh cycle of 8 msec, each of the 1024 rows has to be refreshed in \_\_\_\_\_ when Distributed refresh is used.

**7.8 microsec**

**Question No:235** (Marks:1)

**Vu-Topper RM**

The NOR logic gate is the same as the operation of the \_\_\_\_\_ gate with an inverter connected to the output.

**NAND**

**Question No:236** (Marks:1)

**Vu-Topper RM**

Select the mode of programming in which GAL16V8 can be programmed:

**All of the given**

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**Question No:237**

**(Marks:1)**

**Vu-Topper RM**

Divide-by-32 counter can be achieved by using  
**Flip-Flop and DIV 32**

**Question No:238**

**(Marks:1)**

**Vu-Topper RM**

The next state table for REQ1, FLOOR1 and OPEN inputs indicates that the \_\_\_\_\_ can be pressed at any time either on the first floor or the second floor in elevator.

**REQ1**

**Question No:239**

**(Marks:1)**

**Vu-Topper RM**

Consider A=1, B=0, C=1. A, B and C represent the input of three bit NAND gate, the output of the NAND gate will be \_\_\_\_\_.

**One**

**Question No:240**

**(Marks:1)**

**Vu-Topper RM**

A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is:

**1111**

**Question No:241**

**(Marks:1)**

**Vu-Topper RM**

Adding two octal numbers "36" and "71" result in \_\_\_\_\_.

**127**

**Question No:242**

**(Marks:1)**

**Vu-Topper RM**

The ABEL Input file can use a \_\_\_\_\_ instead of the equation to specify the Boolean expressions.

**Truth Table**

**Question No:243**

**(Marks:1)**

**Vu-Topper RM**

The domain of the expression  $AB'CD + AB' + C'D + B$  is

**A, B, C and D**

**Question No:244**

**(Marks:1)**

**Vu-Topper RM**

If the number of samples that are collected is reduced by half, the reconstructed signal will be \_\_\_\_\_ from/to the original.

**Different 1**

**Question No:245**

**(Marks:1)**

**Vu-Topper RM**

In DRAM read cycle R /W<sup>-</sup> signal is activated to read data which is made available on the \_\_\_\_\_ data line.

**D(OUT)**

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**Question No:246** (Marks:1) **Vu-Topper RM**  
In case of cascading Integrated Circuit counters, the enable inputs and RCO of the Integrated Circuit counters allow cascading of multiple counters together.  
**True**

**Question No:247** (Marks:1) **Vu-Topper RM**  
Implementation of the FIFO buffer in \_\_\_\_\_ is usually takes the form of a circular buffer.  
**RAM**

**Question No:248** (Marks:1) **Vu-Topper RM**  
As data values are written or read from the RAM Stack Pointer Register increments or decrements its contents always pointing to the stack \_\_\_\_\_.  
**Top**

**Question No:249** (Marks:1) **Vu-Topper RM**  
Which one flip-flop has an invalid output state?  
**SR**

**Question No:250** (Marks:1) **Vu-Topper RM**  
The output of a NAND gate is \_\_\_\_\_ when all the inputs are one.  
**1 47**

**Question No:251** (Marks:1) **Vu-Topper RM**  
The Transition table is very similar to the \_\_\_\_\_ table.  
**State**

**Question No:252** (Marks:1) **Vu-Topper RM**  
Consider the sum of weight method for converting decimal into binary value, \_\_\_\_\_ is the highest weight for 411.  
**256**

**Question No:253** (Marks:1) **Vu-Topper RM**  
Canonical form is a unique way of representing \_\_\_\_\_.  
**SOP 117**

**Question No:254** (Marks:1) **Vu-Topper RM**  
\_\_\_\_\_ Counters as the name indicates are not triggered simultaneously.  
**Synchronous**

**Question No:255** (Marks:1) **Vu-Topper RM**  
Cin is part of \_\_\_\_\_ Adder.  
**Full**

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**Question No:256** (Marks:1) **Vu-Topper RM**  
Flash memories Operation are classified into \_\_\_\_\_ different operation.  
**Two**

**Question No:257** (Marks:1) **Vu-Topper RM**  
A Product term is 0 when \_\_\_\_\_  
**Any one literal is 0**

**Question No:258** (Marks:1) **Vu-Topper RM**  
In 8-input multiplexer, the two outputs are connected through a/an \_\_\_\_\_ gate.  
**OR**

**Question No:259** (Marks:1) **Vu-Topper RM**  
\_\_\_\_\_ Device dissipate varying amount of power depending upon the frequency of operation.  
**CMOS**

**Question No:260** (Marks:1) **Vu-Topper RM**  
Boolean Addition operation is performed by a(an) \_\_\_\_\_ gate.  
**OR**

**Question No:261** (Marks:1) **Vu-Topper RM**  
A SOP expression can be implemented by an \_\_\_\_\_ combination of gates.  
**AND-OR**

**Question No:262** (Marks:1) **Vu-Topper RM**  
The maximum decimal number that can be represented using the 64-bit unsigned representation is \_\_\_\_\_.  
 **$(2^{64})-1$**

**Question No:263** (Marks:1) **Vu-Topper RM**  
In 16-bit ALU, The G output is activated if the 4-bit unit generate a Carry \_\_\_\_ irrespective of Carry \_\_\_\_.  
**Out, In 150**

**Question No:264** (Marks:1) **Vu-Topper RM**  
A standard POS form has \_\_\_\_\_ terms that have all the variables in the domain of the expression.  
**Sum**

**Question No:265** (Marks:1) **Vu-Topper RM**  
In Cascading Priority Encoders, the EO output is connected to the EI input of the encoder which handles \_\_\_\_\_.  
**Lower priority inputs**

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**Question No:266**

**(Marks:1)**

**Vu-Topper RM**

Which of the following is the example of comparater?

**XNOR**

**Question No:267**

**(Marks:1)**

**Vu-Topper RM**

IN CMOS 5 Volt series, Input voltage of Logic high signal (VIH) with a ranges from \_\_\_\_ to \_\_\_\_ volts.

**3,5,5**

**Question No:268**

**(Marks:1)**

**Vu-Topper RM**

The Adjacent 1 S Detector accepts 4-bits input. If \_\_\_\_ adjacent 1S are detected in the input, the output is set to high.

**4**

**Question No:269**

**(Marks:1)**

**Vu-Topper RM**

DE Morgan's two theorems prove the equivalency of the NAND and \_\_\_\_ gates and the NOR and \_\_\_\_ gates respectively.

**Negative-AND, Negative-OR**

**Question No:270**

**(Marks:1)**

**Vu-Topper RM**

Adding two octal numbers "36 and 71" result in \_\_\_\_.

**127**

**Question No:271**

**(Marks:1)**

**Vu-Topper RM**

Any of the \_\_\_\_ forms of the Karnaugh Map can be used to simplify Boolean expressions

**2 89**

**Question No:272**

**(Marks:1)**

**Vu-Topper RM**

Quine-McCluskey and K-Map methods are used for \_\_\_\_ of Boolean expression.

**Simplification 111**

**Question No:273**

**(Marks:1)**

**Vu-Topper RM**

The number "1259" may belong to \_\_\_\_ number system.

**Decimal or Hexadecimal system**

**Question No:274**

**(Marks:1)**

**Vu-Topper RM**

The series of TTL chips are characterized by their \_\_\_\_.

**Switching Speed only 61**

**Question No:275**

**(Marks:1)**

**Vu-Topper RM**

The \_\_\_\_ input selects/deselects both the decoders simultaneously.

**Enable 161**

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**Question No:276** (Marks:1) **Vu-Topper RM**  
All ABEL statements must end with\_\_\_\_.  
**;** **203**

**Question No:277** (Marks:1) **Vu-Topper RM**  
In sequential circuit memory elements are connected with\_\_\_\_.  
**Clock**

**Question No:278** (Marks:1) **Vu-Topper RM**  
In the 32-bit Single Precision Floating Point format, the exponent value\_\_\_\_ is reserved to represent infinity exponents.  
**255**

**Question No:279** (Marks:1) **Vu-Topper RM**  
The limitation in implementation of parallel binary address is known as\_\_\_\_\_  
**Carry input**

**Question No:280** (Marks:1) **Vu-Topper RM**  
The Gray code is different form the unsigned binary code because\_\_\_\_.  
**Successive value of Gray code by only one bit**

**Question No:281** (Marks:1) **Vu-Topper RM**  
Removing the NOT gate at the output of the NOR gate result in an\_\_\_\_\_  
**OR gate** **50**

**Question No:282** (Marks:1) **Vu-Topper RM**  
Portable devices that run on batteries use\_\_\_\_ circuit that have low power dissipation.  
**Integrated**

**Question No:283** (Marks:1) **Vu-Topper RM**  
The domain of the expression  $AB'CD+B$  is  
**B only**

**Question No:284** (Marks:1) **Vu-Topper RM**  
\_\_\_\_\_ is a single input gate  
**OR**

**Question No:285** (Marks:1) **Vu-Topper RM**  
To represent in digital value, the number of digit (0s and 1s) that represent a quantity is \_\_\_\_ to the range of values that are to be represented.  
**Equal**

**Question No:286** (Marks:1) **Vu-Topper RM**  
BCD code of 16 is\_\_\_\_.  
00010001

**Question No:287** (Marks:1) **Vu-Topper RM**  
To determine the seven expressions for each of the seven outputs in 7-segment display, seven\_\_\_\_ variable Karnaugh Maps are used.  
3

**Question No:288** (Marks:1) **Vu-Topper RM**  
In Odd parity generator circuit which gate is used to detect parity errors?  
XOR 132

**Question No:289** (Marks:1) **Vu-Topper RM**  
A 3-variable Karnaugh map has  
Eight cells

**Question No:290** (Marks:1) **Vu-Topper RM**  
The measurable values generally change over a  
Continuous range

**Question No:291** (Marks:1) **Vu-Topper RM**  
\_\_\_\_ uses E2CMOS technology which is Electrically Erasable CMOS instead of Bipolar technology and fusible links.  
GAL

**Question No:292** (Marks:1) **Vu-Topper RM**  
When the number 29 is represent on 7-segment display, which BCD input is represented on LSD display unit?  
1001 172

**Question No:293** (Marks:1) **Vu-Topper RM**  
The expression \_\_\_\_\_ is an example of Commutative Law for Multiplication.  
AB=BA 72

**Question No:294** (Marks:1) **Vu-Topper RM**  
The look-ahead carry circuits\_\_\_\_\_  
Reduce propagation delay

**Question No:295** (Marks:1) **Vu-Topper RM**  
What is the output expression of segment 'b' implementation in BCD to 7-segment decoder?  
B'+C'D'+CD

**For More Help Vu-Topper RM Contact What's app 03224021365**