Virtual University of Pakistan

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CS501 Advance Computer Architecture

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Compiled and Prepared by:
Muhammad Ishfaq (PakPattan)

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Introduction.

Course Content:

Distinction between Computer Architecture, Organization and design, Levels of abstraction in digital design ,Perspectives of different people about computers, General operation of a stored program digital computer, The Fetch – Execute process, Concept of an ISA ,A taxonomy of computers and their instructions, Instruction set features, Addressing Modes, RISC and CISC architectures, Measures of performance, Introduction to the ISA and instruction formats, Coding examples and Hand assembly, Using Behavioral RTL to describe the SRC, Implementing Register Transfers using Digital Logic Circuits, Introduction to the ISA of the FALCON – A,FALCON-E,EAGLE and Modified EAGLE, The Design Process, A Uni-Bus implementation for the SRC, Structural RTL for the SRC instructions, Logic Design for the 1-Bus SRC, The Control Unit, The 2-and 3-Bus Processor Designs. The Machine Reset, Machine Exceptions, Pipelining, Microprogramming, I/O interface design, Programmed I/O Interrupt driven I/O, Direct memory access (DMA),Addition, subtraction, multiplication & division for integer unit, Floating point unit, Memory organization and design, Memory hierarchy, Cache memories, Virtual memory

Course Outline

Course Synopsis

This course will provide the students with an understanding of the various levels of studying computer architecture, with emphasis on instruction set level and register transfer level. This course prepares the students to use basic combinational and sequential building blocks to design larger structures like Arithmetic Logic Units, memory subsystems, I/O subsystems etc.

Learning Outcomes

At the end of the course, you should be able to:

- Understand Instruction Set Architecture design and Central Processing Units of the RISC (Reduced Instruction Set Computers) and the CISC (Complex Instruction Set Computers) type
- Describe the behavior and structure of a computer using RTL (Register transfer language)
- Explain Pipelining and instruction level Parallelism
- Explain the I/O sub systems
- Understand Magnetic disk drives
- Explain the memory module of computer
- Understand Number Systems and Radix Conversion

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FAQ updated version.

Question: what is nested interrupt?

Answer: A system of interrupts that allows an interrupt handler to be interrupted is known as nested interrupts.

Question: What is an interrupt mask?

Answer: A collection of all I/O device interrupt enable bits is known as as a bit vector or Interrupt Mask.

Question: What is memory mapped I/O ?

Answer: In memory mapped I/O a single bus is used for both I/O and memory. Memory mapped I/O is common is common in modern processors. It has two primary motivations: Data transfer to and from the processor is standardized, and the number of connections to the processor chip or board is reduced.

Question: What is Programmed I/O?

Answer: Programmed I/O is used with devices that preform operations that take many instruction execution times and do not deliver or demand quantities of data larger than 1 word in a high-speed burst. Printers would fall into this category.

Question: What is Virtual Memory?

Answer: Virtual memory is a technique of using secondary storage such as disks, to extend the apparent size of physical memory. It permits each process to use the main memory as if it were the only user, and to extend the apparent size of accessible memory beyond its actual physical size.

Question: Difference between Little Endian and Big Endian?

Answer:
Little Endian:
"Little Endian" means that the low-order byte of the number is stored in memory at the lowest address, and the high-order byte at the highest address. (The little end comes first.) For example, a 4 byte LongInt
Byte3 Byte2 Byte1 Byte0will be arranged in memory as follows:
Base Address+0 Byte0
Base Address+1 Byte1
Base Address+2 Byte2
Base Address+3 Byte3
Intel processors (those used in PC's) use "Little Endian" byte order.
Big Endian:
"Big Endian" means that the high-order byte of the number is stored in memory at the lowest address, and the low-order byte at the highest address. (The big end comes first.) Our LongInt, would then be stored as:
Base Address+0 Byte3
Base Address+1 Byte2
Base Address+2 Byte1
Base Address+3 Byte0
Motorola processors (those used in Mac's) use "Big Endian" byte order.

Question: Explain Booth's Algorithm with example.

Answer: Booth's multiplication can be performed using the following method:
Example:
Assume n=7 bits available. Multiply B=22=(0010110)2 by A=34=-(0100010)2 . First represent both operands and their negation in signed 2's complement:
22: 0010110, -22: 1101010
34: 0100010, -34: 1011110
Then carry out the multiplication

The product is given in signed 2's complement and its actual value is negative of the 2's complement:
BxA= -11110100010100 = -00001011101100= -74810

Example: 2 x 6
m=2,p=6;
m = 0010
p = 0000 0110
p
0000 0110 0 no-op
0000 0011 0 >> p
1110 0011 0 p = p - m
1111 0001 1 >> p
1111 0001 1 no-op
1111 1000 1 >> p
0001 1000 1 p = p + m
0000 1100 0 >> p
=12

Example: 2 x -3
m = 0010
p = 0000 1101
1110 1101 0 p = p - m
1111 0110 1 >> p
0001 0110 1 p = p + m
0000 1011 1 >> p
1110 1011 0 p = p - m
1111 0101 1 >>p
1111 0101 1 no-op
1111 1010 1 >>p
=-6

Also note that:

•As the operands are in signed 2's complement form, the arithmetic shift is used for the right shifts above, i.e., the MSB bit (sign bit) is always repeated while all other bits are shifted to the right. This guarantees the proper sign extension for both positive and negative values represented in signed 2's complement.

•When the multiplicand is negative represented by signed 2's complement, it needs to be complemented again for subtraction (when the LSB of multiplier is 1 and the extra bit is 0, i.e., the beginning of a string of 1's).

Question: How we identify the Address Mode of the Instructions ?

Answer: It is extremely easy to identify the addressing mode of the instruction. Just a little concentration is required to understand the concept. I shall use SRC ld (load) instruction to discuss the addressing modes. This instruction is also used in lectures. ld instruction is used to load accumulator (register). Now one can load accumulator

1. by directly moving the data
2. by giving the address of memory location using [] (address operator)
3. by copying the data from some other register
4. by giving the address of memory location. This address will be provided by some other register
5. by using some constant to point the memory address where our desired data is lying
6. by some relative positioning.

On the basis of above given points, addressing modes are obtained.
When directly data is accessed, for example ld 123, then mode is immediate. (According to point 1)

When memory address is given like, ld[123], then mode is direct addressing.
There is also indirect addressing mode, ld[[123]]. Here data in memory at address 123 will be calculated by [123] and the resulting data will be calculated again by [result] to gain the final data to be moved in accumulator. (According to point 2)

When data is moved from some register, ld R2, then it is called register direct. (According to point 3)
When some register contains the address, ld [R2], then mode is register indirect. (According to point 4)

For ld[R1 + 12], the addressing mode is Displacement. (According to point 5)

Instruction jump 4 is example of relative addressing mode. Here directly address is given of memory. Jump 4 will take the control to memory address 4. (According to point 6)

Question: Explain the bench mark programming ?

Answer: Benchmark program is used to measure the performance of hardware or software. Benchmark is termed as a test used to measure hardware or software performance. Benchmarks for hardware use programs that test the capabilities of the equipment, for example, the speed at which a CPU can execute instructions or handle floating-point numbers. Benchmarks for software determine the efficiency, accuracy, or speed of a program in performing a particular task, such as recalculating data in a spreadsheet. The same data is used with each program tested, so the resulting scores can be compared to see which programs perform well and in what areas. The design of fair benchmarks is something of an art, because various combinations of hardware and

software can exhibit widely variable performances under different conditions. Often, after a benchmark has become a standard, developers try to optimize a product to run that benchmark faster than similar products run it in order to enhance sales.

Question: How a debugger disassemble the machine language?

Answer: Debuggers offer more sophisticated functions such as running a program step by step ('single-stepping'), stopping ('breaking') (pausing the program to examine the current state) at some kind of event, and tracking the values of some variables. Debuggers have the ability to modify the state of the program while it is running, rather than merely to observe it.

Question: Why Data Dependence Distance is required for the Branch delays?

Answer: Designing a data forwarding unit requires the study of dependence distances. Without forwarding, the minimum spacing required between two data dependent instructions to avoid hazard is four. The load instruction has a minimum distance of two from all other instructions except branch. Branch delays cannot be removed even with forwarding.

Question: How are shift instructions useful? When do we use them?

Answer: SHIFT instructions move a bit string (or operand treated as a bit string) to the right or left, with excess bits discarded (although one or more bits might be preserved in flags). SHIFT instructions are useful in many ways. e.g., if you multiply two 16 bit numbers the result will be of 32 bit number, so shift is used to adjust the result in the two 16 bit registers. Also, as to multiply or divide by 2, SHIFT Left or SHIFT Right instructions are used.

Question: What is Data bus, Address bus and control bus? How these three are interrelated with MAR and MBR with each other. please explain with diagram ?

Answer: A bus is essentially a shared highway that connects different parts of the system—including the microprocessor, disk-drive controller, memory, and input/output ports; and enables them to transfer information. The bus consists of specialized groups of lines that carry different types of information. One group of lines carries data; another carries memory addresses (locations) where data items are to be found; yet another carries control signals. Buses are characterized by the number of bits they can transfer at a single time, equivalent to the number of wires within the bus.
Address Bus is a hardware path usually consisting of 20 to 64 separate lines used to carry the signals specifying a memory location.
Control Bus is the set of lines (conductors) within a computer that carry control signals between the CPU and other devices. For example, a control bus line is used to indicate whether the CPU is attempting to read from memory or to write to it; another control bus line is used by memory to request an interrupt in case of a memory error.

The CPU can put an address in a special-purpose register known as the memory address register (MAR), and then use a control connection to the main memory. memory-buffer

register (MBR) hold the content of memory operation (load or store). They play a vital role in fetch cycle of a unit. To start off the fetch cycle, the address which is stored in the program counter (PC) is transferred to the memory address register (MAR). The CPU then transfers the instruction located at the address stored in the MAR to the memory buffer register (MBR) via the data lines connecting the CPU to memory. This transfer from memory to CPU is coordinated by the control unit (CU). To finish the cycle, the newly fetched instruction is transferred to the instruction register (IR) and unless told otherwise, the CU increments the PC to point to the next address location in memory.

The illustrated fetch cycle above (Figure 3) can be summarised by the following points:
PC => MAR
MAR => memory => MBR
MBR => IR
PC incremented

After the CPU has finished fetching an instruction, the CU checks the contents of the IR and determines which type of execution is to be carried out next. This process is known as the decoding phase. The instruction is now ready for the execution cycle.

Question: What is the difference between compiler and assembler?

Answer: Compiler is a program that translates another program written in a high-level language into machine language so that it can be executed.
Assembler is a program operating on symbolic input data to produce the equivalent executable machine code.

Question: Sir what are the disadvantages of RICS machine architecture (as there are lot of disadvantages of CISC)?

Answer: There are many advantages of RISC also:
RISC supporters argue that it the way of the future, producing faster and cheaper processors - an Apple Mac G3 offers a significant performance advantage over its Intel equivalent.
Instructions are executed over 4x faster providing a significant performance boost!
However, RISC chips require more lines of code to produce the same results and are increasingly complex. This will increase the size of the application and the amount of overhead required.
RISC developers have also failed to remain in competition with CISC alternatives. The Macintosh market has been damaged by several problems that have affected the availability of 500MHz+ PowerPC chips. In contrast, the PC compatible market has stormed ahead and has broken the 1GHz barrier.
Despite the speed advantages of the RISC processor, it cannot compete with a CISC CPU that boasts twice the number of clock cycles.

Question: Which one is better CISC or RISC?

Answer: RISC is comparatively better than CISC as it has reduced instruction sets. That is why it is used more now a days in computer systems.

Question: What is vex machine?

Answer: The Machine is a dual frequency-tripler circuit that uses crossover distortion. It generates the distortion of the wave in the sloped part of the cycle, instead of the peaks and valleys.

Question: Tell me about Behavioral RTL ? What are its functions ?

Answer: Register Transfer Level (RTL) is by far the most commonly used style of VHDL (Very High Speed Integrated Circuit Hardware Description Language) description. At this level, systems are described in terms of combinational and sequential functions at the behavioral level. The functions are often described using individual processes and interconnected using signals to form a dataflow. Typical functions included in an RTL description are Registers, Counters and State Machines along with combinational functions such as Multiplexers, Arithmetic Units and Decoders. The RTL style may include some structural information via the dataflow. However, the individual functional blocks are invariably described using behavioral constructs rather than instantiated gates and flip-flops. Many designs are made up from registers interspersed with combinational functions and together these form the data path. Transfers between registers and operations carried out by combinational functions are controlled by the controller or control path which is usually a behavioral description of a Finite State Machine.
The RTL level of description is possibly the most useful of all the alternative levels and is particularly relevant to those people involved with producing real hardware using VHDL, ie. users of logic synthesis, since this level is the accepted style for designs which are intended for synthesis. The majority of VHDL users are targeting synthesis tools and therefore it is probably true to say that the majority of VHDL descriptions are written in the RTL style.

Question: How can we utilize the functional parallelism ?

Answer: This kind of parallelism is based on different functional blocks in your application. The idea is simple: The application is split into separate processing units, that communicate with a fixed number other units in such a way that the output of one part serves as the input of another part. Thus we can visualize such a system as a set of nodes that are connected by pipes in which data only flow in one direction.
A good example is a compiler. Such a compiler may consist of a scanner, a parser and a code-generator. The output of the scanner is the input of the parser. The output of the parser is the input of the code-generator. And the output of the codegenerator is written to the disk.

Question: I want to know about PVM (PARALLEL VIRTUAL MACHINE) and MPI (MESSAGES PASSING INTER FACE).

Answer: PVM (Parallel Virtual Machine) is a software package that permits a heterogeneous collection of Unix and/or Windows computers hooked together by a network to be used as a single large parallel computer. Thus large computational problems can be solved more cost effectively by using the aggregate power and memory of

many computers. PVM enables users to exploit their existing computer hardware to solve much larger problems at minimal additional cost. Hundreds of sites around the world are using PVM to solve important scientific, industrial, and medical problems in addition to PVM's use as an educational tool to teach parallel programming. With tens of thousands of users, PVM has become the de facto standard for distributed computing world-wide.

MPI-Message passing is a programming paradigm used widely on parallel computers, especially Scalable Parallel Computers (SPCs) with distributed memory, and on Networks of Workstations (NOWs). The MPI standard defines the user interface and functionality for a wide range of message-passing capabilities. The major goal of MPI, as with most standards, is a degree of portability across different machines. Another type of compatibility offered by MPI is the ability to run transparently on heterogeneous systems, that is, collections of processors with distinct architectures. Another type of compatibility offered by MPI is the ability to run transparently on heterogeneous systems, that is, collections of processors with distinct architectures. It is possible for an MPI implementation to span such a heterogeneous collection, yet provide a virtual computing model that hides many architectural differences. One example is that MPI guarantees that the underlying transmission of messages is reliable. The user need not check if a message is received correctly.

Question: What is Process - Level **Concurrent Execution ?**

Answer: Modern operating systems allow several processes to execute concurrently. It is not difficult to imagine several independent processes each being concurrently executed statement-by-statement on a different machine.

On a single processor, the OS, to create the illusion of concurrency, switches a single processor among several processes, allowing it to run one for only a few thousandths of a second before moving on to another. When viewed by a human, these processes appear to run concurrently.

Thus in the example, the execution of the three processes is interleaved. As a result, the output on the screen is a mixture of `As' and `Bs'.

Question: What is difference between hardware debugger & software debugger?

Answer: Hardware Debugger is a graphical tool for detection, diagnostics and testing of custom hardware, designed to meet the needs of the hardware developer by enabling quick and easy testing of hardware without writing any code.
Hardware Debugger runs under Linux, Solaris, Windows 98, Me, NT, 2000 and Windows CE.

Software Debugger is a program designed to aid in debugging another program by allowing the programmer to step through the program, examine data, and monitor conditions such as the values of variables.

Question: What is difference between concurrent and sequential statements?

Answer: Concurrent is the characteristic of a computer operation in which two or more processes (programs) have access to the microprocessor's time and are therefore carried out nearly simultaneously. Because a microprocessor can work with much smaller units of time than people can perceive, concurrent processes appear to be occurring simultaneously but in reality are not.

Sequestial statements are formed or characterized by a sequence, as of units.

Question: What is FALCON-A ?

Answer: FALCON-A is an acronym for First Architecture for Learning Computer Organization and Networks (version A). The term Organization is intended to include Architecture and Design in this acronym.

Question: What is CPU register and processor register?

Answer: CPU registers are memory slots on the actual processor, storing data there gets rid of the overhead of retrieving the data from normal memory. This memory is quite small compared to normal memory though so only a few variables can be stored there. There is no such term as processor register. All registers are the part of processor.

Question: Explain the bench-mark programming ?

Answer: Benchmark programming is used to measure the performance of hardware or software. Its is a test program used to measure hardware or software performance. Benchmarks for hardware use programs that test the capabilities of the equipment; for example, the speed at which a CPU can execute instructions or handle floating point numbers. Benchmarks for software determine the efficiency, accuracy, or speed of a program in performing a particular task, such as recalculating data in a spreadsheet. The same data is used with each program tested, so the resulting scores can be compared to see which programs perform well and in what areas.

Question: Define MIPS computer?

Answer: MIPS is an acronym for millions of instructions per second. A common measure of processor speed. It is an old measure of a computer's speed and power, MIPS measures roughly the number of machine instructions that a computer can execute in one second. However, different instructions require more or less time than others, and there is no standard method for measuring MIPS. In addition, MIPS refers only to the CPU speed, whereas real applications are generally limited by other factors, such as I/O speed.

Question: What difference between the logical address and effective address ?

Answer: Logical address is a virtual address which is a memory location accessed by an application program in a system with virtual memory such that intervening hardware

and/or software maps the virtual address to real (physical) memory. During the course of execution of an application, the same virtual address may be mapped to many different physical addresses as data and programs are paged out and paged in to other locations. Effective address is the operand or the destination address

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Question: What is the meaning of ISA ?

Answer: This set of instructions or operations and the resources together form the instruction set architecture (ISA). It is the ISA, which serves as an interface between the program and the functional units of a computer, i.e., through which, the computer's resources, are accessed and controlled.

Question: What are the "Emulators " and what are the function of emulators . Is it hardware tool?

Answer: Emulators are designed to make one type of computer or component act as if it were another. By means of an emulator, a computer can run software written for another machine. In a network, microcomputers might emulate mainframes or terminals so that two machines can communicate. It can be a hardware or software.

Question: Why CISC processors are faster in execution as compared to RISC?

Answer: RISC architecture optimizes each of these instructions so that it can be carried out very rapidly, usually within a single clock cycle.

CISC architecture can be very powerful, allowing for complicated and flexible ways of calculating such elements as memory addresses. All this complexity, however, usually requires many clock cycles to execute each instruction.

So, RISC architecture is faster in execution.

Question: Sir, please tell me that what is the SRC NOTATION?

Answer: SRC Notation can be written as:
• R[3] means contents of register 3 (R for register)
• M[8] means contents of memory location 8 (M for memory)
• A memory word at address 8 is defined as the 32 bits at address 8,9,10 and 11 in the memory. This is shown in the figure.
• A special notation for 32-bit memory words is

M[8]<31…0>:=M[8]ãM[9]ãM[10]ãM[11]

ã is used for concatenation.

Question: Sir what is an ISA ? What is ISA design and development ?

Answer: ISA is an acronym for Industry Standard Architecture. A bus design specification that allows components to be added as cards plugged into standard expansion slots in IBM Personal Computers and compatibles. Originally introduced in the IBM PC/XT with an 8-bit data path, ISA was expanded in 1984, when IBM introduced the PC/AT, to permit a 16-bit data path. A 16-bit ISA slot actually consists of two separate 8-bit slots mounted end-to-end so that a single 16-bit card plugs into both slots. An 8-bit expansion card can be inserted and used in a 16-bit slot (it occupies only one of the two slots), but a 16-bit expansion card cannot be used in an 8-bit slot.

ISA design is composed of Data types/sizes, instruction types, memory address modes, control flow instructions, instructions encoding etc .

Question: RISC and CISC architectures? what is the difference between these two?

Answer: RISC is an acronym for reduced instruction set computers. A microprocessor design that focuses on rapid and efficient processing of a relatively small set of simple instructions that comprises most of the instructions a computer decodes and executes. RISC architecture optimizes each of these instructions so that it can be carried out very rapidly, usually within a single clock cycle. RISC chips thus execute simple instructions more quickly than general-purpose CISC (complex instruction set computers) microprocessors, which are designed to handle a much wider array of instructions. They are, however, slower than CISC chips at executing complex instructions, which must be broken down into many machine instructions that RISC microprocessors can perform. CISC is an acronym for complex instruction set computers. The implementation of complex instructions in a microprocessor design so that they can be invoked at the assembly language level. The instructions can be very powerful, allowing for complicated and flexible ways of calculating such elements as memory addresses. All this complexity, however, usually requires many clock cycles to execute each instruction.

Question: What is Parallel Architecture and what is relation between Language & Parallel Architecture?

Answer: The architecture of a computer system that can carry out several computational operations simultaneously. Parallel architectures have evolved from special-purpose machines to commodity servers.
Parallel Architecture can be hardware of software based, therefore, software based parallel architecture are related to language based.

Question: Tell me about Parallel Processing & ILP Processing? Tell me also about the difference between these two?

Answer: Parallel Processing is a method of processing that can run only on a type of computer containing two or more processors running simultaneously. Parallel processing differs from multiprocessing in the way a task is distributed over the available processors. In multiprocessing, a process might be divided up into sequential blocks, with one processor managing access to a database, another analyzing the data, and a third handling graphical output to the screen. Programmers working with systems that perform parallel processing must find ways to divide a task so that it is more or less evenly distributed among the processors available.

Instruction Level Parallel Processing utilizes the parallel execution of the lowest level computer operations; adds, multiplies, loads, and so on, to increase performance transparently.

ILP overlap individual machine operations (add, mul, load…) so that they execute in parallel, transparent to the user , speeds up execution.
Parallel Processing is having separate processors getting separate chunks of the program (processors programmed to do so) , non-transparent to the user, speed up and quality up.

Question: What are Basic ILP Classes ?

Answer: Instruction level parallelism is obtained primarily in two ways in uniprocessors: through pipelining and through keeping multiple functional units busy executing multiple instructions at the same time. When a pipeline is extended in length beyond the normal five or six stages (e.g., I-Fetch, Decode/Dispatch, Execute, D-fetch, Writeback), then it may be called Superpipelined. If a processor executes more than one instruction at a time, it may be called Superscalar. These two techniques can be combined into a Super-Super architecture.

Question: I want to know about RAW , WAR & WAW Dependencies.

Answer: RAW (read after write) is an issue for pipelined processors.
B tries to read a register before A has written it and gets the old value. This is common, and forwarding helps to solve it.

WAW (write after write)
B tries to write an operand before A has written it.

After instruction B has executed, the value of the register should be B's result, but A's result is stored instead.

WAW (write after write)
B tries to write an operand before A has written it.

After instruction B has executed, the value of the register should be B's result, but A's result is stored instead.
This can only happen with pipelines that write values in more than one stage.

Question: What is branching in advance architecture?

Answer: A sequence of program instructions to which the normal sequence of instructions give up control, depending on the value of certain variables. The instructions executed as the result of such a passing of control.

Question: What is data Parallelism?

Answer: Data parallelism involves performing a similar computation on many data objects simultaneously. This kind of parallelism is based on the need to process a lot of data in the same way. Well known examples are found in the area of image processing (raytracing, frame analysis), the queens problem discussed in a later chapter, database transaction systems etc. The common principle is that one program code treats different kinds of data on several independently processing nodes. The corresponding 'farm' software architecture usually consists of one 'master' process, distributing the data and several 'worker' processes that do the work.

Question: What are super scaler processors?

Answer: The name means these processors are scalar processors that are capable of executing more than one instruction in each cycle. The keys to superscalar execution are an instruction fetching unit that can fetch more than one instruction at a time from cache; instruction decoding logic that can decide when instructions are independent and thus executed simultaneously; and sufficient execution units to be able to process several instructions at one time. Note that the execution units may be pipelined, e.g. they may be floating point adders or multipliers, in which case the cycle time for each stage matches the cycle times on the fetching and decoding logic. In many systems the high level architecture is unchanged from earlier scalar designs. The superscalar designs use instruction level parallelism for improved implementation of these architectures.

Question: Tell me something about the Processing of Control Transfer Instructions .

Answer: In the binary file, there may be gaps in between the instructions due to the alignment constraints. Control of the program execution never reaches to such gaps. The flow of a program is affected by the control transfer instructions. We have divided the control transfer instructions under six categories, namely unconditional and conditional jump instructions, unconditional and conditional call (to a procedure) instructions and lastly unconditional and conditional return (from a procedure) instructions. The process of disassembly takes care of such instructions. An occurance of an instruction of such type is used to identify the address ranges that contains the code. Otherwise, disassembled instructions sequence might be completely wrong. Therefore, we need the information about all such instructions.

Instructions under each category can be found by a simple method. The method is based on the assumption that instructions are described in a hierarchical manner in the processor specification. If a complete instruction specification tree is made, then instruction of a category can be marked under a subtree i.e. an instruction is put under a particular category if the root node of the corresponding subtree is traversed during flattening of the instruction. If a processor specification is not written in this manner, then a little effort is needed to modify it.

Question: Tell me something about Pipelined Processors and its Types .

Answer: Pipelined Processors are consisting of the method of processing on a computer that allows fast parallel processing of data. This is accomplished by overlapping operations using a pipe(A portion of memory that can be used by one process to pass information along to another. Essentially, a pipe works like its namesake: It connects two processes so that the output of one can be used as the input to the other), or a portion of memory that passes information from one process to another.

Question: What is meant by Pipelining & Repilication ?

Answer: Pipelining is a method of fetching and decoding instructions (preprocessing) in which, at any given time, several program instructions are in various stages of being fetched or decoded. Ideally, pipelining speeds execution time by ensuring that the microprocessor does not have to wait for instructions; when it completes execution of one instruction the next is ready and waiting. In parallel processing, a method in which instructions are passed from one processing unit to another, as on an assembly line, and each unit is specialized for performing a particular type of operation.

Replication means to copy. In a distributed database management system, the process of copying the database (or parts of it) to the other parts of the network. Replication allows distributed database systems to remain synchronized.

Question: Tell me about VILW Architecture in detail.

Answer: Very-Long Instruction Word (VLIW) architectures are a suitable alternative for exploiting instruction-level parallelism (ILP) in programs, that is, for executing more than one basic (primitive) instruction at a time. These processors contain multiple functional units, fetch from the instruction cache a Very-Long Instruction Word containing several primitive instructions, and dispatch the entire VLIW for parallel execution. These capabilities are exploited by compilers which generate code that has grouped together independent primitive instructions executable in parallel. The processors have relatively simple control logic because they do not perform any dynamic scheduling nor reordering of operations (as is the case in most contemporary superscalar processors).
VLIW has been described as a natural successor to RISC, because it moves complexity from the hardware to the compiler, allowing simpler, faster processors.
The objective of VLIW is to eliminate the complicated instruction scheduling and parallel dispatch that occurs in most modern microprocessors. In theory, a VLIW processor should be faster and less expensive than a comparable RISC chip.
The instruction set for a VLIW architecture tends to consist of simple instructions (RISC-like). The compiler must assemble many primitive operations into a single "instruction word" such that the multiple functional units are kept busy, which requires enough instruction-level parallelism (ILP) in a code sequence to fill the available operation slots. Such parallelism is uncovered by the compiler through scheduling code speculatively across basic blocks, performing software pipelining, reducing the number of operations executed, among others.

VLIW has been perceived as suffering from important limitations, such as the need for a powerful compiler, increased code size arising from aggresive scheduling policies, larger memory bandwidth and register-file bandwidth, limitations due to the lock-step

operation, binary compatibility across implementations with varying number of functional units and latencies. In recent years, there has been significant progress regarding these issues, due to general advances in semiconductor technology as well as to VLIW-specific activities. For example, our tree-based VLIW architecture provides binary compatibility for VLIW implementations of varying width, and our VLIW compiler contains state-of-the-art parallelizing/optimizing algorithms.
Question: How a debugger disassemble the machine language? What is mean by functional unit ?What is source and destination operand?
Answer: Debuggers offer more sophisticated functions such as running a program step by step ('single-stepping'), stopping ('breaking') (pausing the program to examine the current state) at some kind of event, and tracking the values of some variables. Debuggers have the ability to modify the state of the program while it is running, rather than merely to observe it.

Functional Unit is an entity of hardware, software, or both, capable of accomplishing a specified purpose. It is a subsystem of the central processing unit of a computer. For example, arithmetic and logic unit, memory address register, barrel shifter, register file.

Source operand is an argument of an operator or of a machine language instruction which is used in the instruction operation.
In destination operand, the result is stored or where the resulting is pointing.

Question: What are FLYNN's Classification and Proposed Classification?

Answer: Flynn uses the stream concept for describing a machine's structure. A stream simply means a sequence of items (data or instructions). Four main types of machine organizations can be found:
SISD (Singe-Instruction stream, Singe-Data stream)
SISD corresponds to the traditional mono-processor (von Neumann computer). A single data stream is being processed by one instruction stream.
SIMD (Singe-Instruction stream, Multiple-Data streams)
In this organization, multiple processing units of the same type process on multiple-data streams . This group is dedicated to array processing machines. Sometimes, vector processors can also be seen as a part of this group.
MISD (Multiple-Instruction streams, Singe-Data stream)
In case of MISD computers, multiple processing units operate on one single-data stream. In practice, this kind of organization has never been used.
MIMD (Multiple-Instruction streams, Multiple-Data streams)
This last machine type builds the group for the traditional multi-processors. Several processing units operate on multiple-data streams.

There is no such specific parallel classification named as proposed classification. More likely, it is termed as the most recommended classification used for parallel architectures. The explicit architectures, for example, SIMD and MIMD are proposed as in reconfigurable architecture as they are prototyped more easily and ahead of their time.

Question: What is Binary Semaphore and the Queue Semaphore?

Answer: Binary Semaphore uses a boolean value as in case of flags. The value of the semaphore is tested, and if it is true, sets it to false, and if false, waits. In Queue Semaphore, the value of the semaphore is set in queue to be processed. A semaphore indicates to other potential users that a file or other resource is in use and prevents access by more than one user.

Question: When CPU encounter an opcode of the instruction from the system memory, in what register does it hold that opcode?

Answer: When there are no queue of instructions , then it will not be stored in the memory , rather it will directly be processed. Otherwise , instruction register IR , is used to hold the current instruction.

Question: What is diffrence between encoding and decoding?

Answer: Encoding:
In programming, to put something into code, which frequently involves changing the form, for example, changing a decimal number to binary-coded form.In Computer Science, to convert (a character, routine, or program) into machine language.

Decoding:
To convert from code into plain text.

Question: Differentiate between CPU register and Cache Memory.

Answer: CPU registers are memory slots on the actual processor, storing data there gets rid of the overhead of retrieving the data from normal memory. This memory is quite small compared to normal memory though so only a few variables can be stored there.

Cache Memory is a special memory subsystem in which frequently-used data values are duplicated for quick access. A memory cache stores the contents of frequently-accessed RAM locations and the addresses where these data items are stored. When the processor references an address in memory, the cache checks to see whether it holds that address. If it does hold the address, the data is returned to the processor; if it does not, a regular memory access occurs. A cache is useful when RAM accesses are slow compared with the microprocessor speed, because cache memory is always faster than main RAM memory. In Computer Science, a fast storage buffer in the central processing unit of a computer. In this sense, also called cache memory.

Question: How the processor knows that it has executed the instruction,who generate the control signal for that. What is exectiopn?

Answer: Instruction Pointer contains the address of the next instruction to be executed and once the instruction is executed, the next address is shifted in IP, processor has no part in it.

Exception:

In programming, a problem or change in conditions that causes the microprocessor to stop what it is doing and handle the situation in a separate routine. An exception is similar to an interrupt; both refer the microprocessor to a separate set of instructions.

Question: What are Dependencies Between the Instructions of a Program?

Answer: Several important aspects of software systems can be expressed as dependencies between their components. A special class of dependencies concentrates on the program text and captures the technical structure and behavior of the target system. The central characteristic making such program dependencies valuable in software engineering environments is that they can be automatically extracted from the program by applying well-known methods of programming language implementation. Dependencies between the instructions is caused as some instructions may not occur before some specific instruction.

Glossary (Updated Version)

Activation record :

Values of the parameters, local variables and return address of a procedure call

---

Address:

A number that identifies a memory location

---

address bus :

The set of electrical pathways for address signals

---

assembler :

A program that translates an assembly language program into machine language. bus

---

bus :

A set of wires or connections connecting the CPU, memory, and I/O ports
Clock cycle : Fundamental time unit of a computer. Every operation executed by the computer takes at least one and possibly multiple cycles. Typically, the clock cycle is now in the order of one to a few nanoseconds.

Clock frequency :

Reciproke of the clock cycle:

the number of cycles per second expressed in Hertz (Hz). Typical clock frequencies nowadays are 400 MHz--1 GHz.

Clock period :

The time interval between two clock pulses

---

clock rate :

The number of clock pulses per second, measured in megahertz (MHz)

---

control bus :

The set of electrical paths for control signals

Control processor :

The processor in a processor array machine that issues the instructions to be executed by all the processors in the processor array. Alternatively, the control processor may perform tasks in which the processors in the array are not involved, e.g., I/O operations or serial operations.

---

data bus :

The set of electrical paths for data signals

---

handshaking :

A protocol for devices to communicate with each other

I/O devices :

Devices that handle input and output data of the computer; typical I/O devices are display monitor, disk drive and printer

---

I/O ports :

Circuits that function as transfer points between the CPU and I/O devices
instruction pointer, IP : A CPU register that contains the address of the next instruction

---

instruction set :

The instructions the CPU is capable of performing

---

mask :

A bit pattern used in logical operations to clear, set or test specific bits in an operand

---

multiprocessing :

A mode of operation in which two or more connected and roughly equal processing units each carry out one or more processes (programs or sets of instructions) in tandem. In multiprocessing, each processing unit works on a different set of instructions or on different parts of the same process.

---

multitasking :

The ability of a computer to execute several programs at the same time
object file : The machine language file created by the assembler from the source program file

---

opcode :

Numeric or symbolic code denoting the type of operation for an instruction

---

operand :

The data specified in an instruction

---

parallel processing :

A method of processing that can run only on a type of computer containing two or more processors running simultaneously. Parallel processing differs from multiprocessing in the way a task is distributed over the available processors. In multiprocessing, a process might be divided up into sequential blocks, with one processor managing access to a database, another analyzing the data, and a third handling graphical output to the screen. Programmers working with systems that perform parallel processing must find ways to divide a task so that it is more or less evenly distributed among the processors available.

Pipelining:

In parallel processing, a method in which instructions are passed from one processing unit to another, as on an assembly line, and each unit is specialized for performing a particular type of operation.

RISC :

Reduced Instruction Set Computer. A CPU with its instruction set that is simpler in comparison with the earlier Complex Instruction Set Computers (CISCs) The instruction set was reduced to simple instructions that ideally should execute in one cycle.

Shared Memory :

Memory configuration of a computer in which all processors have direct access to all the memory in the system. Because of technological limitations on shared bandwidth generally not more than about 16 processors share a common memory.

---

simulator :

One that simulates, especially an apparatus that generates test conditions

---

source operand :

Second operand in an instruction usually not changed by the instruction

---

VLIW :

Very Large Instruction Word processing. The use of large instruction words to keep many functional units busy in parallel. The scheduling of instructions is done statically by the compiler and, as such, requires high quality code generation by that compiler

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Fall 2011 Latest Papers (Current)
Papers Number 01

Mid-Term Past Papers (Updated Version)

Short Question (Set-1)

Question No: 17 (M a r k s: 2)

Write the following statement of an Arithmetic Instruction using RTL.
If op-code is 0, the instruction is 'add'. The values in register rb and rc are added and the result is stored in register ra.

Answer:

(op<4..0>=0):R[ra] ← R[rb]+R[rc]

Question No: 18 (M a r k s: 2)

Given below are the various fields of an SRC instruction register.

a) operation code field : **op<4..0>**
b) target register field : **ra<4..0>**
c) operand, address index, or branch target register : **rb<4..0>**
d) second operand, conditional test, or shift count register: **rc<4..0>**

Rewrite these various fields of an SRC instruction, using the **RTL.**

Answer:

op<4..0>:=IR<31..27>
ra<4..0>:= IR<26..22>
rb<4..0>:= IR<21..17>
rc<4..0>:= IR<16..12>

Question No: 19 (M a r k s: 2)

How can you define microprogram ?

Answer:

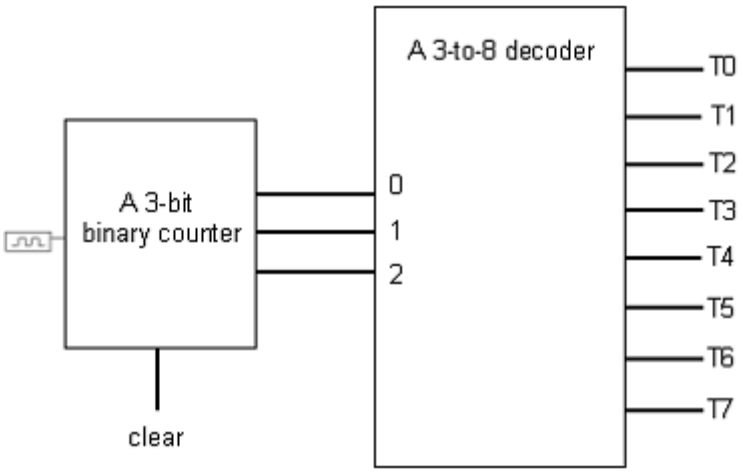
A collection of microinstructions is called a microprogram. These microprograms generate the sequence of necessary control signals required to process an instruction. These microprograms are stored in a memory called the control store.

Question No: 20 (M a r k s: 3)

What is the role of timing step generator in a processor?

Answer:

To ensure the correct and controlled execution of instructions in a program, and all the related operations, a timing device is required. This is to ensure that the operations of essentially different instructions do not mix up in time. There exists a 'timing step generator' that provides mutually exclusive and sequential timing intervals. This is analogous to the clock cycles in the actual processor. A possible implementation of the timing step generator is shown in the figure. Each mutually exclusive step is carried out in one timing interval. The timing intervals can be named T0, T1…T7. The given figure is helpful in understanding the 'mutual exclusiveness in time' of these timing intervals.



Question No: 21 (M a r k s: 3)

What is the utility of reset operation and when it is required?

Answer:

The reset operation

Reset operation is required to change the processor's state to a known, defined value. The two essential features of a reset instruction are clearing the control step counter and reloading the PC to a predefined value. The control step counter is set to zero so that operation is restarted from the instruction fetch phase of the next instruction. The PC is reloaded with a predefined value usually to execute a specific recovery or initializing program.

In most implementations the reset instruction also clears the interrupt enable flags so as to disable interrupts during the initialization operation. If a condition code register is present, the reset instruction usually clears it, so as to clear any effects of previously executed instructions. The external flags and processor state registers are usually cleared too.

Question No: 22 (M a r k s: 5)

Write the Structural RTL description for un-conditional jump instruction for uni-bus data path implementation.

jump [ra+c2]

Answer:

step	RTL
T0-T2	Instruction fetch
T3	(ra=0):A←PC, (ra≠0):A←R[ra]
T4	C←A+c2(sign extend)
T5	PC←C

Question No: 23 (M a r k s: 5)

What function is performed by the reset operation of a processor? What are the two types of reset operations?

Answer:
Reset operation is required to change the processor's state to a known, defined value. The two essential features of a reset instruction are clearing the control step counter and reloading the PC to a predefined value.

Hard Reset

The SRC performs a hard reset upon receiving a start (Strt) signal. This initializes the PC and the general registers.

Soft Reset

The SRC performs a soft reset upon receiving a reset (rst) signal. The soft reset results in initialization of PC only.

==========>

Short Question (Set-2)

Question No: 17 (Marks: 2)

Write the following statement of an Arithmetic Instruction using RTL.
If op-code is 0, the instruction is 'add'. The values in register rb and rc are added and the result is stored in register rc .

Answer:
(op<4..0>=0):R[ra] ← R[rb]+R[rc]

Write short answers to the following questions:
[3 x 5]

a. What is the advantage of a linker in the development of assembly language programs?

Solution:-
The linker:
When developing large programs, different people working at the same time can develop separate modules of functionality. These modules can then be 'linked' to form a single module that can be loaded and executed. The modularity of programs, that the linking step in assembly language makes possible, provides the same convenience as it does in higher-level languages; namely abstraction and separation of concerns. Once the functionality of a module has been verified for correctness, it can be re-used in any number of other modules. The programmer can focus on other parts of the program. This is the so-called "modular" approach, or the "top-down" approach.

b. Define term "Single stepping".

Solution:-
Single stepping:
Single stepping and breakpoints that allow the examination of the status of the program and registers at desired points during execution.

c. Define term "Type checking".

Solution:-
Type Checking:-

High-level languages provide various primitive data types, such as integer, Boolean and a string, that a programmer can use. Type checking provides for the verification of proper usage of these data types. It allows the compiler to determine memory requirements for variables and helping in the detection of bad programming practices.
On the other hand, there is generally no provision for type checking at the machine level, and hence, no provision for type checking in assembly language. The machine only sees strings of bits. Instructions interpret the strings as a type, and it is usually limited to signed or unsigned integers and floating point numbers. A given 32-bit word might be an instruction, an integer, a floating-point number, or 4 ASCII characters. It is the task of the compiler writer to determine how high-level language data types will be implemented using the data types available at the machine level, and how type checking will be implemented.

d. Define term "Instruction set".

Solution:-
Instruction Set
A collection of all possible machine language commands that a computer can understand and execute is called its instruction set. Every processor has its own unique instruction set. Therefore, programs written for one processor will generally not run on another processor. This is quite unlike programs written in higher-level languages, which may be portable. Assembly/machine languages are generally unique to the processors on which they are run, because of the differences in computer architecture.
Three ways to list instructions in an instruction set of a computer:
• by function categories
• by an alphabetic ordering of mnemonics
• by an ascending order of op-codes

e. Why computer logic design is different from classical logic design?

Solution:-
Classical logic design versus computer logic design:
The traditional sequential circuit design techniques for a finite state machine are not very practical when it comes to the design of a computer, in spite of the fact that a computer is a finite state machine. The reason is that employing these techniques ismuch too complex as the computer can assume hundreds of states.

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Short Question (Set-3)

In this section we have listed the instructions that are common to the Instruction Set Architectures of all the processors under our study.
• Arithmetic Instructions add, addi & sub.
• Logic Instructions and, andi, or, ori, not.
• Shift Instructions. Right shift, left shift & arithmetic right shift.
• Data movement Instructions. Load and store instructions.
• Control Instructions Conditional and unconditional branches, nop & reset.

Q : DEFINE HARD RESET AND SOFT RESET OPERATIONS IN SRC.

Answer:

Hard Reset

The SRC should perform a hard reset upon receiving a start (Strt) signal. This initializes the PC and the general registers.

Soft Reset

The SRC should perform a soft reset upon receiving a reset (rst) signal. The soft reset results in initialization of PC only.

Q : Write two pipelining problem and define them briefly.

Answer:

Certain complications may arise from pipelining a processor. They are explained below:

Data dependence

This refers to the situation when an instruction in one stage of the pipeline uses the results of an instruction in the previous stage.

Data forwarding

When using data forwarding, special hardware is added to the processor, which allows the results of a particular pipeline stage to be transferred directly to another stage in the pipeline where they are required. Data may be forwarded directly from the execute stage of one instruction to the decode stage of the next instruction. Considering the above example, S1 will be in the execute stage when S2 will be decoded. Using a comparator we can determine that the destination operand of S1 and source operand of S2 are the same. So, the result of S1 may be directly forwarded to the decode stage.

Branch delay

Branches can cause problems for pipelined processors. It is difficult to predict whether a branch will be taken or not before the branch condition is tested. Hence if we treat a branch instruction like any normal instruction, the instructions following the branch will be loaded in the stages following the stage which carries the branch instruction. If the branch is taken, then those instructions would need to be removed from the pipeline and their effects if any, will have to be undone. An alternate method is to introduce stalls, or nop instructions, after the branch instruction.

Load delay

Another problem surfaces when a value is loaded into a register and then immediately used in the next operation.

Q : What information is provided by the addressing modes of some processors?

Answer:

Addressing modes are the different ways in which the CPU generates the address of operands. In other words, they provide access paths to memory locations and CPU registers.

Q : Eleborate Pre-Fetching Concept?

Answer:

Pre-fetching and speculative execution techniques are used with a pipelined architecture.

Instruction pipelining means having multiple instructions in different stages of execution as instructions are issued before the previous instruction has completed its execution;

pipelining will be studied in detail later. The RISC machines examine the instructions to check if operand fetches or branch instructions are involved. In such a case, the perands or the branch target instructions can be 'pre-fetched'. As instructions are issued before the preceding instructions have completed execution, the processor will not know in case of a conditional branch instruction, whether the condition will be met and the branch will be taken or not. But instead of waiting for this information to be available, the branch can be "speculated" as taken or not taken, and the instructions can be issued. Later if the speculation is found to be wrong, the results can be discarded and actual target instructions can be issued. These techniques help improve the performance of processors.

Q : Write RTL functions and there was a rb +rc instruction.

Answer:
Using RTL to describe the SRC RTL stands for Register Transfer Language. The Register Transfer Language provides a formal way for the description of the behavior and structure of a computer. The RTL facilitates the design process of the computer as it provides a precise, mathematical representation of its functionality. In this section, a Register Transfer Language is presented and introduced, for the SRC (Simple 'RISC' Computer), described in the previous discussion.

Behavioral RTL

Behavioral RTL is used to describe the 'functionality' of the machine only, i.e. what the machine does.

Structural RTL

Structural RTL describes the 'hardware implementation' of the machine, i.e. how the functionality made available by the machine is implemented.

Behavioral versus Structural RTL:

In computer design, a top-down approach is adopted. The computer design process typically starts with defining the behavior of the overall system. This is then broken down into the behavior of the different modules. The process continues, till we are able to define, design and implement the structure of the individual modules. Behavioral RTL is used for describing the behavior of machine whereas structural RTL is used to define the structure of machine, which brings us to the some more hardware features.

Using RTL to describe the static properties of the SRC

In this section we introduce the RTL by using it to describe the various static properties of the SRC.

Specifying Registers

The format used to specify registers is
Register Name<register bits>
For example, IR<31..0> means bits numbered 31 to 0 of a 32-bit register named "IR" (Instruction Register). "Naming" using the := naming operator: The := operator is used to 'name' registers, or part of registers, in the Register Transfer Language. It does not create a new register; it just generates another name, or "alias" for an already existing register or part of a register. For example, Op<4..0>: = IR<31..27> means that the five most significant bits of the register IR will be called op, with bits 4..0.

Fields in the SRC instruction

In this section, we examine the various fields of an SRC instruction, using the RTL.
op<4..0>: = IR<31..27>; operation code field
The five most significant bits of an SRC instruction, (stored in the instruction register in this example), are named op, and this field is used for specifying the operation.

ra<4..0>: = IR<26..22>; target register field
The next five bits of the SRC instruction, bits 26 through 22, are used to hold the address of the target register field, i.e., the result of the operation performed by the instruction is stored in the register specified by this field.
rb<4..0>: = IR<21..17>; operand, address index, or branch target register
The bits 21 through 17 of the instruction are used for the rb field. rb field is used to hold an operand, an address index, or a branch target register.
rc<4..0>: = IR<16..12>; second operand, conditional test, or shift count register
The bits 16 through 12, are the rc field. This field may hold the second operand, conditional test, or a shift count.
c1<21..0>: = IR<21..0>; long displacement field
In some instructions, the bits 21 through 0 may be used as long displacement field. Notice that there is an overlap of fields. The fields are distinguished in a particular instruction depending on the operation.
c2<16..0>: = IR<16..0>; short displacement or immediate field
The bits 16 through 0 may be used as short displacement or to specify an immediate operand. c3<11..0>: = IR<11..0>; count or modifier field
The bits 11 through 0 of the SRC instruction may be used for count or modifier field.

Describing the processor state using RTL

The Register Transfer Language can be used to describe the processor state. The following registers and bits together form the processor state set.
PC<31..0>; program counter (it holds the memory address of next instruction to be executed)
IR<31..0>; instruction register, used to hold the current instruction
Run; one bit run/halt indicator
Strt; start signal
R [0..31]<31..0>; 32, 32 bit general purpose registers

Q : how we speed-up a computer?

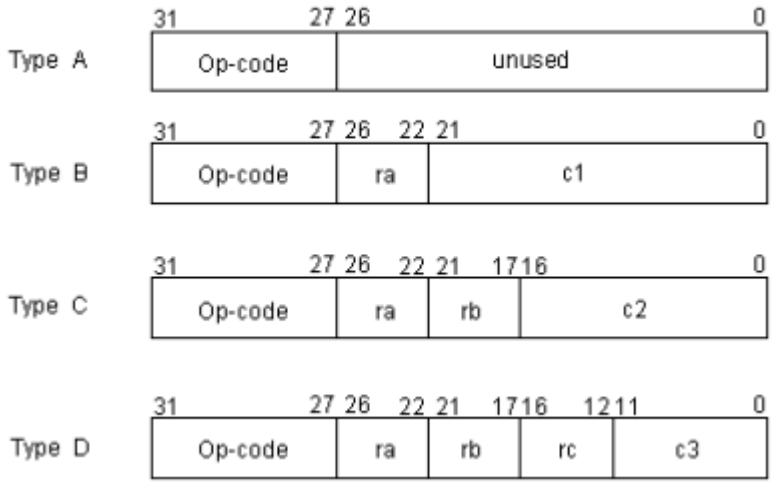
Answer:
Think beyond boundaries.

Q : Write execution time of an instruction(there was a description too)

Answer:
As we know, the execution time is dependent on the following three factors.
ET = IC x CPI x T
ET = CPI x IC x T = CPI x IC / f
where
CPI = clocks per instruction
IC = instruction count
T = time period of the clock,
and
f = frequency of the clock.

Q : Types of instructions

Answer:
Four types of instructions are supported by the SRC. Their representation is given in the figure shown.



Q : How you represent register data field?

Answer:

What is cu?Features of cu?

The Control Unit

The control unit is responsible for generating control signals as well as the timing signals.

Hence the control unit is responsible for the synchronization of internal as well as external events. By means of the control signals, the control unit instructs the data path what to do in every clock cycle during the execution of instructions.

Control Unit Design

Since the control unit performs quite complex tasks, its design must be done very carefully. Most errors in processor design are in the Control Unit design phase. There are primarily two approaches to design a control unit.

1. Hardwired approach
2. Micro programming

Hardwired approach is relatively faster, however, the final circuit is quite complex. The micro-programmed implementation is usually slow, but it is much more flexible.

"Finite-state machine" concepts are usually used to represent the CU. Every state corresponds to one "clock cycle" i.e., 1 state per clock. In other words each timing step could be considered as just 1 state and therefore from one timing step to other timing step, the state would change. Now, if we consider the control unit as a black box, then there would be four sets of inputs to the control unit. These are as follows:

1. The output of timing step generator (There are 8 disjoint timing steps in our example T0-T7).
2. Op-code (op-code is first given to the decoder and the output of the decoder is given to the control unit).
3. Data path generated signals, like the "CON" control signal,
4. Signals from external events, like "Interrupt" generated by the Interrupt generator.

The complexity of the control is a function of the

- Number of states
- Number of inputs to the CU

- Number of the outputs generated by the CU

Write RTL structural lang that is shlr ra, rb, c2

Step	RTL
T0-T2	Instruction fetch
T3	n<4..0> ← IR<4..0>;
T4	(N = 0) : (n<4..0> ← R[rc]<4..0>);
T5	C ← (Nα0) © R[rb]<31..N>;
T6	R[ra] ← C;

==========>

Short Question (Set-4)

Question No: 31 (Marks: 1)

How many bits are included in one 1KByte ?

Answer:

1024*8=8104 bits

Question No: 32 (Marks: 1)

In which type of interrupts, the address of the service routine needs to be supplied externally by the device?

Answer:

Hardware interrupts.

==========>

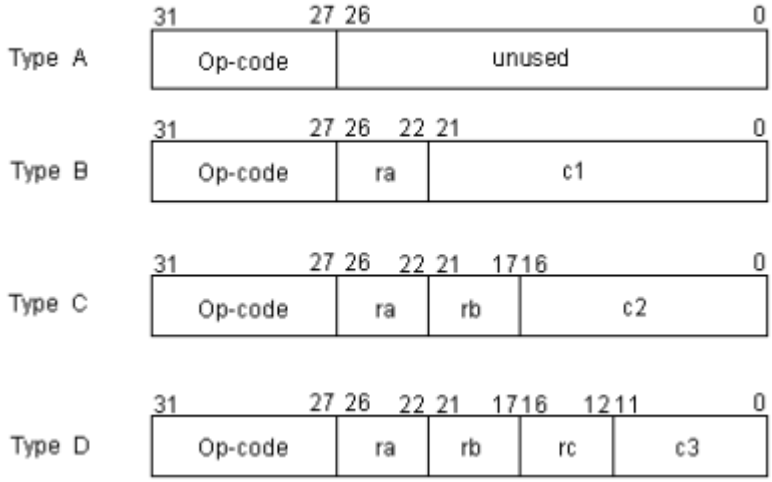
Short Question (Set-5)

How many types of instructions are available in SRC? Name them. What is the format of each of these instructions.....5marks

Answer:

Answer:

Four types of instructions are supported by the SRC. Their representation is given in the figure shown.



Write the Structural RTL for the call instruction for uni-bus data path implementation. call ra, rb.....5 marks

Answer:

Structural RTL for the call instruction

call ra, rb

Step	RTL
T0-T2	Instruction Fetch
T3	C ← PC;
T4	R[ra] ← C;
T5	C ← R[rb];
T6	PC ← C;

In this instruction we need to give the control to the procedure, sub-routine or to another address specified in the program. First three steps would fetch the call instruction. In step T3 we store the present contents of PC in to the buffer register C and then from C we transfer the data to the register ra in step T4. As a result register ra would contain the original contents of PC and this would be a pointer to come back after executing the sub-routine and it would be later used by a return instruction. In step T5 we take the contents of register rb, which would actually indicate to the point where we want to go. So in step T6 the contents of C are placed in PC and as a result PC would indicate the position in the memory from where new execution has to begin.

==========

Structural RTL for the in instruction

in ra, c2

First three steps would fetch the instruction In step T3 we take the IO [c2] which indicates that go to IO address indicated by c2 which is a positive constant in this case and then data would be taken to the buffer register C. In step T4 we would transfer the data from C to the destination register ra.

Step	RTL
T0-T2	Instruction fetch
T3	C ← IO[c2];
T4	R[ra] ← C

Structural RTL for the out instruction

out ra, c2

This instruction is opposite to the 'in' instruction. First three instructions would fetch the instruction. In step T3 the contents of register ra are placed in to the buffer register C and then in Step T4 from C the data is placed at the output port indicated by the c2 constant. So this instruction is just opposite to the 'in' instruction.

Step	RTL
T0-T2	Instruction fetch
T3	C ← R[ra];
T4	IO[c2] ← C

Structural RTL description for un-conditional jump instruction

jump [ra+c2]

In first three steps, T0-T2, we would fetch the jump instruction, while in T3 we would either take the contents of PC and place them in a temporary register A if the condition given in jump instruction is true, that is if the ra field is zero, otherwise we would place the contents of register ra in the temporary register A. Comma ',' indicates that these two instructions are concurrent and only one of them would execute at a time. If the ra field is zero then it would be PC-relative jump otherwise it would be register-relative jump. In step T4 we would add the constant c2 after sign-extension to the contents of temporary register A. As a result we would have the effective address in the buffer register C, to which we need to jump. In step T5 we will take the contents of C and load it in the PC, which would be the required address for the jump.

Step	RTL
T0-T2	Instruction Fetch
T3	(ra=0): A← PC, (ra≠0): A ← R[ra];
T4	C ← A + c2(sign extend);
T5	PC ← C;

Structural RTL for the shift instruction

shiftr ra, rb, c1

First three steps would fetch the shift instruction. c1 is the count field. It is a 5-bit constant and is obtained from the lower 5-bits of the instruction register IR. In step T3 we would load the 5-bit register 'n' from the count field or the lower 5-bits of the IR and then in T4 depending upon the value of 'N' which indicates the decimal value of 'n', we would take the contents of register rb and shift right by N-bits which would indicate how many shifts are to be performed. 'n' indicates the register while 'N' indicates the decimal value of the bits present in the register 'n'. So as a result we need to copy the zeros to the left most bits, this shows that zeros are replicated 'N' times and are concatenated with the shifted bits that are actually 15…N. In T5, we take the contents from C through the bus and feed it to the register ra which is the destination register. Other instructions that would have similar tables are 'shiftl' and 'asr'. In case of asr, when the data is shifted right, instead of copying zeros on the left side, we would copy the sign bit from the original data to the left-most position.

Step	RTL
T0-T2	Instruction fetch
T3	n<4..0> ← IR<4..0>;
T4	C ← (Nα0) © R[rb]<15..N>;
T5	R[ra] ← C;

Write the Structural RTL for the mov instruction for uni-bus data path implementation. mov ra, rb……3 marks

Answer:

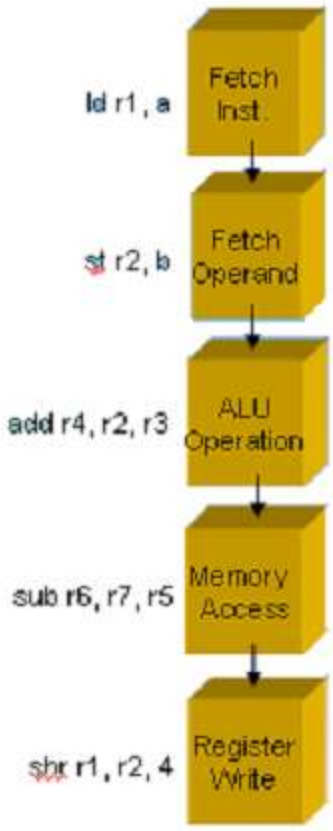
Step	RTL
T0-T2	Instruction fetch
T3	C ← R[rb];
T4	R[ra] ← C;

How many stages are in the pipelined version of SRC? Name them.....3 Marks

Answer:

Description of the five Pipeline Stages

- Instruction Fetch
- Fetch Operand
- ALU Operation
- Memory Access
- Register Write



1. Instruction fetch

As the name implies, the instruction is fetched from the instruction memory in this stage. The fetched instruction bits are loaded into a temporary pipeline register.

2. Instruction decode/operand fetch

In this stage the operands for the instruction are fetched from the register file. If the instruction is add r1, r2, r3 the registers r2 and r3 will be read into the temporary pipeline registers.

3. ALU5 operation

In this stage, the fetched operand values are fed into the ALU along with the function which is required such as addition, subtr is stored into temporary pipeline registers. In case of a memory access such as a load or a store instruction, the ALU calculates the effective memory address in this stage.

4. Memory access

For a load instruction, a memory read operation takes place. For a store instruction, a memory write operation is performed. If there is no memory access involved in the instruction, this stage is simply bypassed.

5. Register write

The result is stored in the destination register in this stage.

Latency & throughput

Latency is defined as the time required processing a single instruction, while throughput is defined as the number of instructions processed per second.

Write the Structural RTL for the 'not instruction'.....2 marks

Answer:

not (op-code = 23) The not instruction inverts the operand register's value and assigns it back to the same register, as shown in the example :

not r6

R[6] ← ! R[6]

==========

Seven instructions of the processor are of type Y. These are

• add(op-code=11)
The type Y add instruction adds register ra's contents to register R0. For example,
add r1
In the behavioral RTL, we show this as
R[0] ← R[1]+R[0]
and(op-code=19)
This instruction obtains the logical AND of the value stored in register specified by field ra and the register R0, and assigns the result to R0, as shown in the example:
and r5
which is represented in RTL as
R[0] ← R[1]&R[0]
• div(op-code=16)
This instruction divides the contents of register R0 by the value stored in the register ra, and assigns result to R0. The remainder is stored in the divisor register, as shown in example,
div r6
In RTL, this is
R[0] ← R[0]/R[6]
R[6] ← R[0]%R[6]
• mul (op-code = 15)
This instruction multiplies the values stored in register R0 and the operand register, and assigns the result to R0). For example,
mul r4
In RTL, we specify this as
R[0] ← R[0]*R[4]
• not (op-code = 23)
The not instruction inverts the operand register's value and assigns it back to the same register, as shown in the example
not r6
R[6] ← ! R[6]
• or (op-code=21)
The or instruction obtains the bit-wise OR of the operand register's and R0's value, and assigns it back to R0. An example,
or r5
R[0] ← R[0] ~ R[5]
• sub (op-code=12)
The sub instruction subtracts the value of the operand register from R0 value, assigning it back to register R0. Example:
sub r7
In RTL:
R[0] ← R[0] – R[7]
mov (op-code = 0)
The contents of one register are copied to the destination register ra.
Example: mov r5, r1
RTL Notation: R[5]← R[1]
Type W
Again, only one instruction belongs to this type. It is the branch instruction
• br (op-code = 252)

This is the unconditional branch instruction, and the branch target is specified by the 8-bit immediate field. The branch is taken by incrementing the PC with the new value. Hence it is a 'near' jump. For instance,
br 14
PC ← PC+14
Type V
Most of the instructions of the processor EAGLE are of the format type V. These are
• addi (op-code = 13)
The addi instruction adds the immediate value to the register ra, by first sign-extending the immediate value. The result is also stored in the register ra. For example,
addi r4, 31
In behavioral RTL, this is
R[4] ← R[4]+(8ac<7>)©c<7…0>;
• andi (op-code = 20)
Logical 'AND' of the immediate value and register ra value is obtained when this instruction is executed, and the result is assigned back to register ra. An example,
andi r6, 1
R[6] ← R[6] &1
• in (op-code=29)
This instruction is to read in a word from an IO device at the address specified by the immediate field, and store it in the register ra. For instance,
in r1, 45
In RTL this is
R[1] ← IO[45]
• load (op-code=8)
The load instruction is to load the memory word into the register ra. The immediate field specifies the location of the memory word to be read. For instance,
load r3, 6
R[3] ← M[6]
• brn (op-code = 28)
Upon the brn instruction execution, the value stored in register ra is checked, and if it is negative, branch is taken by incrementing the PC by the immediate field value. An example is
brn r4, 3
In RTL, this may be written as
if R[4]<0, PC ← PC+3
• brnz (op-code = 25)
For a brnz instruction, the value of register ra is checked, and if found non-zero, the PC-relative branch is taken, as shown in the example,
brnz r6, 12
Which, in RTL is
if R[6]!=0, PC ← PC+12
brp (op-code=27)
brp is the 'branch if positive'. Again, ra value is checked and if found positive, the PC-relative near jump is taken, as shown in the example:
brp r1, 45
In RTL this is

if R[1]>0, PC ← PC+45

- brz (op-code=8)

In this instruction, the value of register ra is checked, and if it equals zero, PC-relative branch is taken, as shown,

brz r5, 8

In RTL:

if R[5]=0, PC ← PC+8

- loadi (op-code=9)

The loadi instruction loads the immediate constant into the register ra, for instance,

loadi r5,54

R[5] ← 54

- ori (op-code=22)

The ori instruction obtains the logical 'OR' of the immediate value with the ra register value, and assigns it back to the register ra, as shown,

ori r7, 11

In RTL,

R[7] ← R[7]~11

- out (op-code=30)

The out instruction is used to write a register word to an IO device, the address of which is specified by the immediate constant. For instance,

out 32, r5

In RTL, this is represented by

IO[32] ← R[5]

- shiftl (op-code=17)

This instruction shifts left the contents of the register ra, as many times as is specified through the immediate constant of the instruction. For example:

shiftl r1, 6

- shiftr(op-code=18)

This instruction shifts right the contents of the register ra, as many times as is specified through the immediate constant of the instruction. For example:

shiftr r2, 5

- store (op-code=10)

The store instruction stores the value of the ra register to a memory location specified by the immediate constant. An example is,

store r4, 34

RTL description of this instruction is

M[34] ← R[4]

- subi (op-code=14)

The subi instruction subtracts the immediate constant from the value of register ra, assigning back the result to the register ra. For instance,

subi r3, 13

mnemonic	opcode	operand1 3 bits	operand2 3 bits	constant 8 bits	Format	Behavioral RTL
add	01011	ra	-	-	Y	R [0] ← R [ra]+R [0];
addi	01101	ra	-	c	V	R [ra] ← R [ra]+(8αc<7>)©c;
and	10011	ra	-	-	Y	R[0] ← R[ra]&R[0];
andi	10100	ra	-	c	V	R [ra] ← R [ra]& (8αc<7>)©c;
br	11111100	-	-	c	W	PC ← PC+(8αc<7>)©c;
brnv	11100	ra	-	c	V	(R [ra]<0): PC ← PC+(8αc<7>)©c;
brnz	11001	ra	-	c	V	(R [ra]<>0): PC ← PC+(8αc<7>)©c;
brpl	11011	ra	-	c	V	(R [ra]>0): PC ← PC+(8αc<7>)©c;
brzr	11010	ra	-	c	V	(R [ra]=0): PC ← PC+(8αc<7>)©c;
div	10000	ra	-	-	Y	R [0] ← R [0]/R [a], R [ra] ←R [0]%R [ra],
halt	11111010	-	-	-	Z	RUN← 0;
in	11101	ra	-	c	V	R [ra] ←IO[c];
init	11111011	-	-	-	Z	R [7…0] ← 0;
load	01000	ra	-	c	V	R [ra] ←M[c];
loadi	01001	ra	-	c	V	R [ra] ← (8αc<7>)©c;
mov	00	ra	rb	-	X	R [ra] ← R [rb];
mul	01111	ra	-	-	Y	R [ra] © R [r0] ← R [ra]*R [0];
nop	11111001	-	-	-	Z	;
not	10111	ra	-	-	Y	R [ra] ←! (R [ra]);
or	10101	ra	-	-	Y	R [0] ← R [ra]~R [0];
ori	10110	ra	-	c	V	R [ra] ← R [ra]~ (8αc<7>)©c;
out	11110	ra	-	c	V	IO[c] ←R [ra];
reset	11111000	-	-	-	Z	TBD;
shiftl	10001	ra	-	c	V	R [ra] ← R [ra]<(7-n)..0>©(nα0);
shiftr	10010	ra	-	c	V	R [ra] ← (nα0)©R [ra]<7…n>;
store	01010	ra	-	c	V	M[c]← R [ra];
sub	01100	ra	-	-	Y	R [0] ← R [0]-R [a];
subi	01110	ra	-	c	V	R [ra] ← R [ra]- (8αc<7>)©c;

Symbol	Meaning	Symbol	Meaning
α	Replication	%	Remainder after integer division
©	Concatenation	&	Logical AND
:	Conditional constructs (IF-THEN)	~	Logical OR
;	Sequential constructs	!	Logical NOT or complement
,	Concurrent constructs	←	LOAD or assignment operator

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Short Question (Set-6)

A question about to define the shift right instruction ? (2 Marks)

Answer:
SHIFT instructions move a bit string (or operand treated as a bit string) to the right or left, with excess bits discarded (although one or more bits might be preserved in flags). SHIFT instructions are useful in many ways. e.g., if you multiply two 16 bit numbers the result will be of 32 bit number, so shift is used to adjust the result in the two 16 bit

registers. Also, as to multiply or divide by 2, SHIFT Left or SHIFT Right instructions are used.

Right shift instruction shifts the bits to the right side as per command.

Shfr z, a, 16

This command will shift a to right side 16 bits, and assign the value to z

Structural RTL instructions definition? (3 Marks)

Answer:

Answered Above.

Write the Structural RTL description for un-conditional jump instruction for uni-bus data path implementation. (5 Marks) ??????

Answer:

Answered above.

Define two hazards in pipelining and how can to overcome these. (5 Marks)

Answer:

In accordance with the chosen data path implementation, the structural RTL for every instruction is described in this step. The structural RTL is formed according to the proposed micro-architecture which includes many hidden temporary registers necessary for instruction execution. Since the structural RTL shows the actual implementation steps, it should satisfy the time and space requirements of the CPU as specified by the clocking interval and the number of registers and buses in the data path.

Pipeline Hazards

The instructions in the pipeline at any given time are being executed in parallel. This parallel execution leads to the problem of instruction dependence. A hazard occurs when an instruction depends on the result of previous instruction that is not yet complete.

Classification of Hazards

There are three categories of hazards

1. Branch Hazard
2. Structural Hazard
3. Data Hazard

Branch hazards

The instruction following a branch is always executed whether or not the branch is taken.

This is called the branch delay slot. The compiler might issue a nop instruction in the branch delay slot. Branch delays cannot be avoided by forwarding schemes.

Structural hazards

A structural hazard occurs when attempting to access the same resource in different ways at the same time. It occurs when the hardware is not enough to implement pipelining properly e.g. when the machine does not support separate data and instruction memories.

Data hazards

Data hazard occur when an instruction attempts to access some data value that has not yet been updated by the previous instruction. An example of this RAW (read after write) data hazard is;

200: add r2, r3, r4
204: sub r7, r2, r6

The register r2 is written in clock cycle 5 hence the sub instruction cannot proceed beyond stage 2 until the add instruction leaves the pipeline.

Data Hazard Detection & Correction

Data hazards can be detected easily as they occur when the destination register of an instruction is the same as the source register of another instruction in close proximity. To remedy this situation, dependent instructions may be delayed or stalled until the ones ahead complete. Data can also be forwarded to the next instruction before the current instruction completes, however this requires forwarding hardware and logic. Data can be forwarded to the next instruction from the stage where it is available without waiting for the completion of the instruction. Data is normally required at stage 2 (operand fetch) however data is earliest available at stage 3 output (ALU result) or stage 4 output (memory access result). Hence the forwarding logic should be able to transfer data from stage 3 to stage 2 or from stage 4 to stage 2.

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Short Question (Set-7)

What is relation b/w data path and control unit in SRC processors…….2marks

Answer:

2. Define Pre-fetching……..2marks

Answer:

The RISC machines examine the instructions to check if operand fetches or branch instructions are involved. In such a case, the operands or the branch target instructions can be ‘pre-fetched’.

5. Write the Structural RTL for “call ra, rb”…….5marks

Answer:

Step	RTL
T0-T2	Instruction Fetch
T3	C ← PC;
T4	R[ra] ← C;
T5	C ← R[rb];
T6	PC ← C;

==========>

Short Question (Set-9)

Q no 1: Define Control unit. (2 marks)

Answer:

The design process

The control unit is responsible for generating control signals as well as the timing signals. Hence the control unit is responsible for the synchronization of internal as well as external events. By means of the control signals, the control unit instructs the data path what to do in every clock cycle during the execution of instructions.

Q no 2:How can you define Microprogram (2 marks)

Answer:

In the previous lectures, we have discussed how to implement logic circuitry for a control unit based on logic gates. Such an implementation is called a hardwired control unit. In a micro programmed control unit, control signals which need to be generated at a certain time are stored together in a control word. This control word is called a microinstruction.

A collection of microinstructions is called a microprogram. These microprograms generate the sequence of necessary control signals required to process an instruction. These microprograms are stored in a memory called the control store.

As described above microprogramming or microcoding is an alternative way to design the control unit. The microcoded control unit is itself a small stored program computer consisting of

ƒ Micro-PC

ƒ Microprogram memory

ƒ Microinstruction word

1. How many types of instructions are available in SRC? Name them. What is the format of each of these instructions.....5marks

Answer:

Discussion4-address instruction

- The code size

is 13 bytes (1+3+3+3+3 = 13 bytes)

- Number of bytes accessed from memory is 22 (13 bytes for instruction fetch + 6 bytes for source operand fetch + 3 bytes for storing destination operand = 22 bytes)

Note that there is no need for an additional memory access for the operand corresponding to the next instruction, as it has already been brought into the CPU during instruction fetch.

3-address instruction

- The code size is 10 bytes (1+3+3+3 = 10 bytes)
- Number of bytes accessed

from memory is 19 (10 bytes for instruction fetch + 6 bytes for source operand fetch + 3 bytes for storing destination operand = 19 bytes)

2-address instruction

- The code size is 7 bytes (1+3+3 = 7 bytes)
- Number of bytes accessed from memory is 16(7 bytes for instruction fetch + 6 bytes for source operand fetch + 3 bytes for storing destination operand = 16 bytes)

1-address instruction

- The code size is 4 bytes (1+3= 4 bytes)
- Number of bytes accessed from memory is 7 (4 bytes for instruction fetch + 3 bytes for source operand fetch + 0 bytes for storing destination operand = 7 bytes)

0-address instruction

- The code size is 1 byte
- Number of bytes accessed from memory is 10 (1 byte for instruction fetch + 6 bytes for source operand fetch + 3 bytes for storing destination operand = 10 bytes)

The following table summarizes this information

Instruction Format	Code size	Number of memory bytes
4-address instruction	13	22
3-address instruction	10	19
2-address instruction	7	16
1-address instruction	4	7
0-address instruction	1	10

Q no5

what are the types of SRC?Name them? also explain its format? (5 marks)

Answer:

==========>

Short Question (Set-11)

Question No: 17 (Marks: 2)

Write the following statement of an Arithmetic Instruction using RTL.

If op-code is 0, the instruction is 'add'. The values in register rb and rc are added and the result is stored in register rc

Sol.

(op<4..0>=0):R[ra] ← R[rb]+R[rc]

Question No: 18 (Marks: 2)

Given below are the various fields of an SRC instruction register.

a) operation code field : **op<4..0>**
b) target register field : **ra<4..0>**
c) operand, address index, or branch target register : **rb<4..0>**
d) second operand, conditional test, or shift count register: **rc<4..0>**

Rewrite these various fields of an SRC instruction, using the **RTL.**

Sol.

op<4..0>:=IR<31..27>
ra<4..0>:= IR<26..22>
rb<4..0>:= IR<21..17>
rc<4..0>:= IR<16..12>

Question No: 20 (Marks: 3)

What is the role of timing step generator in a processor?

Sol.

To ensure the correct and controlled execution of instructions in a program, and all the related operations, a timing device is required. This is to ensure that the operations of essentially different instructions do not mix up in time. There exists a 'timing step generator' that provides mutually exclusive and sequential timing intervals. This is analogous to the clock cycles in the actual processor. A possible implementation of the timing step generator is shown in the figure. Each mutually exclusive step is carried out in one timing interval. The timing intervals can be named T0, T1…T7. The given figure is helpful in understanding the 'mutual exclusiveness in time' of these timing intervals.

Question No: 22 (Marks: 5)
Write the Structural RTL description for un-conditional jump instruction for uni-bus data path implementation.

jump [ra+c2]

step	RTL
T0-T2	Instruction fetch
T3	(ra=0):A←PC, (ra≠0):A←R[ra]
T4	C←A+c2(sign extend)

T5	PC←C

Question No: 23 (Marks: 5)

What is Control Unit?features of CU?

Difference b/w soft and hard reset operation in SRC

write RTL structual lang that is shlr ra, rb, c2

Difference b/w hardwired CU and Micro-Programmed CU.

What is reset operation and what does it?

define Latency and throughput.

Reverse assemble the following SRC machine language instructions:
68C2003A h

Question No: 46

Give control signals for the addi instructions.

Note: Fill the given table only. If you require other control signals to complete the table, do it as rough work. Marks will be given only for the required fields in the table.

Question No: 47

Explain the complications related to pipelining Question 4

Question No: 65

Briefly describe five important features of RISC machines.

RISC and CISC architectures:

Generally, computers can be classified as being RISC machines or CISC machines. These concepts are explained in the following discussion.

RISC (Reduced instruction set computers)

RISC is more of a philosophy of computer design than a set of architectural features. The underlying idea is to reduce the number and complexity of instructions. However, new RISC machines have some instructions that may be quite complex and the number of instructions may also be large.

The common features of RISC machines are

- **One instruction per clock period**
- **Fixed size instructions**
- **CPU accesses memory only for Load and Store operations**
- **Simple and few addressing modes**
- **Less work per instruction**
- **Improved usage of delay slots**
- **Efficient usage of Pre-fetching and Speculative Execution Techniques**

CISC (Complex Instruction Set Computers)

The complex instruction set computers does not have an underlying philosophy. The CISC machines have resulted from the efforts of computer designers to efficiently utilize memory and minimize execution time, yet add in more instruction formats and addressing modes.

The common attributes of CISC machines are discussed below.

- **Variable instruction lengths and execution times per instruction**
- **More work per instruction**
- **Wide variety of addressing modes**
- **CISC machines attempt to reduce the "semantic gap"**
- **Clock period T, cannot be reduced beyond a certain limit**
- **Complex addressing modes delay operand fetch from memory**

Question No: 78

What is a non-maskable interrupt (NMI) and what is its role

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Short Question (Set-12)

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Short Question (Set-13)

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Short Question (Set-14)

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MCQz

MCQz (Set-1)

Question # 1 of 10 (Start time: 12:51:35 AM)

Which one of the following registers store a previously calculated value or a value loaded from the main memory?

Select correct option:

- **Accumulator** *see explanation below*
- Address Mask not found in the handout/book
- Instruction Register
- Program Counter

*The instruction that is to be executed is fetched from the memory and temporarily stored in a CPU register, called the **instruction register (IR).** The instruction register holds the instruction while it is decoded and executed by the central processing unit (CPU) of the computer. However, before loading an instruction into the instruction register for execution, the computer needs to know which instruction to load.*

*The **program counter (PC**), also called the instruction pointer in some texts, is the register that holds the address of the next instruction in memory that is to be executed.*

*In case of branch instructions, the contents of the PC are replaced by the address of the next instruction contained in the present branch instruction, and the current status of the processor is stored in a register called the **Processor Status Word (PSW).** Another name for the PSW is the **flag register**.*

*The accumulator holds one of the operands; one more register may be required to hold the address of another operand. The **accumulator** is not used to hold an address. So accumulator based machines are also called 1-address machines.*

Question # 2 of 10 (Start time: 12:50:20 AM)

For any of the instructions that are a part of the instruction set of the SRC, there are certain _____required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.

Select correct option:

- Registers
- **Control signals**
- Memory
- None of the given

Then there are the control signals that form the interface between the data path and the control unit. These control signals move data onto buses, enable and disable flip-flops, specify the ALU functions and control the buses and memory operations. Hence an integral

part of the data path design is the seamless embedding of the control signals into it. ***Page 151***

Question # 3 of 10 (Start time: 12:47:17 AM)

Which one of the following portions of an instruction represents the operation to be performed?

Select correct option:

- Address
- Instruction code
- **Opcode**
- Operand

Op-code *(op-code is first given to the decoder and the output of the decoder is given to the control unit).page 188*

an opcode (operation code) is the portion of a machine language instruction that specifies the operation to be performed. Their specification and format are laid out in the instruction set architecture of the processor in question (which may be a general CPU or a more specialized processing unit). Apart from the opcode itself, an instruction normally also has one or more specifiers for operands (i.e. data) on which the operation should act, although some operations may have implicit operands, or none at all. There are instruction sets with nearly uniform fields for opcode and operand specifiers, as well as others (the x86 architecture for instance) with a more complicated, varied length structure.

Question #4 of 10 (Start time: 12:49:08 AM)

The external interface of FALCON-A consists of a _____ address bus and a data bus.

Select correct option:

- 8-bit. 8-bit
- **16-bit. 16-bit**
- 16-bit. 24-bit
- 16-bit. 32-bit

The external interface consists of a 16-bit address bus, a 16-bit data bus and a control bus on which different control signals like MRead, MWrite, IORead, IOWrite are present. ***Page 169.***

Question # 5 of 10 (Start time: 12:43:40 AM)

FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC ____ wide.

Select correct option:

- 8-bits
- 16-bits
- **32-bits**
- 64-bits

Comparing the uni-bus implementation of FALCON-A with that of SRC results in the following differences: ***(Page-159)***

- ***FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is 32-bits wide.***
- *All registers of FALCON-A are of 16-bits while in case of SRC all registers are 32-bits.*
- *Number of registers in FALCON-A are 8 while in SRC the number of registers is 32.*
- *Special registers i.e. Program Counter (PC) and Instruction Register (IR) are 16-bit registers while in SRC these are 32-bits.*
- *Memory Address Register (MAR) and Memory Buffer Register (MBR) are also of 16-bits while in SRC these are of 32-bits*

Question # 6 of 10 (Start time: 12:46:08 AM)

Which one of the following registers holds the instruction that is being executed?

Select correct option:

- Accumulator
- Address Mask
- **Instruction Register**
- Program Counter

For reference read first page

Question # 7 of 10 (Start time: 12:44:41 AM)

Which of the following registers is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?

Select correct option:

- Instruction Register
- Memory address register
  Memory Buffer Register
- **Registers A and C**

(Page 153)

Overview of the Unibus SRC Data Path

The 1-bus implementation of the SRC data path is shown in the figure given.

The control signals are omitted here for the sake of simplicity. Following units are present in the SRC data path.

1. The Register File The general-purpose register file includes 32 registers R0 to R31 each 32 bit wide. These registers communicate with other components via the internal processor bus.

2. MAR

The Memory Address Register takes input from the ALSU as the address of the memory location to be accessed and transfers the memory contents on that location onto the memory sub-system.

3. MBR

The Memory Buffer Register has a bi-directional connection with both the memory sub-system and the registers and ALSU. It holds the data during its transmission to and from memory.

4. PC

The Program Counter holds the address of the next instruction to be executed. Its value is incremented after loading of each instruction. The value in PC can also be changed based on a branch decision in ALSU. Therefore, it has a bi-directional connection with the internal processor bus.

5. IR

The Instruction Register holds the instruction that is being executed. The instruction fields are extracted from the IR and transferred to the appropriate registers according to the external circuitry (not shown in this diagram).

6. Registers A and C

The registers A and C are required to hold an operand or result value while the bus is busy transmitting some other value. Both these registers are programmer invisible.

7. ALSU

There is a 32-bit Arithmetic Logic Shift Unit, as shown in the diagram. It takes input from memory or registers via the bus, computes the result according to the control signals applied to it, and places it in the register C, from where it is finally transferred to its destination.

Question # 8 of 10 (Start time: 12:54:10 AM)

_____ **control signal allows the contents of the Program Counter register to written onto the internal processor bus.**

Select correct option:

- INC4
- LPC
- **PCout**
- LC

To provide data to the bus through tri-state buffers we need to activate the 'out' control signal named as ***'PCout'****, making contents of the PC available to the ALSU and so control unit provides the increment signal 'INC2' to increment the PC.* ***(Page 168)***

See also at page no 174

We require four control signals to be issued in the time step T0:

PCout*: This control signal allows the contents of the Program Counter register to be written onto the internal processor bus.*

LMAR: This signal enables write onto the memory address register (MAR), thus the value of PC that is on the bus, is copied into this register

INC4*: It lets the PC value to be incremented by 4 in the ALSU, and result to be stored in C. Notice that the value of PC has been received by the ALSU as an operand. This control signal allows the constant 4 to be added to it.*

The ALSU is assumed to include an INC4 function

***LC**: This enables the input to the register C for writing the incremented value of PC onto it.*
During the time step T1, the following control signals are applied:
LMBR: This enables the "write" for the register MBR. When this signal is activated, whatever value is on the bus, can be written into the MBR.
MRead: Allow memory word to be gated from the external CPU data bus into the MBR.
MARout: This signal enables the tri-state buffers at the output of MAR.
Cout: This will enable writing of the contents of register C onto the processor's internal data bus.
***LPC**: This will enable the input to the PC for receiving a value that is currently on the internal processor bus. Thus the PC will receive an incremented value.*
At the final time step, T2, of the instruction fetch phase, the following control signals are issued:
MBRout: To enable the tri-state buffers with the MBR.
LIR: To allow the IR read the value from the internal bus. Thus the instruction stored in the MBR is read into the Instruction Register (IR)

Question # 9 of 10 (Start time: 12:47:51 AM)
What is the instruction length of the FALCON-A processor?
Select correct option:

- 8 bits
- **16 bits**
- 32 bits
- 64 bits

A summary of the instruction lengths of our processors is given in the table below.

EAGLE	FALCON-A	FALCON-E	SRC
Fixed 16 bits	Fixed 16 bits	Fixed 32 bits	Fixed 32 bits

Fig. Instruction Length

Question # 10 of 10 (Start time: 12:52:50 AM)
_____ control signal enable the input to the PC for receiving a value that is currently on the internal processor bus.
Select correct option:

LPC

- INC4
- LC
- Cout
- I

- ***LPC**: This will enable the input to the PC for receiving a value that is currently on the internal processor bus. Thus the PC will receive an incremented value.* ***See page no 173.***

==========

Question # 1 of 10 (Start time: 07:19:15 PM) Total Marks: 1

What is the instruction length of the FALCON-E processor?

Select correct option:

- 8 bits
- 16 bits
- **32 bits see table above.**
- 64 bits

Question # 2 of 10 (Start time: 07:19:35 PM) Total Marks: 1

_____ **control signal allows the contents of the Program Counter register to be written onto the internal processor bus.**

Select correct option:

- INC4
- LPC
- **PCout**
- LC

Question # 3 of 10 (Start time: 07:20:12 PM) Total Marks: 1

What is the instruction length of the FALCON-A processor?

Select correct option:

- 8 bits
- **16 bits see table above.**
- 32 bits
- 64 bits

Question # 4 of 10 (Start time: 07:20:23 PM) Total Marks: 1

Motorola MC68000 is an example of ---------microprocessor.

Select correct option:

- **CISC**
- RISC
- SRC
- FALCON

Question # 5 of 10 (Start time: 07:21:08 PM) Total Marks: 1

FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is _____ wide.

Select correct option:

8-bits

16-bits

32-bits

64-bits

Question # 6 of 10 (Start time: 07:21:20 PM) Total Marks: 1

Which one of the following registers holds the instruction that is being executed?

Select correct option:

Accumulator

Address Mask

Instruction Register

Program Counter

Question # 7 of 10 (Start time: 07:21:58 PM) Total Marks: 1

Which one of the following portions of an instruction represents the operation to be performed?

Select correct option:

Address

Instruction code

Opcode

Operand

Question # 8 of 10 (Start time: 07:22:13 PM) Total Marks: 1

Which one of the following registers stores a previously calculated value or a value loaded from the main memory?

Select correct option:

Accumulator

Address Mask

Instruction Register

Program Counter

Question # 9 of 10 (Start time: 07:22:31 PM) Total Marks: 1

The external interface of FALCON-A consists of a _____address bus and a _____ data bus.

Select correct option:

8-bit , 8-bit

16-bit , 16-bit

16-bit , 24-bit

16-bit , 32-bit

Question # 10 of 10 (Start time: 07:23:31 PM) Total Marks: 1

P: R3 <- R5 MAR <- IR These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?

Select correct option:

Parentheses ()

Arrow <-

Colon :

Comma ,

The displacement (or the direct) address is being calculated in this example. The ","

operator separates statements in a single instruction, and indicates that these tatements are to be executed simultaneously. However, since in this example these are two disjoint conditions, therefore, only one action will be performed at one time. Page (67)

Question # 1 of 10 (Start time: 05:34:30 PM) Total Marks: 1
Type A of SRC has which of the following instructions? a) andi, instruction b) No operation or nop instruction c) lar instruction d) ldr instruction e) Stop operation or stop instruction
Select correct option:
(a)& (b)
(b)&(c)
(a)&(e)
(b)&(e)

Type A is used for only two instructions:
- **No operation or nop, for which the op-code = 0. This is useful in pipelining**
- **Stop operation stop, the op-code is 31 for this instruction.**

Both of these instructions do not need an operand (are 0-operand instructions).Page 45

Question # 2 of 10 (Start time: 05:36:02 PM) Total Marks: 1
What functionality is performed by the instruction "lar R3, 36" of SRC?
Select correct option:
It will load the register R3 with the contents of the m
It will load the register R3 with the relative address i
It will load the register R3 with the relative address itself (PC+36).
It will store the register R3 contents to the memory lo
No operation

Question # 3 of 10 (Start time: 05:37:18 PM) Total Marks: 1
Which one of the following is a bi-stable device, capable of storing one bit of Information?
Select correct option:
Decoder
Flip-f lop
Flip-Flop
Multiplexer
Diplexer

Question # 4 of 10 (Start time: 05:37:50 PM) Total Marks: 1
What does the word „D" in the „D-flip-Flop" stands for?
Select correct option:
Data
Data
Digital
Dynamic
Double

Question # 5 of 10 (Start time: 05:38:23 PM) Total Marks: 1
Which type of instructions enables mathematical computations?
Select correct option:
Arithmetic
Arithmetic
Control
Data transfer
None of the given

Question # 6 of 10 (Start time: 05:39:02 PM) Total Marks: 1
In which one of the following addressing modes, the value to be stored in memory is obtained by directly retrieving it from another memory location?
Select correct option:
Direct Addressing Mode
Immediate addressing mode
Indirect Addressing Mode**not confirm**
Register (Direct) Addressing Mode

Question # 7 of 10 (Start time: 05:40:34 PM) Total Marks: 1
Which instruction is used to store register to memory using relative address?
Select correct option:
ld instruction
ldr instruction
lar instruction
str instruction
str instruction
The str is used to store register to memory using relative address (op-code = 4) Page 46

Question # 8 of 10 (Start time: 05:41:26 PM) Total Marks: 1
Which one of the following circuit design levels is called the gate level?
Select correct option:
Logic Design Level
Logic Design Level
Circuit Level
Mask Level
None of the given

Question # 9 of 10 (Start time: 05:42:00 PM) Total Marks: 1
In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?
Select correct option:
Arithmetic/logic
Load/store
Load/Store
Test/branch
None of the given

Question # 10 of 10 (Start time: 05:43:29 PM) Total Marks: 1
An "assembler" that runs on one processor and translates an assembly language program written for another processor into the machine language of the other processor is called a ----------
Select correct option:
compiler
cross assembler
Cross Assembler
debugger
linker

==========

Question # 1
Which operator is used to 'name' registers, or part of registers, in the Register Transfer Language?
Select correct option:
:= Page 65
&
%
©

Question # 2
Which field of the machine language instruction is the "type of operation" that is to be performed?
Select correct option:
Op-code (or the operation code)____page 31
CPU registers
Memory cells
I/O locations

Question # 3
Execution time of a program with respect to the processor is calculated as:
Select correct option:
Execution Time = IC x CPI x MIPS
Execution Time = IC x CPI x T
Execution Time = CPI x T x MFLOPS
Execution Time = IC x T

Question # 4
An "assembler" that runs on one processor and translates an assembly language program written for another processor into the machine language of the other processor is called a ----------
Select correct option:

compiler
cross assembler
debugger
linker

Question # 5
In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?
Select correct option:
Arithmetic/logic
Load/store
Test/branch
None of the given

Question # 6
Which one of the following circuit design levels is called the gate level?
Select correct option:
Logic Design Level
Circuit Level
Mask Level
None of the given

Question # 7
Which type of instructions load data from memory into registers, or store data from registers into memory and transfer data between different kinds of special-purpose registers?
Select correct option:
Arithmetic
Control
Data transfer
Floating point

Question # 9
Almost every commercial computer has its own particular ---------- language
Select correct option:
3GL
English language
Higher level language
assembly language

Question # 10
Which one of the following is the highest level of abstraction in digital design in

which the computer architect views the system for the description of system components and their interconnections?

Select correct option:

Processor-Memory-Switch level (PMS level)

Instruction Set Level

Register Transfer Level

None of the given

==========

Question No: 1

What is the instruction length of the SRC and Falcon E processor?

_ 8 bits

_ 16 bits

_ 32 bits

_ 64 bits

Question No: 2

Which one of the following is the memory organization of FALCON-E processor?

_ 2^8 * 8 bits

_ 2^{16} * 8 bits

_ 2^{32} * 8 bits

_ 2^{64} * 8 bits

Question No: 3

"If P = 1, then load the contents of register R1 into register R2".

This statement can be written in RTL as:

_ R1 ¬ R2

_ P: R1 ¬ R2

_ P: R2 ¬ R1

_ P: R2 ¬ R1, P: R1 ¬ R2

Question No: 4

The instruction ----------will load the register R3 with the contents of the memory location M [PC+56]

___Add R3, 56

___lar R3, 56

___ldr R3, 56

___str R3, 56

Question No: 5

----------are faster than cache memory

° Accumulator register

° CPU registers

° I/O devices

° ROM

P: R3 ¬ R5

MAR ¬ IR
These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?
_ Arrow ¬
_ Colon :
_ Comma ,
_ Parentheses ()

Question No: 7
Prefetching can be considered a primitive form of----------
___Pipelining Page 40
___Multi-processing
___Self-execution
___Exception

Question No: 8
The processor must have a way of saving information about its state or context so that itcan be restored upon return from the ----------
___Exception
___Function
___Stack
___Thread

Question No: 9
Which one of the following circuit design levels is called the gate level?
_____Logic Design Level
_____Circuit Level
_____Mask Level
_____None of the given

Question No: 10
_____ enable the input to the PC for receiving a value that is currently on the internal processor bus.
_ LPC
_ INC4
_ LC
_ Cout

Question No: 11
_____ operation is required to change the processor's state to a known, defined value.
_ Change
_ Reset
_ Update
_ None of the given
Question No: 12
There are _____ types of reset operations in SRC

_ Two (Hard and Soft Reset)
_ Three
_ Four
_ Five

Question No: 13
_____ controller controls the sequence of the flow of microinstructions.
_ Multiplexer
_ Microprogram
_ ALU
_ None of the given

Question No: 14
FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is _____ wide.
_ 8-bits
_ 24-bits
_ 32-bits
_ 64-bits

Question No: 15
Which of the following statement(s) is/are correct about Reduced Instruction Set Computer (RISC) architectures.
(i) The typical RISC machine instruction set is small, and is usually a subject of a CISC instruction set.
(ii) No arithmetic or logical instruction can refer to the memory directly.
(iii) A comparatively large number of user registers are available.
(iv) Instructions can be easily decoded through hard-wired control units.
_ (i) and (iii) only
_ (i), (iii) and (iv)
_ (i), (ii) and (iii) only
_ (i),(ii),(iii) and (iv)

Question No: 16
Which one of the following register holds the instruction that is being executed?

_ Accumulator
_ Address Mask
_ Instruction Register
_ Program Counter

==========>

MCQz (Set-2)

Q1

_____all memory systems are dumb, in that they respond to only two commands: read or write
Virtually
Logically
Physically
None of These

Q 3
To access an operand in memory, the CPU must first generate an address, which it then issues to the _____
MEMORY
REGISTER
DATA BUS
ALL OF ABOVE
Q 4
_____ or Branch instructions affect the order in which instructions are performed, or control the flow of the program
Control
DATA MOVMENT
Arithmetic
LOGICAL
Q5
Reverse assemble the following SRC machine language instructions:
[10]
68C2003A h
Simple decode each hexa letter into equivalent 4 bit number.
Q6
An instruction that specifies one operand in memory and one operand in a register would be known as a _____ address instruction.
2-1/2
1-1/2
0
2
Q7
The data movement instructions _____ data within the machine and to or from input/output devices
Store
LOAD
MOVE
NONE OF ABOVE.
Q8
==========>

MCQz (Set-3)

Question # 1 of 10 (Start time: 05:25:03 PM) Total Marks: 1
Which one of the following is a bi-stable device, capable of storing one bit of Information?
Select correct option:

Decoder
Flip-flop
Multiplexer
Diplexer

Question # 2 of 10 (Start time: 05:26:00 PM) Total Marks: 1
The instruction ----------will load the register R3 with the contents of the memory location M [PC+56]
Select correct option:
Add R3, 56
lar R3, 56
ldr R3, 56
str R3, 56

Question # 3 of 10 (Start time: 05:26:46 PM) Total Marks: 1
What is the working of Processor Status Word (PSW)?
Select correct option:
To hold the current status of the processor.
To hold the address of the current process
To hold the instruction that the computer is currently processing
To hold the address of the next instruction in memory that is to be executed
---

Question # 4 of 10 (Start time: 06:00:59 PM) Total Marks: 1
What does the instruction "ldr R3, 58" of SRC do?
Select correct option:
It will load the register R3 with the contents of the memory location M [PC+58] (P # 47)
It will load the register R3 with the relative address itself (PC+58).
It will store the register R3 contents to the memory location M [PC+58]
No operation

Question # 5 of 10 (Start time: 06:02:27 PM) Total Marks: 1
What functionality is performed by the instruction "lar R3, 36" of SRC?
Select correct option:
It will load the register R3 with the contents of the memory location M [PC+36]
It will load the register R3 with the relative address itself (PC+36). (P # 47)
It will store the register R3 contents to the memory location M [PC+36]
No operation

Question # 6 of 10 (Start time: 06:03:55 PM) Total Marks: 1
In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?
Select correct option:
Arithmetic/logic (not sure)

Load/store
Test/branch
None of the given

Question # 7 of 10 (Start time: 06:05:24 PM) Total Marks: 1
Type A of SRC has which of the following instructions? a) andi, instruction b) No operation or nop instruction c) lar instruction d) ldr instruction e) Stop operation or stop instruction
Select correct option:
(a)& (b)
(b)&(c) (not sure)
(a)&(e)
(b)&(e) confirmed.

Question # 8 of 10 (Start time: 06:06:36 PM) Total Marks: 1
Which of the instruction is used to load register from memory using a relative address?
Select correct option:
ld instruction
ldr instruction
lar instruction
str instruction

Question # 9 of 10 (Start time: 06:07:12 PM) Total Marks: 1
Which type of instructions help in changing the flow of the program as and when required?
Select correct option:
Arithmetic
Control
Data transfer
Floating point

Question # 10 of 10 (Start time: 06:08:32 PM) Total Marks: 1
In which one of the following addressing modes, the value to be stored in memory is obtained by directly retrieving it from another memory location?
Select correct option:
Direct Addressing Mode
Immediate addressing mode
Indirect Addressing Mode
Register (Direct) Addressing Mode (not sure)

Question # 1 of 10 (Start time: 06:20:21 PM) Total Marks: 1
Which one of the following circuit design levels is called the gate level?
Select correct option:
Logic Design Level

Circuit Level
Mask Level
None of the given

Question # 2 of 10 (Start time: 06:21:08 PM) Total Marks: 1
What is the working of Processor Status Word (PSW)?
Select correct option:
To hold the current status of the processor.
To hold the address of the current process
To hold the instruction that the computer is currently processing
To hold the address of the next instruction in memory that is to be executed
---

Question # 3 of 10 (Start time: 06:21:40 PM) Total Marks: 1
Which one of the following is the highest level of abstraction in digital design in which the computer architect views the system for the description of system components and their interconnections?
Select correct option:
Processor-Memory-Switch level (PMS level)
Instruction Set Level
Register Transfer Level
None of the given

Question # 5 of 10 (Start time: 06:23:26 PM) Total Marks: 1
Execution time of a program with respect to the processor is calculated as:
Select correct option:
Execution Time = IC x CPI x MIPS
Execution Time = IC x CPI x T
Execution Time = CPI x T x MFLOPS
Execution Time = IC x T

Question # 6 of 10 (Start time: 06:24:08 PM) Total Marks: 1
What does the word 'D' in the 'D-flip-Flop' stands for?
Select correct option:
Data
Digital
Dynamic
Double

Question # 8 of 10 (Start time: 06:26:57 PM) Total Marks: 1
Which field of the machine language instruction is the "type of operation" that is to be performed?
Select correct option:
Op-code (or the operation code)
CPU registers

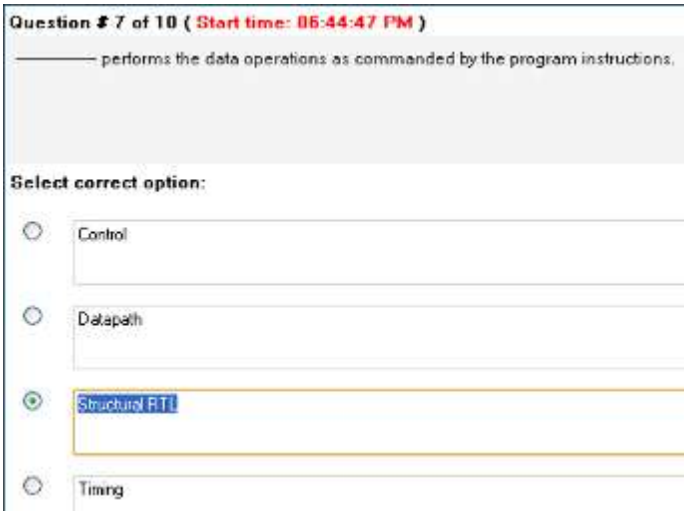
Memory cells
I/O locations

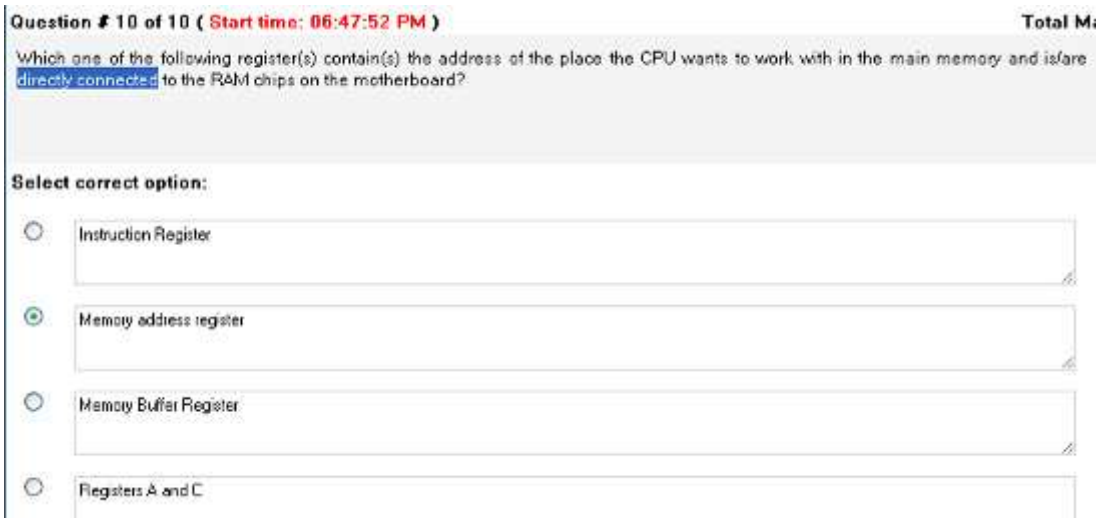
Question # 9 of 10 (Start time: 06:28:23 PM) Total Marks: 1
Which of the instruction is used to load register from memory using a relative address?
Select correct option:
ld instruction
ldr instruction
lar instruction
str instruction

Question # 10 of 10 (Start time: 06:28:59 PM) Total Marks: 1
The instruction ----------will load the register R3 with the contents of the memory location M [PC+56]
Select correct option:
Add R3, 56
lar R3, 56
ldr R3, 56
str R3, 56

==========>

MCQz (Set-5)




Question # 10 of 10 (Start time: 06:47:52 PM) Total M

Which one of the following register(s) contain(s) the address of the place the CPU wants to work with in the main memory and is/are directly connected to the RAM chips on the motherboard?

Select correct option:

- Instruction Register
- Memory address register
- Memory Buffer Register
- Registers A and C

==========>

MCQz (Set-6)

Question No: 1

Which one of the following is the memory organization of **SRC processor?**

- 28 * 8 bits
- 216 * 8 bits

2^{32} * 8 bits

- 264 * 8 bits

Question No: 2

Type A format of SRC uses ----------instructions

two

- three
- four
- five

Question No: 3

The instruction ----------will **load** the register R3 with the contents of the memory location M [PC+56]

- Add R3, 56
- lar R3, 56
- ldr R3, 56
- str R3, 56

Question No: 4

Which format of the instruction is called the accumulator?

- 3-address instructions
- 3-address instructions
- 2-address instructions

1-address instructions

- 0-address instructions

A 1-address instruction has a dedicated CPU register, called the accumulator,

Question No: 5

Which one of the following are the **code size** and the **Number of memory bytes** respectively for a 2-address instruction?

- 4 bytes, 7 bytes

7 bytes, 16 bytes

- 10 bytes, 19 bytes
- 13 bytes, 22 bytes

Instruction Format	Code size	Number of memory bytes
4-address instruction	13	22
3-address instruction	10	19
2-address instruction	7	16
1-address instruction	4	7
0-address instruction	1	10

Question No: 6

Which operator is used to name registers, or part of registers, in the Register Transfer Language?

:=

- &
- %
- © concatenatation.

Question No: 8

Circuitry that is used to move data is called ----------

Bus

- Port
- Disk
- Memory

Question No: 9

Which one of the following is **NOT** a technique used when the CPU wants to exchange data with a peripheral device?

- Direct Memory Access (DMA).
- Interrupt driven I/O
- Programmed I/O

Virtual Memory

Question No: 10

Every time you press a key, an interrupt is generated.

This is an example of

- Hardware interrupt
- Software interrupt

Exception

- All of the given

Question No: 11

The interrupts which are pre-programmed and the processor automatically finds the address of the ISR using interrupt vector table are

- Maskable
- Non-maskable
- Non-vectored

Vectored

Question No: 12

Which is the last instruction of the ISR that is to be executed when the ISR terminates?

IRET

- IRQ
- INT
- NMI

This means that the IRET instruction should be the last instruction of every ISR

Question No: 13

If NMI and INTR both interrupts occur simultaneously, then which one has the precedence over the other

NMI

- INTR
- IRET
- All of the given

NMI has priority over INTR if both occur simultaneously.

Question No: 14

Identify the following type of serial communication error condition:

The prior character that was received was not still read by the CPU and is over written by a new received character.

- Framing error
- Parity error

Overrun error Page 242

- Under-run error

Question No: 15

----------the device usually means reading its status register every so often until the device's status changes to indicate that it has completed the request.

- Executing
- Interrupting
- Masking
- Polling

Question No: 16

Which I/O technique will be used by a sound card that may need to access data stored in the computer's RAM?

Programmed I/O

- Interrupt driven I/O
- Direct memory access(DMA)
- Polling

Question No: 17

For increased and better performance we use _____ which are usually made of glass.

- Coaxial Cables
- Twisted Pair Cables

Fiber Optic Cables

- Shielded Twisted Pair Cables

Question No: 18

In _____ if we find some call party busy we can have provision of call waiting.

- Delay System
- Loss System
- Single Server Model
- None of the given

Question No: 19

In ____ technique memory is divided into segments of variable sizes depending upon the requirements.

- Paging

Segmentation

- Fragmentation
- None of the given

Question No: 20

For a request of data if the requested data is not present in the cache, it is called a _____

- Cache Miss
- Spatial Locality

Temporal Locality

- Cache Hit

Question No: 21

An entire _____ memory can be erased in one or a few seconds which is much faster than EPROM.

- PROM
- Cache
- EEPROM

Flash Memory

Question No: 22

_____chips have quartz windows and by applying ultraviolet light data can be erased from them.

- PROM
- Flash Memory
- EPROM
- EEPROM

Question No: 23

The _____signal coming from the CPU tells the memory that some interaction is required between the CPU and memory.

- REQUEST
- COMPLETE

None of the given

Question No: 24

_____ is a combination of arithmetic, logic and shifter unit along with some multiplexers and control unit.

- Barrel Rotator
- Control Unit
- Flip Flop

ALU

Question No: 25

1. In Multiple Interrupt Line, a number of interrupt lines are provided between the _____ module.

- CPU and the I/O
- CPU and Memory
- Memory and I/O
- None of the given

Question No: 26

The data movement instructions _____ data within the machine and to or from input/output devices.

- Store
- Load

Move

- None of given

Question No: 27

CRC has ---------- overhead as compared to Hamming code.

- Equal

Greater

- Lesser
- None of the given

Question No: 28

The _____ is w-bit wide and contains a data word, directly connected to the data bus which is b-bit wide memory address register (MAR) .

- Instruction Register(IR)
- memory address register (MAR)
- **memory Buffer Register(MBR)**
- Program counter (PC)

Question No: 29

In_____technique, a particular block of data from main memory can be placed in only one location into the cache memory .

- Set Associative Mapping

Direct Mapping page 350

- Associative Mapping
- Block Placement

Question No: 30

_____ indicate the availability of page in main memory.

- Access Control Bits
- Used Bits

- Presence Bits
- None of the given

==========>

MCQz (Set-7)

Question # 1 of 10 (Start time: 09:48:03 PM) Total Marks: 1
_____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.
Select correct option:
INC4
LPC
PCout
TRUE
LC

Question # 2 of 10 (Start time: 09:48:58 PM) Total Marks: 1
_____ enable the input to the PC for receiving a value that is currently on the internal processor bus.
Select correct option:
LPC
TRUE
INC4
LC
Cout

Question # 5 of 10 (Start time: 09:51:19 PM) Total Marks: 1
For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required; which may
be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate
memory location.
Select correct option:
Registers
Control signals
TRUE
Memory
None of the given

Question # 7 of 10 (Start time: 09:52:34 PM) Total Marks: 1
Which one of the following registers holds the address of the next instruction to be executed?
Select correct option:
Accumulator
Address Mask

Instruction Register
Program Counter
TRUE
Click here to Save Answer & Move to Next Question

==========>

MCQz (Set-8) (Not for Miterm)

Question No: 1
The _____ RTN describes the overall effect of instructions on the programmer visible
Registers.
1. **Abstract (doubtful)**
2. Concrete
3. Absolute
4. Basic

Question No: 2
The instruction set is of _____ importance in governing the structure and function of the pipeline.
Least (doubtful)
Primary
Secondary
No
Question No: 3
_____ is the most general and least useful performance metrics for RISC machines.
MIPS
Instruction Count
Number of registers
Clock Speed
Question No: 4
A _____ provides four functions: Select, DataIn, DataOut and Read/Write.
ALU
Bus
Register
Memory Cell
Question No: 5
We can classify or partition the SRC instructions by their overall _____ behavior.
Register transfer
Memory transfer
Execution
Logical

Question No: 6
The _____ RTN describes detailed register transfer steps in the data path that produce
the overall effect.
Abstract
Concrete
Absolute
Basic

Question No: 7
All members of the MC68000 family are _____ processors.
32-bit
16-bit
64-bit
8-bit
Question No: 8
_____Operations refers to a processor that can issue more than one instruction simultaneously.
Macro
Micro
Scalar
Superscalar
Question No: 9
Exceptions which are _____occur in response to events that are paced by the internal processor clock.
Asynchronous
Synchronous
Internal
External
External exceptions or interrupts are generally asynchronous (do not depend on the system clock) while internal exceptions are synchronous (paced by internal clock)
Question No: 10
In the hazard detection by hardware, resolved by pipeline stalls, if the instructions are in the adjoining stages, then the hazard must be detected in stage _____.
4 not confirm
2
3
1
Question No: 38
In floating point representations _____ is also called mantissa.
Sign
Base
Significant
Exponent

Question No: 39
Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)

Framing error
Parity error
Overrun error
Under-run error

Question No: 40
What should be the behavior of interrupts during critical sections?

Must remain Disable
Must remain Enable
Can be either enable or disable
Only important interrupts be enable.

Question No: 41
The _____signal coming from the CPU tells the memory that some interaction is required
between the CPU and memory.

R/W
COMPLETE
None of the given

REQUEST

Question No: 42
_____ is the simplest form for representing a signed number

Sign Magnitude Form
None of the given
Biased Representation
Diminished Radix Compliment Form

Question No: 43
Which of the instruction is used to load register from memory using a relative address?

ld instruction

ldr instruction
lar instruction
str instruction

Question No: 44
_____ is/are defined as the number of instructions processed per second

Throughput
Latency
Throughput and Latency
None of the given

Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A and source register B) from the following example. ADD R1, R2, R3
Select correct option:

Opcode= R1, DR=ADD, SA=R2, SB=R3

Opcode= ADD, DR=R1, SA=R2, SB=R3

Opcode= R2, DR=ADD, SA=R1, SB=R3

Opcode= ADD, DR=R3, SA=R2, SB=R1

Which type of instructions help in changing the flow of the program as and when required?

Select correct option:

Arithmetic

Control

Data transfer

Floating point

Almost every commercial computer has its own particular ---------- language

Select correct option:

3GL

English language

Higher level language

assembly language

Which one of the following is a binary cell capable of storing one bit of information?

Select correct option:

Decoder

Flip-flop

Multiplexer

Diplexer

Which statement(s)from the following is/are correct about Reduced Instruction Set Computer (RISC) architectures.

(i) The typical RISC machine instruction set is small, and is usually a subject of a CISC instruction set.

(ii) (ii) No arithmetic or logical instruction can refer to the memory directly.

(iii) (iii) A comparatively large number of user registers are available.

(iv) (iv) Instructions can be easily decoded through hard-wired control units.

Select correct option:

(i) and (iii) only

(i), (iii) and (iv)

(i), (ii) and (iii) only

(i),(ii),(iii) and (iv)

What is the instruction length of the FALCON-E processor?
Select correct option:

8 bits
16 bits
32 bits
64 bits

Which one of the following are the code size and the Number of memory bytes respectively for a 3-address instruction?
Select correct option:

0 bytes, 10 bytes
4 bytes, 7 bytes =1-address instruction
7 bytes, 16 bytes =2-address instruction
10 bytes, 19 bytes =3-address instruction

The CPU includes three types of instructions, which have different operands and will need different representations. Which one of the instructions requires two source registers?
Select correct option:

Jump and branch format instructions
Immediate format instructions
Register format instructions
All of the above

In which one of the following addressing modes, the operand does not specify an address but it is the actual data to be used.
Select correct option:

Direct
Indirect
Immediate
Relative

Question # 10 of 10 (Start time: 11:17:26 PM) Total Marks: 1
Which type of instructions load data from memory into registers, or store data from registers into memory and transfer data between different kinds of special-purpose registers?
Select correct option:
Arithmetic

Control
Data transfer
Floating point

Question # 3 of 10 (Start time: 07:17:26 PM) Total Marks: 1
What does the RTL expression [M(1234)] means?
Select correct option:
The contents of memory whose address is 1234.
The contents of data register 1234
The effective address of register 1234
The address of memory whose address is 1234.

Question # 5 of 10 (Start time: 07:20:00 PM) Total Marks: 1
Which type of instructions enables mathematical computations?
Select correct option:

Arithmetic
Control
Data transfer
Floating point

Question # 7 of 10 (Start time: 07:22:33 PM) Total Marks: 1
Which one of the following is the memory organization of EAGLE processor?
Select correct option:

2^8 * 8 bits
2^16 * 8 bits
2^32 * 8 bits
2^64 * 8 bits
Memory organization is 2^{16} x 8 bits. This means that there are 216 memory cells, each one byte long Page 112

==========>

MCQz (Set-9)

Question No: 1
The _____ RTN describes the overall effect of instructions on the programmer visible registers.
Abstract
Concrete
Absolute
Basic

Question No: 2
The instruction set is of _____ importance in governing the structure and function of the pipeline.
Least Not Confirm
Primary
Secondary
No

Question No: 3
_____ is the most general and least useful performance metrics for RISC machines.
MIPS
Instruction Count
Number of registers
Clock Speed

Question No: 4
A _____ provides four functions: Select, DataIn, DataOut and Read/Write.
ALU
Bus
Register
Memory Cell

Question No: 5
We can classify or partition the SRC instructions by their overall _____ behavior.
Register transfer
Memory transfer
Execution
Logical

Question No: 6
The _____ RTN describes detailed register transfer steps in the data path that produce the overall effect.
Abstract
Concrete
Absolute
Basic

Question No: 41
The _____signal coming from the CPU tells the memory that some interaction is required between the CPU and memory.
R/W
COMPLETE
None of the given
REQUEST

Question No: 42
_____ is the simplest form for representing a signed number
Sign Magnitude Form

None of the given
Biased Representation
Diminished Radix Compliment Form

Question No: 43
Which of the instruction is used to load register from memory using a relative address?
ld instruction
ldr instruction
lar instruction
str instruction

Question No: 44
_____ is/are defined as the number of instructions processed per second
Throughput
Latency
Throughput and Latency
None of the given
Latency is defined as the time required to process a single instruction, while throughput is defined as the number of instructions processed per second. Pipelining cannot lower the latency of a single instruction; however, it does increase the throughput.

==========>

MCQz (Set-10)

Question # 9 of 10 (Start time: 07:25:30 PM) Total Marks: 1
Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A and source register B) from the following example. ADD R1, R2, R3
Select correct option:

Opcode= R1, DR=ADD, SA=R2, SB=R3
Opcode= ADD, DR=R1, SA=R2, SB=R3 Page 97
Opcode= R2, DR=ADD, SA=R1, SB=R3
Opcode= ADD, DR=R3, SA=R2, SB=R1

Question # 1 of 10 (Start time: 07:31:22 PM) Total Marks: 1
Which instruction is used to store register to memory using relative address?
Select correct option:
ld instruction
ldr instruction
lar instruction
str instruction

Question # 2 of 10 (Start time: 07:32:11 PM) Total Marks: 1
Which one of the following languages presents a simple, human-oriented language to specify the operations, register communication and timing of the steps that take place within a CPU to carry out higher level (user programmable) instructions?

Select correct option:

Assembly Language
OOP(Object Oriented Language)
RTL (Register Transfer Language)
UML(Unified Modeling language)

Question # 3 of 10 (Start time: 07:33:40 PM) Total Marks: 1
Which one of the following instructions is used to load register from memory using a relative address?
Select correct option:

la
lar
ldr
str

Question # 4 of 10 (Start time: 07:34:15 PM) Total Marks: 1
Which field of the machine language instruction is the "type of operation" that is to be performed?
Select correct option:

Op-code (or the operation code)
CPU registers
Memory cells
I/O locations

Question # 5 of 10 (Start time: 07:35:43 PM) Total Marks: 1
What is the instruction length of the FALCON-A processor?
Select correct option:

8 bits
16 bits
32 bits
64 bits

Question # 6 of 10 (Start time: 07:37:17 PM) Total Marks: 1
Which one of the following are the code size and the Number of memory bytes respectively for a 3-address instruction?
Select correct option:

0 bytes, 10 bytes
4 bytes, 7 bytes
7 bytes, 16 bytes
10 bytes, 19 bytes

Question # 7 of 10 (Start time: 07:38:47 PM) Total Marks: 1
The data movement instructions _____ data within the machine and to or from input/output devices.
Select correct option:

Store
Load
Move
None of given

Question # 8 of 10 (Start time: 07:40:20 PM) Total Marks: 1
In----------address mode, the actual data is stored in the instruction.
Select correct option:

Direct
Indirect
Immediate
Relative

Question # 9 of 10 (Start time: 07:41:44 PM) Total Marks: 1
Which one of the following are the code size and the Number of memory bytes respectively for a 2-address instruction?
Select correct option:

4 bytes, 7 bytes
7 bytes, 16 bytes
10 bytes, 19 bytes
13 bytes, 22 bytes

Question # 10 of 10 (Start time: 07:42:43 PM) Total Marks: 1
Which type of instructions enables mathematical computations?
Select correct option:

Arithmetic
Control
Data transfer
Floating point

Question # 3 of 10
An "assembler" that runs on one processor and translates an assembly language program written for another processor into the machine language of the other processor is called a ----------
Compiler
Cross assembler
Debugger
linker

Which one of the following is an address (binary bit pattern) issued by CPU?
Memory
Effective
Base
Next instruction

Question # 2 of 10 (Start time: 09:40:12 PM) Total Marks: 1
What functionality is performed by the instruction "str R8, 34" of SRC?
It will load the register R8 with the contents of the memory location M [PC+34]
It will load the register R8 with the relative address itself (PC+34).
It will store the register R8 contents to the memory location M [PC+34]
No operation

Question # 3 of 10 (Start time: 09:41:18 PM) Total Marks: 1
For the _____ type instructions, we require a register to hold the data that is to be loaded from the memory, or stored back to the memory .
1. Jump
2. Control
3. Load/store
4. None of the given.

Question # 4 of 10
The instruction ----------will load the register R3 with the contents of the memory location M [PC+56]
Add R3, 56
lar R3, 56
ldr R3, 56
str R3, 56

Question # 9 of 10 (Start time: 09:47:52 PM) Total Marks: 1
Which of the following can be defined as an address of the operand in a computer type instruction or the target address in a branch type instruction?
Base address
Binary addres
Effective address

All of the given

Question # 10 of 10 (Start time: 09:49:19 PM) Total Marks: 1
Which one of the following is a bi-stable device capable of storing one bit of Information?
Decoder
flip-flop
Multiplexer
Diplexer

==========>

MCQz (Set-11)

Question No: 1 (M a r k s: 1)
What is the instruction length of the SRC processor?
► 8 bits
► 16 bits
► 32 bits
► 64 bits

Question No: 2 (M a r k s: 1)
Which one of the following is the memory organization of **FALCON-E processor?**
► 2^8 * 8 bits
► 2^{16} * 8 bits
► 2^{32} * 8 bits
► 2^{64} * 8 bits

Question No: 3 (M a r k s: 1)
"If P = 1, then load the contents of register R1 into register R2".
This statement can be written in RTL as
► R1 ¬ R2
► P: R1 ¬ R2
► P: R2 ¬ R1
► P: R2 ¬ R1, P: R1 ¬ R2

Question No: 4 (M a r k s: 1)
The instruction ----------will **load** the register R3 with the contents of the memory location M [PC+56]
► Add R3, 56
► lar R3, 56
► ldr R3, 56
► str R3, 56

Question No: 5 (M a r k s: 1)
----------are faster than cache memory
► Accumulator register
► CPU registers Page 31
► I/O devices
► ROM

Question No: 6 (M a r k s: 1)

P: R3 ¬ R5
MAR ¬ IR
These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?
► Arrow ¬
► Colon :
► **Comma ,**
► Parentheses ()
Question No: 7 (M a r k s: 1)
Prefetching can be considered a primitive form of----------
► **Pipelining**
► Multi-processing
► Self-execution
► Exception
==========>

MCQz (Set-12)

Question # 1 of 10 (Start time: 10:48:22 PM) Total Marks: 1
Keyboard Interrupt (INT 9) is an example of ----- interrupt.
Select correct option:
Hardware TRUE
Software
Click here to Save Answer & Move to Next Question

Question # 2 of 10 (Start time: 10:49:48 PM) Total Marks: 1
Shifting of the radix point towards left or right is called _____
Select correct option:
Shifting
Logical Shift
Right Shift
Scaling TRUE
Click here to Save Answer & Move to Next Question

Question # 3 of 10 (Start time: 10:50:27 PM) Total Marks: 1
For _____ of an error we just need to know that there exists an error.
Select correct option:
Detection TRUE
Correction
Both Correction and Detection
None of the given

Question # 4 of 10 (Start time: 10:51:00 PM) Total Marks: 1
A user program has to delete a file. The user program will be executing in the user mode. When it makes the specific system call to delete the file, an interrupt will be generated, this will cause the processor to halt its current activity and switch to supervisor mode.

Once in supervisor mode, the operating system will delete the file and then control will return to the user program. This is an example of
Select correct option:
Hardware interrupt
Software interrupt TRUE
Exception
All of the given

Question # 5 of 10 (Start time: 10:52:14 PM) Total Marks: 1
By which file extension does the FALCON-A Assembler loads a FALCON-A assembly file?
Select correct option:
.asmfa TRUE
.org
.exe
.src

Question # 6 of 10 (Start time: 10:53:17 PM) Total Marks: 1
All ----------interrupts have priority over all ---------interrupts
Select correct option:
internal, external TRUE
external,internal

Question # 7 of 10 (Start time: 10:53:41 PM) Total Marks: 1
Given an m-digit base b number x, the _____ of x is xc = (bm– x) mod bm
Select correct option:
Radix Compliment TRUE
Diminished Radix Compliment
Signed Magnitude Form
Biased Representation

Question # 8 of 10 (Start time: 10:54:45 PM) Total Marks: 1
The ------- can also be used anywhere in the source file to force code at a particular address in the memory.
Select correct option:
.end directive
.start directive
.label directive
.org directive TRUE

Question # 9 of 10 (Start time: 10:55:11 PM) Total Marks: 1
Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?
Select correct option:
Daisy-Chaining Priority
Asynchronous Priority
Parallel Priority TRUE
Semi-synchronous Priority

Question # 10 of 10 (Start time: 10:56:26 PM) Total Marks: 1

An ---------- is the memory address of an interrupt handler.
Select correct option:
Interrupt vector TRUE
Interrupt service routine
Exception
Mask

==========>

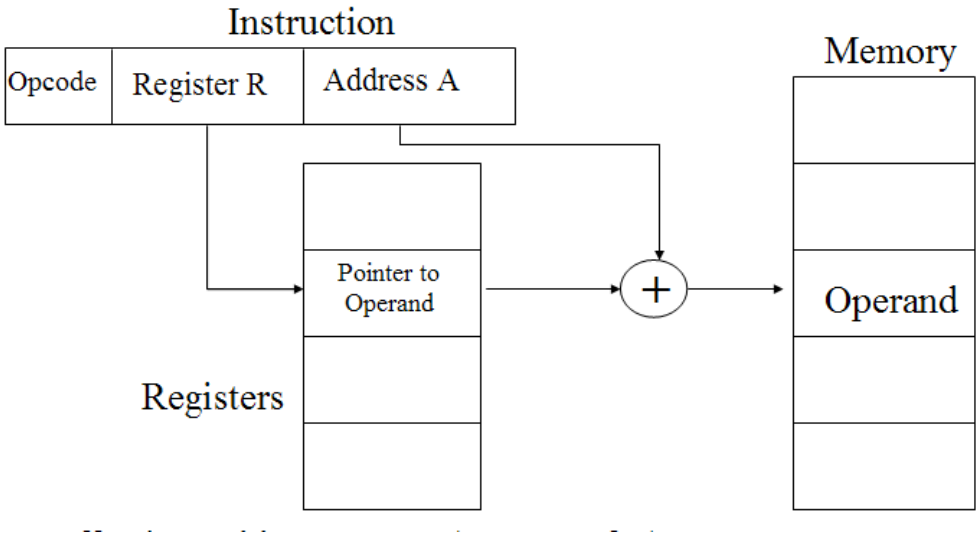
MCQz (Set-13)

Question No: 1

The CPU includes three types of instructions, which have different operands and will need different representations.
Which one of the instructions requires two source registers?

- ► Jump and branch format instructions
- ► **Immediate format instructions**
- ► **Register format instructions**
- ► All of the above

Question No: 2



In this figure, the constant value specified by the immediate field is added to the register value, and the resultant is the index of memory location that is referred i.e. Effective Address = A + (content of R) .
Identify the addressing mode.

- ► **Displacement**
- ► Immediate
- ► Indexed
- ► Relative

Question No: 3

In which one of the following addressing modes, the operand does not specify an address but it is the actual data to be used.

- ► Direct

- Indirect
- **Immediate**
- Relative

Question No: 4

Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A and source register B) from the following example.

ADD R1, R2, R3

- Opcode= R1, DR=ADD, SA=R2, SB=R3
- Opcode= ADD, DR=R1, SA=R2, SB=R3
- Opcode= R2, DR=ADD, SA=R1, SB=R3
- **Opcode= ADD, DR=R3, SA=R2, SB=R1**

Question No: 5

When the address of the subroutine is already known to the Microprocessor then it is called as --------- interrupt.

- Maskable
- Non-maskable
- **Non-vectored**
- Vectored

Question No: 6

The interrupts which are pre-programmed and the processor automatically finds the address of the ISR using interrupt vector table are

- Maskable
- Non-maskable
- **Non-vectored**
- Vectored

Question No: 7

Which is the last instruction of the ISR that is to be executed when the ISR terminates?

- **IRET**
- IRQ
- INT
- NMI

Question No: 8

When is the **"Divide error interrupt"** generated?

- When an attempt is made to divide by decimal number
- When an attempt is made to multiply by zero
- **When an attempt is made to divide by zero**
- When negative number is stored in a register

Question No: 9

Identify the following type of serial communication error condition:

"The prior character that was received was not still read by the CPU and is over written by a new received character."

- Framing error
- Parity error

► **Overrun error**

► Under-run error

Question No: 10

Which one of the following is a term used to describe a **storage systems**' resilience to disk failure through the use of multiple disks and by the use of data distribution and correction techniques?

► Interrupt handling

► Programmed I/O

► Polling

► **RAID**

Question No: 11

_____ is the time for first bit of the message to arrive at the receiver including delays.

► Transmission Time

► Latency

► Transport Latency

► **Time of Flight**

Question No: 12

For a request of data if the requested data is not present in the cache, it is called a _____

► **Cache Miss**

► Spatial Locality

► Temporal Locality

► Cache Hit

Question No: 13

An entire _____ memory can be erased in one or a few seconds which is much faster than EPROM.

► PROM

► Cache

► EEPROM

► **Flash Memory**

Question No: 14

A combination of parallel and sequential hardware used to build a multiplier is known as _____

► Parallel Array Multiplier

► Booth Recording

► **Series Parallel Multiplier**

► None of the given

Question No: 15

The _____ of an m digit number x is $x^{c'}=b^m-1-x$

► Radix Compliment

► **Diminished Radix Compliment**

► Signed Magnitude Form

► Biased Representation

Question No: 16

Along with information bits we add up another bit which is called the _____ bit.

- ▶ CRC
- ▶ Hamming
- ▶ Error Detection
- ▶ **Parity**

Question No: 17

Falcon-A Simulator loads a FALCON-A binary file with a _____ extension and presents its contents into different areas of the simulator.

- ▶ .bin
- ▶ **.binfa**
- ▶ .fa
- ▶ None of the given

Question No: 18

In machines where instructions can be executed in parallel or out of order, two additional hazards can occur: WAW and ----------

- ▶ None fo the given
- ▶ WAR
- ▶ **RAW**
- ▶ RAR

Question No: 19

---------- is the memory address of an interrupt handler.

- ▶ Interrupt vector
- ▶ Interrupt service routine
- ▶ Exception
- ▶ Mask

Question No: 20

Why DMA is faster than Programmer I/O technique ?

- ▶ DMA transfers data directly using CPU.
- ▶ **DMA transfers data directly without using CPU**
- ▶ DMA uses buffers with CPU
- ▶ DMA uses interrupted driven I/O

Question No: 21

For _____ of an error we just need to know that there exists an error.

- ▶ None of the given
- ▶ Correction
- ▶ Detection
- ▶ **Both Correction and Detection**

Question No: 22

In _____ recording ,bits are encoded in pairs so there are only ' n/2' additions instead of 'n'.

- ▶ Booth Recording
- ▶ **Bit Pair Recording**
- ▶ Integer division
- ▶ None of the given

Question No: 23

_____ are computed by the ALU and stored in processor status register.

► **Condition codes**
- ► Conditional Branches
- ► Fraction Division
- ► None of the given

Question No: 24

In floating point representations _____ is also called mantissa.
- ► Sign
- ► Base

► **Significand**
- ► Exponent

Question No: 25

Identify the type of serial communication error condition in which 0 is received instead of a stop bit (which is always a 1)?

► **Framing error**
- ► Parity error
- ► Overrun error
- ► Under-run error

Question No: 26

What should be the behavior of interrupts during critical sections?

► **Must remain Disable**
- ► Must remain Enable
- ► Can be either enable or disable
- ► Only important interrupts be enable.

Question No: 27

The _____signal coming from the CPU tells the memory that some interaction is required between the CPU and memory.
- ► R/W
- ► COMPLETE
- ► None of the given

► **REQUEST**

Question No: 28

_____ is the simplest form for representing a signed number

► **Sign Magnitude Form**
- ► None of the given
- ► Biased Representation
- ► Diminished Radix Compliment Form

Question No: 29

Which of the instruction is used to load register from memory using a relative address?
- ► ld instruction

► **ldr instruction**
- ► lar instruction
- ► str instruction

Question No: 30

_____ is/are defined as the number of instructions processed per second

- ► Throughput
- ► Latency Time to process 1 request.
- ► **Throughput and Latency**
- ► None of the given

==========>

MCQz (Set-14)

Question # 2 of 10 (Start time: 09:36:56 PM) Total Marks: 1

----------is the ability of application software to operate on models of equipment newer than the model for which it was originally developed.

Select correct option:

Backward compatibility

Data migration

Reverse engineering

Upward compatibility

Question # 4 of 10 (Start time: 09:38:07 PM) Total Marks: 1

Which one of the following register(s) that is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other

value?

Select correct option:

Instruction Register

Memory address register

Memory Buf fer Register

Registers A and C

Question # 5 of 10 (Start time: 09:38:39 PM) Total Marks: 1

For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.

Select correct option:

Registers

Control signals

Memory

None of the given

Question # 6 of 10 (Start time: 09:39:07 PM) Total Marks: 1

Which one of the following register(s) contain(s) the address of the place the CPU wants to work with in the main memory and is/are directly connected to the RAM chips on the motherboard?

Select correct option:

Instruction Register

Memory address register

Memory Buffer Register

Registers A and C

Question # 7 of 10 (Start time: 09:40:06 PM) Total Marks: 1
_____ enable the input to the PC for receiving a value that is currently on the internal processor bus.
Select correct option:
LPC
INC4
LC
Cout

Question # 8 of 10 (Start time: 09:40:37 PM) Total Marks: 1
Motorola MC68000 is an example of ---------microprocessor.
Select correct option:
CISC
RISC
SRC
FALCON

Question # 9 of 10 (Start time: 09:41:09 PM) Total Marks: 1
Which one of the following registers holds the address of the next instruction to be executed?
Select correct option:
Accumulator
Address Mask
Instruction Register
Program Counter

Question # 10 of 10 (Start time: 09:42:24 PM) Total Marks: 1
---------- performs the data operations as commanded by the program instructions.
Select correct option:
Control
Datapath
Structural RTL
Timing
==========>

MCQz (Set-15)

Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?
Select correct option:
Daisy-Chaining Priority
Asynchronous Priority
Parallel Priority
Semi-synchronous Priority

Question # 2 of 10 (Start time: 12:14:26 PM) Total Marks: 1
Connection to a CPU that provides a data path between the CPU and external devices, such as a keyboard, display, or reader is called----------

Select correct option:
Buffer
I/O port
Memory mapping
Processor

Question # 3 of 10 (Start time: 12:15:52 PM) Total Marks: 1
Raid Level ____ is not a true member of the RAID family.
Select correct option:
0
2
3
4

Question # 4 of 10 (Start time: 12:17:19 PM) Total Marks: 1
All ----------interrupts have priority over all ---------interrupts
Select correct option:
internal, external
external,internal

Question # 5 of 10 (Start time: 12:18:49 PM) Total Marks: 1
Identify the following type of serial communication error condition in which no character is available at the beginning of an
interval.
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

Question # 6 of 10 (Start time: 12:21:24 PM) Total Marks: 1
---------- is the time needed by the CPU to recognize (not service) an interrupt request.
Select correct option:
Interrupt Latency
Interrupt Handling
Interrupt Precedence
Priority Interrupt

Question # 7 of 10 (Start time: 12:22:30 PM) Total Marks: 1
If NMI and INTR both interrupts occur simultaneously, then which one has the precedence over the other.
Select correct option:
NMI
INTR
INTR
All of the given

Question # 8 of 10 (Start time: 12:23:20 PM) Total Marks: 1
What directive do we use as the last line in the source file to indicate the “end”?

Select correct option:
.end directive
.start directive
.label directive
.org directive

Question # 9 of 10 (Start time: 12:24:08 PM) Total Marks: 1
Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)?
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

Question # 10 of 10 (Start time: 12:24:41 PM) Total Marks: 1
The conversion of numbers from a representation in one base to another is known as_____
Select correct option:
Radix Conversion
Number Representation
Decimal representation
Hexadecimal Representation
==========>

MCQz (Set-16)

Question # 3 of 10 (Start time: 05:53:26 PM) Total Marks: 1
An "assembler" that runs on one processor and translates an assembly language program written for another processor into the machine language of the other processor is called a ----------
Select correct option:
compiler
cross assembler
TRUE
debugger
linker

Question # 4 of 10 (Start time: 05:54:53 PM) Total Marks: 1
Almost every commercial computer has its own particular ---------- language
Select correct option:
3GL
English language
Higher level language
assembly language
TRUE

Question # 5 of 10 (Start time: 05:56:04 PM) Total Marks: 1

Which one of the following is a binary cell capable of storing one bit of information?
Select correct option:
Decoder
Flip-flop
TRUE
Multiplexer
Diplexer
Which one of the following is a binary cell capable of storing one bit of information?

Question # 7 of 10 (Start time: 05:58:39 PM) Total Marks: 1
Which one of the following is an address (binary bit pattern) issued by CPU?
Select correct option:
Memory
Effective
TRUE
Base
Next instruction

Question # 8 of 10 (Start time: 05:59:55 PM) Total Marks: 1
For the _____ type instructions, we require a register to hold the data that is to be loaded from the memory, or stored
back to the memory
Select correct option:
Jump
Control
load/store
TRUE
None of the given

Question # 9 of 10 (Start time: 06:00:50 PM) Total Marks: 1
The CPU includes three types of instructions, which have different operands and will need different representations. Which one
of the instructions requires two source registers?
Select correct option:
Jump and branch format instructions
Immediate format instructions
Register format instructions
TRUE
All of the above

Question # 10 of 10 (Start time: 06:02:01 PM) Total Marks: 1
The instruction ----------will load the register R3 with the contents of the memory location M [PC+56]
Select correct option:
Add R3, 56
lar R3, 56
ldr R3, 56
TRUE
str R3, 56

Click here to Save Answer & Move to Next Question
ldr R3, 56

==========>

MCQz (Set-17)

Question No: 1

What is the instruction length of the SRC processor?

- ► 8 bits
- ► *16 bits*
- ► **32 bits**
- ► *64 bits*

Question No: 2

Which one of the following is the memory organization of ***FALCON-E processor?***

- ► 2^8 * 8 bits
- ► 2^{16} * 8 bits
- ► **2^{32} * 8 bits**
- ► 2^{64} * 8 bits

Question No: 3

"If P = 1, then load the contents of register R1 into register R2".

This statement can be written in RTL as:

- ► *R1 ¬ R2*
- ► *P: R1 ¬ R2*
- ► **P: R2 ¬ R1**
- ► *P: R2 ¬ R1, P: R1 ¬ R2*

Question No: 4

The instruction ----------will ***load*** *the register R3 with the contents of the memory location M [PC+56]*

□□□□□□□►□*Add R3, 56*
□□□□□□□►□*lar R3, 56*
□□□□□□□►□**ldr R3, 56**
□□□□□□□►□*str R3, 56*

Question No: 5

----------are faster than cache memory

□□□□□□□►□*Accumulator register*
□□□□□□□►□**CPU registers**
□□□□□□□►□*I/O devices*
□□□□□□□►□*ROM*

Question No: 6

P: R3 ¬ R5
MAR ¬ IR

These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?

- ► *Arrow ¬*
- ► *Colon :*
- ► **Comma ,**

► *Parentheses ()*

Question No: 7

Prefetching can be considered a primitive form of----------

□□□□□□□►□**Pipelining**

□□□□□□□►□*Multi-processing*

□□□□□□□►□*Self-execution*

□□□□□□□►□*Exception*

Question No: 8

The processor must have a way of saving information about its state or context so that it can be restored upon return from the ----------

□□□□□□□►□**Exception**

□□□□□□□►□*Function*

□□□□□□□►□*Stack*

□□□□□□□►□*Thread*

Question No: 9

Which one of the following circuit design levels is called the gate level?

□□□□□□□►□**Logic Design Level**

□□□□□□□►□*Circuit Level*

□□□□□□□►□*Mask Level*

□□□□□□□►□*None of the given*

Question No: 10

_____ enable the input to the PC for receiving a value that is currently on the internal processor bus.

► **LPC**

► *INC4*

► *LC*

► *Cout*

Question No: 11

_____ operation is required to change the processor's state to a known, defined value.

► *Change*

► **Reset**

► *Update*

► *None of the given*

Question No: 12

There are _____ types of reset operations in SRC

► **Two**

► *Three*

► *Four*

► *Five*

Question No: 13

_____ controller controls the sequence of the flow of microinstructions.

► *Multiplexer*
► **Microprogram**
► *ALU*
► *None of the given*

Question No: 14
FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is _____ wide.

► *8-bits*
► *24-bits*
► **32-bits**
► *64-bits*

Question No: 15
Which of the following statement(s) is/are correct about Reduced Instruction Set Computer (RISC) architectures.
(i) The typical RISC machine instruction set is small, and is usually a subject of a CISC instruction set.
(ii) No arithmetic or logical instruction can refer to the memory directly.
(iii) A comparatively large number of user registers are available.
(iv) Instructions can be easily decoded through hard-wired control units.

► *(i) and (iii) only*
► *(i), (iii) and (iv)*
► *(i), (ii) and (iii) only*
► **(i),(ii),(iii) and (iv)**

Question No: 16
Which one of the following register holds the instruction that is being executed?
► *Accumulator*
► *Address Mask*
► **Instruction Register**
► *Program Counter*

==========>

MCQz (Set-19)

What is the instruction length of the SRC processor?

8 bits
16 bits
32 bits
64 bits

Which one of the following is the memory organization of FALCON-E processor?

28 * 8 bits
216 * 8 bits
2^{32} * 8 bits
264 * 8 bits

_____ operation is required to change the processor's state to a known, defined value.

Change
Reset Page 196
Update (I think)
None of the given

There are _____ types of reset operations in SRC
Two
Three
Four
Five
_____ controller controls the sequence of the flow of microinstructions.

Multiplexer
Microprogram
ALU
None of the given
==========>

MCQz (Set-20)

Question # 3 of 10 (Start time: 07:17:26 PM) Total Marks: 1
What does the RTL expression [M(1234)] means?
Select correct option:
The contents of memory whose address is 1234.
The contents of data register 1234
The effective address of register 1234
The address of memory whose address is 1234.

Question # 4 of 10 (Start time: 07:19:00 PM) Total Marks: 1
Which type of instructions load data from memory into registers, or store data from registers into memory and transfer data between different kinds of special-purpose registers?
Select correct option:

Arithmetic
Control
Data transfer
Floating point

Question # 5 of 10 (Start time: 07:20:00 PM) Total Marks: 1
Which type of instructions enables mathematical computations?
Select correct option:

Arithmetic
Control
Data transfer

Floating point

Question # 6 of 10 (Start time: 07:21:00 PM) Total Marks: 1
What is the instruction length of the FALCON-E and SRC processor?
Select correct option:

8 bits
16 bits
32 bits
64 bits

Question # 7 of 10 (Start time: 07:22:33 PM) Total Marks: 1
Which one of the following is the memory organization of EAGLE processor?
Select correct option:

2^8 * 8 bits
2^16 * 8 bits
2^32 * 8 bits
2^64 * 8 bits

Question # 8 of 10 (Start time: 07:23:56 PM) Total Marks: 1
Type A of SRC has which of the following instructions? a) andi, instruction b) No operation or nop instruction c) lar instruction d) ldr instruction e) Stop operation or stop instruction
Select correct option:

(a)& (b)
(b)&(c)
(a)&(e)
(b)&(e)

Question # 9 of 10 (Start time: 07:25:30 PM) Total Marks: 1
Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A and source register B) from the following example. ADD R1, R2, R3
Select correct option:

Opcode= R1, DR=ADD, SA=R2, SB=R3
Opcode= ADD, DR=R1, SA=R2, SB=R3
Opcode= R2, DR=ADD, SA=R1, SB=R3
Opcode= ADD, DR=R3, SA=R2, SB=R1

Question # 1 of 10 (Start time: 07:31:22 PM) Total Marks: 1
Which instruction is used to store register to memory using relative address?
Select correct option:

ld instruction
ldr instruction
lar instruction

str instruction

Question # 2 of 10 (Start time: 07:32:11 PM) Total Marks: 1
Which one of the following languages presents a simple, human-oriented language to specify the operations, register communication and timing of the steps that take place within a CPU to carry out higher level (user programmable) instructions?
Select correct option:

Assembly Language
OOP(Object Oriented Language)
RTL (Register Transfer Language)
UML(Unified Modeling language)

Question # 5 of 10 (Start time: 07:35:43 PM) Total Marks: 1
What is the instruction length of the FALCON-A processor?
Select correct option:

8 bits
16 bits
32 bits
64 bits

Question # 6 of 10 (Start time: 07:37:17 PM) Total Marks: 1
Which one of the following are the code size and the Number of memory bytes respectively for a 3-address instruction?
Select correct option:

0 bytes, 10 bytes
4 bytes, 7 bytes
7 bytes, 16 bytes
10 bytes, 19 bytes

Question # 7 of 10 (Start time: 07:38:47 PM) Total Marks: 1
The data movement instructions _____ data within the machine and to or from input/output devices.
Select correct option:

Store
Load
Move
None of given

Question # 8 of 10 (Start time: 07:40:20 PM) Total Marks: 1
In----------address mode, the actual data is stored in the instruction.
Select correct option:

Direct

Indirect
Immediate
Relative

Question # 9 of 10 (Start time: 07:41:44 PM) Total Marks: 1
Which one of the following are the code size and the Number of memory bytes respectively for a 2-address instruction?
Select correct option:

4 bytes, 7 bytes
7 bytes, 16 bytes
10 bytes, 19 bytes
13 bytes, 22 bytes

==========>

MCQz (Set-21)

Question # 1 of 10 (Start time: 11:09:40 PM) Total Marks: 1
In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?
Select correct option:
Asynchronous Priority
Daisy-Chaining Priority
Parallel Priority
Semi-synchronous Priority

Question # 2 of 10 (Start time: 11:11:05 PM) Total Marks: 1
Identify the type of serial communication error condition in which a 0 is received instead of a stop bit (which is always a 1)?
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

Question # 3 of 10 (Start time: 11:12:24 PM) Total Marks: 1
An entire _____ memory can be erased in one or a few seconds which is much faster than EPROM.
Select correct option:
PROM
Cache
EEPROM
Flash Memory

Question # 4 of 10 (Start time: 11:13:12 PM) Total Marks: 1
Every time you press a key, an interrupt is generated. This is an example of
Select correct option:
Hardware interrupt

Software interrupt
Exception
All of the given

Question # 5 of 10 (Start time: 11:14:16 PM) Total Marks: 1
The ------- can also be used anywhere in the source file to force code at a particular address in the memory.
Select correct option:
.end directive
.start directive
.label directive
.org directive

Question # 6 of 10 (Start time: 11:15:11 PM) Total Marks: 1
In _____ recording ,bits are encoded in pairs so there are only ' n/2' additions instead of 'n'.
Select correct option:
Booth Recording
Bit Pair Recording
Integer division
None of the given

Question # 7 of 10 (Start time: 11:16:04 PM) Total Marks: 1
Which one the following interrupts is initiated with an INT instruction?
Select correct option:
Hardware
Software
Both hardware and Software
None of the given

Question # 8 of 10 (Start time: 11:17:11 PM) Total Marks: 1
When the address of the subroutine is already known to the Microprocessor then it is called as --------- interrupt.
Select correct option:
Maskable
Non-maskable
Non-vectored
Vectored

Question # 9 of 10 (Start time: 11:18:36 PM) Total Marks: 1
An ----------is a program that takes basic computer instructions and converts them into a pattern of bits that the computer's processor can use to perform its basic operations.
Select correct option:
Assembler
Debugger
Editor
Console

Question # 10 of 10 (Start time: 11:19:41 PM) Total Marks: 1

Taking control of the system bus for a few bus cycles is known as _____.
Select correct option:
Bus Stealing
Cycle Stealing
Cycle Transfering
None of given

Final Short Questions Paper

Set-01

CS501 - Advance Computer Architecture
Final paper 8/11/10

Q1) **suppose an I/O system with a single disk gets (on average) 200 I/O request/second. Assume that average time for a disk to service an I/O request is 4ms. What is the utilization time? 3Marks**

Answer:
Time for an I/O Request =4ms
=0.005 sec
Utilization Time of System =200x0.005
=1 sec.

Q2) **Give an example when DMA can be brought into use? 3Marks**

Answer: **Direct Memory Access (DMA)**
Direct memory access is a technique, where by the CPU passes its control to the memory subsystem or one of its peripherals, so that a contiguous block of data could be transferred from peripheral device to memory subsystem or from memory subsystem to peripheral device or from one peripheral device to another peripheral device.
Example of DMA
If we write instruction load as follows:
load [2], [9]
This instruction is illegal and not available in the SRC processor. The symbols [2] and [9] represent memory locations. If we want to have this transfer to be done then two steps would be required. The instruction would be:
load r1, [9]
store r1, [2]

Q3) **convert the hexadecimal number B316 to base 10 5Marks**

Answer:

Conversion of Base 16 into Base 10

According to the Radix conversion algorithm, convert the hexadecimal number $D4_{16}$ to base 10 (Write down all the steps which are involved in conversion).

Solution:
According to Radix Conversion Algorithm,
X=0
X=x+ D (=13) =13
X=16*13+4=212
Hence $D4_{16} = 212_{10}$

Conversion of Base 10 into Base 16

According to the Radix conversion algorithm, convert 492_{10} to base 16 (Write down all the steps which are involved in conversion).

Solution:
According to Radix Conversion Algorithm,
492/16=30 (remainder=12) , x0=C
30/16=1 (remainder=14) ,x1=E , x3=1
Thus $492_{10} = 1EC_{16}$

Q4) Does DMA affects the relationship b/w the memory system and CPU system. Explain with example.5Marks

Answer: Yes
DMA and memory system
DMA disturbs the relationship between the memory system and CPU.
Direct memory access and the memory system
Without DMA, all memory accesses are handled by the CPU, using address translation and cache mechanism. When DMA is implemented into an I/O system memory accesses can be made without intervening the CPU for address translation and cache access. The problems created by the DMA in virtual memory and cache systems can be solved using hardware and software techniques.

DMA Approach
The DMA approach is to turn off i.e. through tri-state buffers and therefore, electrically disconnect from the system bus, the CPU and let a peripheral device or a memory subsystem or any other module or another block of the same module communicate directly with the memory or with another peripheral device. This would have the advantage of having higher transfer rates which could approach that of limited by the memory itself.

Direct Memory Access (DMA):
Introduction
Direct Memory Access is a technique which allows a peripheral to read from and/or write to memory without intervention by the CPU. It is a simple form of bus mastering where the I/O device is set up by the CPU to transfer one or more contiguous blocks of memory. After the transfer is complete, the I/O device gives control back to the CPU.
The following DMA transfer combinations are possible:
• Memory to memory
• Memory to peripheral
• Peripheral to memory
• Peripheral to peripheral
The DMA approach is to "turn off" (i.e., tri-state and electrically disconnect from the

system buses) the CPU and let a peripheral device (or memory - another module or another block of the same module) communicate directly with the memory (or another peripheral).
ADVANTAGE: Higher transfer rates (approaching that of the memory) can be achieved.
DISADVANTAGE: A DMA Controller, or a DMAC, is needed, making the system complex and expensive.
Generally, DMA requests have priority over all other bus activities, including interrupts. No interrupts may be recognized during a DMA cycle.

Reason for DMA:

The instruction **load [2], [9]** is illegal. The symbols [2] and [9] represent memory locations. This transfer has to be done in two steps:

- **load r1,[9]**
- **store r1,bx**

Thus, it is not possible to transfer from one memory location to another without involving the CPU. The same applies to transfer between memory and peripherals connected to I/O ports. e.g., we cannot have **out [6], datap.** It has to be done in two steps:

- **load r1,[6]**
- **out r1, datap**

Similar comments apply to the **in** instruction.

Thus, the real cause of the limited transfer rate is the CPU itself. It acts as an unnecessary "middleman". The above discussion also implies that, in general, every data word travels over the system bus twice.

Data Transfer using DMA:

Data transfer using DMA takes place in three steps.

1st Step:

in this step when the processor has to transfer data it issues a command to the DMA controller with the following information:

- Operation to be performed i.e., read or write operation.
- Address of I/O device.
- Address of memory block.
- Size of data to be transferred.

After this, the processor becomes free and it may be able to perform other tasks.

2nd Step:

In this step the entire block of data is transferred directly to or from memory by the DMA controller.

3rd Step:

In this, at the end of the transfer, the DMA controller informs the processor by sending an interrupt signal.

Q5) **consider a 128kb direct mapping with a line length of 32 bytes**
_ Determine the number of bits in the address that refers to the bytes within the cache
_ Determine the number of bits in the address required to select the cache line.
5Marks

Answer:

Q6) **consider the following floating point's numbers 3 marks**
-0.5×10^{-3} Find out the sign, significant and exponent

Answer:
Floating Point Representations
Example

-0.5×10^{-3}

Sign = -1
Significand= 0.5
Exponent= -3
Base = 10= fixed for given type of representation

Significand is also called mantissa.

In computers, floating-point representation uses binary numbers to encode significant, exponent and their sign in a single word.
The diagram on Page 293 of the text shows an m-bit floating point number where s represents the sign of the floating point number. If s = 1 then the floating-point number will be a positive number; if s= 0 then it will be a negative number. The e field shows the value of exponent. To represent the exponent, a biased representation is used. So we represent e^ instead of e to show biased representation. In this technique, a number is added to the exponent so that the result is always positive. In general floating point numbers are of the form.

Q7) **why we represent sometime some numbers in sign magnitude form.**

Answer:
Representation of Numbers
There are four possibilities to represent integers.

1. Sign magnitude form
2. Radix complement form
3. Diminished radix complement form
4. Biased representation

Sign magnitude form
• This is the simplest form for representing a signed number
• A symbol representing the sign of the number is appended to the left of the Number
• This representation complicates the arithmetic operations
Radix complement form
• This is the most common representation.
• Given an m-digit base b number x, the radix complement of x is
$x^c = (b^m – x) \bmod b^m$
• This representation makes the arithmetic operations much easier.
Diminished radix complement form
• The diminished radix complement of an m-digit number x is $x^{c'}=b^m -1- x$
• This complement is easier to compute than the radix complement.
• The two complement operations are interconvertible, as $x^c= (x^{c'}+1) \bmod b^m$

==========

Set-04

Question No: 31 (Marks: 1)

What are the hardware interrupts in a computer system?Mention its utility.

Answer:

Hardware interrupts:

Hardware interrupts are generated by external events specific to peripheral devices. Most processors have at least one line dedicated to interrupt requests. When a device signals on this specific line, the processor halts its activity and executes an interrupt service routine.

Such interrupts are always asynchronous with respect to instruction execution, and are not associated with any particular instruction. They do not prevent instruction completion as exceptions like an arithmetic overflows does. Thus, the control unit only needs to check for such interrupts at the start of every new instruction. Additionally, the CPU needs to know the identification and priority of the device sending the interrupt request.

There are two types of hardware interrupt:

- Maskable Interrupts
- Non-maskable Interrupts

Question No: 32 (Marks: 1)

Consider a LAN, using bus topology. If we replace the bus with a switch, what change will occur in such a configuration?

Answer:

Bus versus switches

Consider a LAN, using bus topology. If we replace the bus with a switch, the speed of the data transfer will be improved to a great extent.

Question No: 33 (Marks: 2)

Where do you find the utility of hardware interrupts in a computer system?

Answer:

Question No: 34 (Marks: 2)

Differentiate between CPU register and Cache Memory.

Answer:

In simple terms, the cache is rather like the disk cache which means that access to data stored on a slow device like a hard disk can be cached in a faster store like system memory. The CPU cache uses very high speed memory on chip to speed up access to the much slower system memory. In both cases clever algorithms can be employed to 'look ahead' and pre-cache data which is likely to be used.

The Registers are rather like variables in a high level language and are used to store values which are actually being processed. For example with C = A + B, the values of A and B are loaded into Registers (like assigning variables) and then the instruction 'add A and B and store in C' is executed. Sometimes the next instruction would be to place this

value back into system memory (probably via the cache to speed up instructions which subsequently read this value).

Question No: 35 (Marks: 3)

Name three important schemes that are commonly used for error control.

Answer:
Error Control
Once an error is detected, what is the receiver going to do?
1. Do nothing
2. Return an error message to the transmitter
3. Fix the error with no further help from the transmitter

Do nothing

Seems like a strange way to control errors but some newer systems such as frame relay perform this type of error control.
Return a message has three basic formats:
1. Stop-and-wait ARQ
2. Go-back-N ARQ
3. Selective-reject ARQ

Stop-and-wait ARQ is the simplest of the error control protocols.
A transmitter sends a frame then stops and waits for an acknowledgment.
If a positive acknowledgment (ACK) is received, the next frame is sent.
If a negative acknowledgment (NAK) is received, the same frame is transmitted again.

Go-back-N ARQ and selective reject are more efficient protocols.
They assume that multiple frames are in transmission at one time (sliding window).
A sliding window protocol allows the transmitter to send up to the window size frames before receiving any acknowledgments.
When a receiver does acknowledge receipt, the returned ack contains the number of the frame expected *next*.
Asynchronous transfer mode (ATM) incorporates many types of error detection and error control.
ATM inserts a CRC into the data frame (the cell), which checks only the header and not the data.
This CRC is also powerful enough to perform simple error correction on the header.
A second layer of ATM applies a CRC to the data, with varying degrees of error control.

Question No: 36 (Marks: 3)

What do you understand by the term data synchronization ?
Explain briefly the following schemes of data synchronization in your own words
Synchronous transmission
Asynchronous transmission
Answer:
Data synchronization:
This means that the CPU should input data from an input device only when the device is ready to provide data and send data to an output device only when it is ready to receive data. There are three basic schemes which can be used for synchronization of an I/O data transmission:

- Synchronous transmission
- Semi-synchronous transmission
- Asynchronous transmission

Synchronous transmission:

This can be understood by looking at the waveforms shown in Figure A.
M stands for the bus master and S stands for the slave device on the bus. The master and the slave are assumed to be permanently connected together, so that there is no need for the selection of the particular slave device out of the many devices that may be present in the system. It is also assumed that the slave device can perform the transfer at the speed of the master, so no handshaking signals are needed.

Semi-synchronous transmission:

Figure B explains this type of transfer. All activity is still synchronous with the system clock, but in some situations, the slave device may not be able to provide the data to the master within the allotted time. The additional time needed by the slave, can be provided by adding an integral number of clock periods to the master's cycle time.
The slave indicates its readiness by activating the complete signal. Upon receiving this signal, the master activates the Enable signal to latch the data provided by the slave. Transfers between the CPU and the main memory are examples of semi-synchronous transfer.

Asynchronous transmission:

This type of transfer does not require a common clock. The master and the slave operate at different speeds. Handshaking signals are necessary in this case, and are used to coordinate the data transfer between the master and the slave as shown in the Figure C. When the master wants to initiate a data transfer, it activates its Ready signal. The slave detects this signal, and if it can provide data to the master, it does so and also activates its Acknowledge signal. Upon receiving the Acknowledge signal, the master uses the Enable signal to latch the incoming data .The master then deactivates its Ready line, and in response to it, the slave removes its data and deactivates its Acknowledge line.
In all the three cases discussed above, the waveforms correspond to an "input" or a "read" operation. A similar explanation will apply to an "output" or a "write" operation. It should also be noted that the latching of the incoming data can be done by the master either by using the rising edge of the Enable signal or by using its falling-edge. This will depend on the way the intermediate circuitry between the master and the slave is designed.

Question No: 37 (Marks: 3)

Differentiate between Spatial Locality And Temporal Locality .

Answer:

If a pair of computers communicates once, the pair is likely to communicate again in the near future and then periodically. The pattern is called temporal locality of reference to imply a relationship over time. A computer tends to communicate most often with other computers that are nearby. This pattern is called physical/spatial locality of reference.

Locality of reference Principle:

Locality of reference or principle of Locality helps in predicting the computer communication pattern. It deals with the concept of accessing single resource multiple times. There are three basic types of locality of reference.

1) Spatial Locality of Reference.

2) Temporal locality of Reference.
3) Sequential Locality of Reference.

Spatial Locality of Reference:

In this pattern computer are likely to communicate with other computers located nearby. The concept that likelihood of referencing a resource is higher near it was just referenced.

Temporal Locality of Reference:

It is the concept that the resource that is referenced at one point in time will be referenced in the near future.

Question No: 38 (Marks: 5)

Given a 16-bit parallel output port attached with the FALCON-A CPU as shown in the figure. The port is mapped onto address DEh of the FALCON-A s I/O space. Sixteen LED branches are used to display the data being received from the FALCON-A s data bus. Every LED branch is wired in such a way that when a 1 appears on the particular data bus bit, it turns the LED on; a 0 turns it off.
Which LEDs will be ON when the instruction
out r2, 222
executes on the CPU? Assume r2 contains 1234h. 10 marks question (very tough)
Answer:

Question No: 39 (Marks: 5)

Consider a 4 way set-associative cache with 256KB capacity and 32 byte lines
a) How many sets are there in the cache?
b) How many bits of address are required to select a set in cache?

Answer:

Consider a 2-way set-associative cache with 64KB capacity and 16 byte lines.

a. How many sets are there in the cache?
b. How many bits of address are required to select a set in the cache?
c. Repeat the above two calculations for a 4-way set-associative cache with same size.

Solution

a. A 64KB cache with 16 byte lines contains 4096 lines of data. In a 2-way set associative cache, each set contains 2 lines, so there are 2048 sets in the cache.
b. Log2(2048)=11. Hence 11 bits of the address are required to select the set.
c. The cache with 64KB capacity and 16 byte line has 4096 lines of data. For a 4-way set associative cache, each set contains 4 lines, so the number of sets in the cache would be 1024 and $\text{Log}_2(1024) = 10$. Therefore 10 bits of the address are required to select a set in the cache.

Question No: 40 (Marks: 10)

Describe the following features of FALCON-A Assembler

Symbol Table

I/O Ports
List File
Single Step
Error Log
Answer:
Incomplete

Question No: 41 (Marks: 10)

How many platters are required for a 40GB disk if there are 1024 bytes/sector, 2048 sectors per track and 4096 tracks per platter
How many platters are required for a 80GB disk if there are 1024 bytes/sector, 2048 sectors per track and 4096 tracks per platter

Answer:

How many platters are required for an 80GB disk if there are 2048 bytes/sector, 2048 sectors per track and 2048 tracks per platter?

Solution
The capacity of one platter
= 2048 x 2048 x 2048
= 8GB
For an 80GB hard disk, we need 80/8
= 10 such platters.

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Set-05

My Paper of CS501 19.07.2011

What is DMA?
Answered Above
Differentiate between throughput and latency?
Answered Above

Describe six attributes of SRC Processor?
Answer

Briefly Describe Classification of Networks?

Write note on Pipelining?

What is virtual memory?

How does work Associative Mapping?

How does work set Associative Memory?

How overflow is represented in case of floating point?

==========

Set-06

This is my cs501 Advance computer architecture paper

Q1 (Marks: 5)

Consider a 4 way set-associative cache with 256KB capacity and 32 byte lines
a) How many sets are there in the cache?
b) How many bits of address are required to select a set in cache?

Answer:

Question: 4 **[10 Marks]**

Consider a two way-set associative cache with 16 byte lines and 2048 lines of data.

a. Find the capacity of the cache.
b. How many bits of the addresses are required to select a set in the cache?

Answer:

a.

Capacity of the cache= 16×2048
= 32768 B
= 32KB

b.

Number of sets= 2048
2
= 1024

Number of address bits required to select a set= $\text{Log}_2(1024)$
= 10

Q2 convert the hexadecimal number B316 to base 10 5Marks

Answered above

Q3 what do you know about booth pair recording 3marks

Answer:

Bit-Pair Recoding

Booth recoding may increase the number of additions due to the number of isolated 1s. To avoid this, bit-pair recoding is used. In bit-pair recoding, bits are encoded in pairs so there are only n/2 additions instead of n.

Division

There are two types of division:

• Integer division
• Fraction division

Integer division

The following steps are used for integer division:

1. Clear upper half of dividend register and put dividend in lower half. Initialize quotient counter bit to 0
2. Shift dividend register left 1 bit
3. If difference is +ve, put it into upper half of dividend and shift 1 into quotient. If –ve, shift 0 into quotient
4. If quotient bits<m, goto step 2
5. m-bit quotient is in quotient register and m-bit remainder is in upper half of dividend register

Q.4 assembler symbol table note.3-marks:

Answer:
The FALCON-A Assembler source code has two main modules, the 1st-pass module and the 2nd-pass module. The 1st-pass module takes an assembly file with a (.asmfa) extension and processes the file contents. It then generates a Symbol Table which corresponds to the storage of all program variables, labels and data values in a data structure at the implementation level. The Symbol Table is used by the 2nd-pass module. Failures of the 1st-pass are handled by the assembler using its exception handling mechanism.
The 2nd-pass module sequentially processes the .asmfa file to interpret the instruction opcodes, register op-codes and constants using the Symbol Table. It then produces a list file with a .lstfa extension independent of successful or failed pass. If the pass is successful a binary file with a .binfa extension is produced which contains the machine code for the program contained in the assembly file.

Q.5 configuration of 1x8 memory cell .3marks

Answer:1×8 Memory Cell Array (1D)
In this arrangement, each block is connected through a bi-directional data bus implemented with 2 tri-state buffers. and Select signals are common to all these cells. This 1-dimentional memory array could not be very efficient, if we need to have a very large memory.

4×8 Memory Cell Array (2D)
In this arrangement, 4×8 memory cell array is arranged in 2-dimensions. At the input, we have a 2×4 decoder. Two address bits at the input A0 and A1 would be decoded into 4 select lines. The decoder selects one of four rows of cells and then signal specifies whether the row will be read or written.

A 64k×1 Static RAM Chip
The cell array is indicated as 256 × 256. So, there would be 256 rows and 256 columns. A 64k × 1 cell array requires 16 address lines, a read/write line, , a chip select line,CS, and only a single data line. The lower order 8-address lines select one of the 256 rows using an 8-to-256 line row decoder. Thus the selected row contains 256 bits. The higher order 8-address lines select one of those 256 bits. The 256 bits in the row selected flow through a 256-to-1 line multiplexer on a read. On a memory write, the incoming bit flows through a 1-to-256 line de-multiplexer that selects the correct column of the 256 possible columns.

A 16k×4 Static RAM Chip
In this case, memory is arranged in the form of four 64×256 memory cells. Four bits can be read and written at a time. For this, we use one 8-256 row decoder, four 64-1 muxes

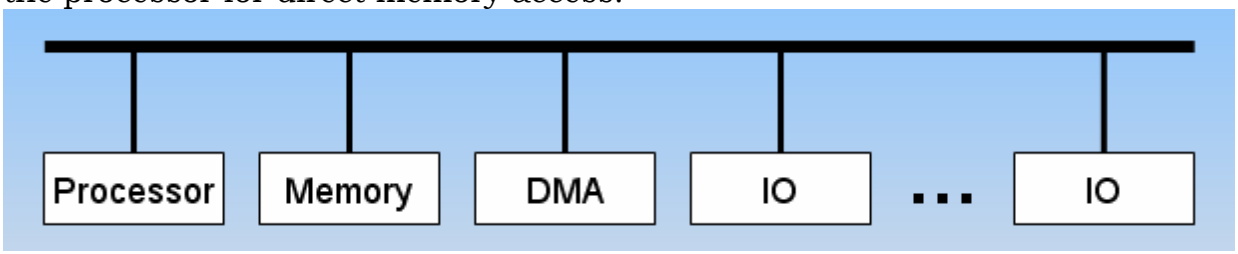
and four 1-64 de muxes. The lower address lines (A0-A7) are decoded into 28 lines, 26 lines from these 28 are used to select row from one of the four 64×256 cell array and the remaining 22 lines are used to select one of the 64×256 cell array. Now the upper address lines (A8-A13) are input into the 4 muxes and their output is used to select the required column from the four 64×256 cell arrays. Control lines read/write, , chip select, CS,are just similar to previous arrangement.

Q.6 Single Bus Detached DMA 5marks

Answer:

Single Bus Detached DMA

In the example provided by the above diagram, there is a single bidirectional bus connecting the processor, the memory,the DMA module and all the I/O modules. When a particular I/O module needs to read or write large amounts contiguous data it requests the processor for direct memory access.



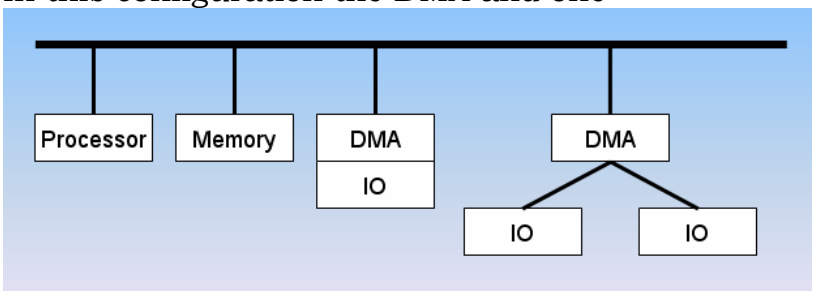
If permission is granted by the processor, the I/O module sends the read or write address and the size of data needed to be read or written to the DMA module. Once the DMA module acknowledges the request, the I/O module is free to read or write its contiguous block of data from or onto main memory. Even though in this situation the processor will not be able to execute while the transfer is going on (as there is a just a single bus to facilitate transfer of data), DMA transfer is much faster then having each word of memory being read by the processor and then being written to its location.

Question Single Bus Integrated DMA 5 Marks

Answer:

Single Bus Integrated DMA

In this configuration the DMA and one

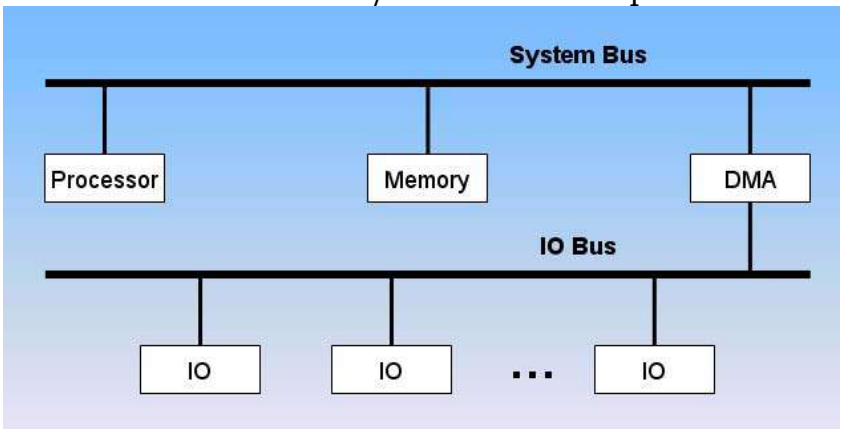


or more I/O modules are integrated without the inclusion of system bus functioning as the part of I/O module or may be as a separate module controlling the I/O module.

Q: Define IO Bus 5 Marks

IO Bus

In this configuration we integrate the DMA and I/O modules through an I/O bus. So it will cut the number of I/O interfaces required between DMA and I/O module.



Q.7 what is hardisk 2 marks

Answer: A hard disk drive (HDD; also hard drive, hard disk, or disk drive)[2] is a device for storing and retrieving digital information, primarily computer data. It consists of one or more rigid (hence "hard") rapidly rotating discs (often referred to as platters), coated with magnetic material and with magnetic heads arranged to write data to the surfaces and read it from them.

Hard drives are classified as non-volatile, random access, digital, magnetic, data storage devices. Introduced by IBM in 1956, hard disk drives have decreased in cost and physical size over the years while dramatically increasing in capacity and speed.

Hard disk drives have been the dominant device for secondary storage of data in general purpose computers since the early 1960s.[3] They have maintained this position because advances in their recording capacity, cost, reliability, and speed have kept pace with the requirements for secondary storage.[3]

Q.8 difference bw connection oriented and connection less

Answer:

Connection Oriented vs. Connection less Communication

Connection Oriented Communication

• In this method, same path is always taken for the transfer of messages.
• It reserves the bandwidth until the transfer is complete. So no other server could use that path until it becomes free.
• Telephone exchange and circuit switching is the example of connection oriented communication.

Connection less Communication

• Here message is divided into packets with each packet having destination address.
• Each packet can take different path and reach the destination from any route by looking at its address.
• Postal system and packet switching are examples of connection less communication.

Q.9 pipeline disadvantage 3 marks

Answered Above

- **Data dependence**
- **Branch delay**
- **Load delay**

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Set-07

FINAL CS501 BY
25 July 2011
5 marks

1. The following table shows a partial summary of the ISA for the SRC. Write an assembly language program using the SRC assembly language to evaluate the expression:

Z= (7 + 16a) - (8b - c)

Note: a, b and c are names of memory locations. Your program should not change the source operands. Do not worry about the contents of a and b. There is no need to worry about assembler directives. Comments in your code may be helpful.
Find the bandwidth of a memory system that has a latency of 30ns, a pre charge time of 10ns and transfers 3 bytes of data per access **.**

2. Explain the Direct Mapping cache strategy.
3. How many platters are required for a 40GB disk if there are 1024 bytes/sector, 2048 sectors per track and 4096 tracks per platter?

3 marks

What do you understand by RAID 2?

Answer:

RAID stands for Redundant Array of Independent Disks and with at least two hard disk drives you can setup them as a RAID array in order to increase the disk performance or to improve data reliability.
Building a RAID system:
Requirements:-
In order to have a RAID system on your PC you will need two things: a RAID controller and at least two identical hard disk drives. If you want to setup a system different from RAID0 or RAID1 more hard disk drives may be necessary. Assuming that you are going to build a RAID0 or a RAID 1 system, so assume a system with two hard disk drives from now on.
So the first thing you need to check is whether your motherboard has an embedded RAID controller or not. This can be seen on the manual of your motherboard. The motherboard chipset – the south bridge chip (which is also known as ICH, I/O Controller Hub, on Intel chipsets) to be more exact – is in charge of controlling the hard disk ports of your motherboard. So the south bridge chip of your motherboard needs to have an embedded RAID controller. On Intel chipsets, this chip needs to have the letter "R" in order to have this feature. For instance, ICH7 chip does not have RAID feature, while ICH7R does. The same thing may happen with chipsets from other suppliers.

If your motherboard doesn't have a RAID chip, you still can use a RAID system by buying an add-on RAID controller.
In order to have a RAID system on our PC we will need two things: a RAID controller and at least two identical hard disk drives.
Installation:-
The RAID installation process is divided into three parts:
Physical installation, where we install the hard disk drives on our PC in such a way they will be able to be used as a RAID system;
RAID configuration, where we setup the system to use the two hard disk drives as a RAID array.
Operating system installation, where we need to install the operating system loading a special driver in order to recognize our RAID array.
Physical installation:
The physical installation is pretty straightforward: install our hard disk drives to our case, connect a power supply plug on each hard disk drive and connect each hard disk drive to the appropriate hard disk drive port on the motherboard.
RAID configuration:
After the physical installation our hard disk drives will operate as two separated hard disk drives. So we need to configure them as a RAID system.
We need to enter first on the motherboard setup and configure them as "RAID" instead of "IDE". Under "IDE" configuration they work as normal IDE ports, while under "RAID" configuration we can enable them to work as a RAID system.
Operating System Installation:
The problem is that Windows XP doesn't automatically recognize RAID systems, so it will think that our computer has no hard disk drives installed.
We need to generate a floppy disk containing the RAID controller driver. Motherboards used to come with this disk in the past, but nowadays we will have to create it by our self, running a small utility present on the CD-ROM that comes with our motherboard or add-on RAID controller. This utility will be located on a directory called RAID or similar.

1. Give an example for the logic design level, circuit level and mask level abstractions of digital design.

Answer:
Logic Design Level
The logic design level is also called the gate level. The basic elements at this level are gates and flip-flops. The behavior is less visible, while the hardware structure predominates.
The above level relates to "logic design".
Circuit Level
The key elements at this level are resistors, transistors, capacitors, diodes etc.
Mask Level
The lowest level is mask level dealing with the silicon structures and their layout that implement the system as an integrated circuit.
The above two levels relate to "circuit design".
The focus of this course will be the register transfer level and the instruction set level, although we will also deal with the PMS level and the Logic Design Level.

Differentiate between Spatial Locality And Temporal Locality .

Answered above:

2. Suppose an I/O system with a single disk gets (on average) 200 I/O requests/second. Assume that average time for a disk to service an I/O request is 4ms. What is the utilization of the I/O system? 2 marks

Answered Above:

1. Which term do we use to describe a "storage systems" resilience to disk failure through the use of multiple disks and by the use of data distribution and correction techniques?

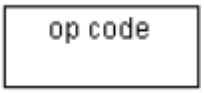
2. Differentiate between CPU register and Cache Memory.

Write one advantage and one disadvantage of cache design.

Answer:
Advantage:
Simplicity
Disadvantage:
Only a single block from a given group is present in cache at any time. Direct map Cache imposes a considerable amount of rigidity on cache organization.

What is the format of a 0-address instruction set?

Answer:
0-address instruction
A 0-address instruction uses a stack to hold both the operands and the result. Operations are performed on the operands stored on the top of the stack and the second value on the stack. The result is stored on the top of the stack. Just like the use of an accumulator register, the addresses of the stack registers need not be specified, their usage is implicit. Therefore, only one field is required in 0-address instruction; it specifies the op-code.



FINAL CS501 BY
25 July 2011

How many drives do you need a minimum to form RAID 0?
0
Only 1
Minimum 2
Maximum 2

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Set-08

CS501

My Today Paper (15.07.2011)

Q1 what is assembler and what is it important in assembly language (2)

Answer:

Q2 what is program instruction control? (2)

Answer:

Q3 define virtual memory (2)

Answer:

Q4 difference between higher level language and assembler (3)

Answer:

Q5 define ISA (3)

Answer:

Q6 convert (390)10 into base 16 (5)

Answer:

Q7 define pipelining (5)

Answer:

Q8 define the type of error control (5)

Answer:

Q9 define booth recording (2)

Answer:

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Set-09

5 marks question
Define RAID 0
Calculate bandwidth
Discuss problems of Pipelining

3 marks questions
Differenciate Shared Medium and Switched Medium
R[ra] = R[rb] - R[rc] Discuss its functionality

Serial and Parallel data transfer
Cache Direct Memory access approach

2 marks questions
How you define microprogramming
Interrupt driven I/O
In Bus topology if we change bus to switch then what will happen

MCQ
RAID related 4-5
ISR related 4-5
Interrupt driven I/O 2-3
Cache 2-3
RISC and CISC 2

Today is my paper
52 total question
40 one no mcq
what is ISA, explain ? 5 marks
how instruction set is defined 5 marks
one numircal 2 marks?
mostly mcq from the old papers.....about 60%

CS501 Final Term Current Paper (Feb 2011)

differentiate b/w RISC n CISC according to their instruction size and hardware, software? 5 marks.
find total capacity of hard disk. (it was the same example that is on page no. 304 examle no 3 of our handouts.) 5 marks.
what is the finction of Cntrol unit? 3 marks.
what is the difference between control unit n data path? 2 marks
what is the working of DMA controller? 5 marks
define 64K x 1 static RAM chip? 5 marks.
total were 52 questions. Mcqs were quite easy. bt...

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Set-10

Write short answers to the following questions: [3 x 5]

a. What is the advantage of a linker in the development of assembly language programs?

Solution:-

The linker:

When developing large programs, different people working at the same time can develop separate modules of functionality. These modules can then be 'linked' to form a single module that can be loaded and executed. The modularity of programs, that the linking step in assembly language makes possible, provides the

same convenience as it does in higher-level languages; namely abstraction and separation of concerns. Once the functionality of a module has been verified for correctness, it can be re-used in any number of other modules. The programmer can focus on other parts of the program. This is the so-called "modular" approach, or the "top-down" approach.

b. Define term "Single stepping".

Solution:-

Single stepping:

Single stepping and breakpoints that allow the examination of the status of the program and registers at desired points during execution.

c. Define term "Type checking".

Solution:-

Type Checking:-

High-level languages provide various primitive data types, such as integer, Boolean and a string, that a programmer can use. Type checking provides for the verification of proper usage of these data types. It allows the compiler to determine memory requirements for variables and helping in the detection of bad programming practices.

On the other hand, there is generally no provision for type checking at the machine level, and hence, no provision for type checking in assembly language. The machine only sees strings of bits. Instructions interpret the strings as a type, and it is usually limited to

signed or unsigned integers and floating point numbers. A given 32-bit word might be an instruction, an integer, a floating-point number, or 4 ASCII characters. It is the task of the

compiler writer to determine how high-level language data types will be implemented using the data types available at the machine level, and how type checking will be implemented.

d. Define term "Instruction set".

Solution:-

Instruction Set

A collection of all possible machine language commands that a computer can understand and execute is called its instruction set. Every processor has its own unique instruction set. Therefore, programs written for one processor will generally not run on another processor. This is quite unlike programs written in higher-level languages, which may be portable. Assembly/machine languages are generally unique to the processors on which they are run, because of the differences in computer architecture.

Three ways to list instructions in an instruction set of a computer:

- by function categories
- by an alphabetic ordering of mnemonics
- by an ascending order of op-codes

e. Why computer logic design is different from classical logic design?

Solution:-

Classical logic design versus computer logic design:

The traditional sequential circuit design techniques for a finite state machine are not very practical when it comes to the design of a computer, in spite of the fact that a computer is a finite state machine. The reason is that employing these techniques is much too complex as the computer can assume hundreds of states.

==========

Set-11

b) Give short answers: [5]

1. When exceptions must be disabled?

Machine Exceptions

• Anything that interrupts the normal flow of execution of instructions in the processor is called an exception.

• Exceptions may be generated by an external or internal event such as a mouse click or an attempt to divide by zero etc.

• External exceptions or interrupts are generally asynchronous (do not depend on the system clock) while internal exceptions are synchronous (paced by internal clock)

The exception process allows instruction flow to be modified, in response to internal or external events or anomalies. The normal sequence of execution is interrupted when an exception is thrown.

2. How machine check exceptions are generated?

Question No: 10 (Marks: 15)

a. Briefly describe the following errors with respect to serial communication. [9]

i- Frame error

ii- Parity

iii-Overrun

b. List down the advantages of Virtual Memory [6

QuestionNo.1 Marks:15

Consider a hard disk that rotates at 6000 rpm. The seek time to move the head between adjacent tracks is 1 ms. There are 64 sectors per track stored in linear order. Assume that the read/write head is initially at the start of sector 1 on track 7.

(a) How long will it take to transfer sector 1 on track 7 to sector 1 on track 9?

(b) How long will it take to transfer all the sectors on track 12 to corresponding sectors on track 13?

QuestionNo.2 Marks:10

Briefly describe five important features of RISC machines 5 marks

a) Drawing a timing diagram, briefly explain the sequence of steps that take place during a synchronous transfer between a master device and a slave device.

(b) List one advantage and one disadvantage of DMA

Consider a DRAM with 2048 rows and a refresh time of 20ms.
(a) Find the frequency of row refresh operations.
(b) What fraction of the DRAM's time is spent on refreshing if each refresh takes 100ns

Question No: 11 (Marks: 15)

a) What are the approaches used to design a Control unit? Briefly compare them. [5]
b) Evaluate the instruction z = 16(a -b) + 32(c+58) with the 3 address machine.[5]
c) What is the difference between "branch" and "branch link" instructions of SRC? [5]

Question No: 12 (Marks: 10)

A hard disk with 5 platters has 1024 tracks per platter, 512 sectors per track and 512 bytes/sector.
a) What is the total capacity of the disk? [8]
b) How many platters are required for a 80GB disk if there are 1024 bytes/sector, 2048 sectors per track and 4096 tracks per platter. [2]

Question No: 14 (Marks: 10)

Give comparison of advantages and disadvantages of serial and parallel transfer of data between the CPU and an I/O device. [10]

Question No: 15 (Marks: 10)

What are different I/O techniques? Briefly describe the comparison of Interrupt driven I/O and Polling. [3+7]

Compare Programmed I/O,Interrupt driven I/O,Polling and Direct Memory Access(DMA) and explain which technique is best suited for data transfer.Give reasons for your answer
Programmed I/O refers to the situation when all I/O operations are performed under the direct control of a program running on the CPU. This program, which usually consists of a "tight loop", controls all I/O activity, including device status sensing, issuing read or write commands, and transferring the data. A subsequent I/O operation cannot begin until the current I/O operation to a certain device is complete. This causes the CPU to wait, and thus makes the scheme extremely inefficient
Polling is the process of periodically checking the status of a device to see if it is ready for the next I/O operation. It is the simplest way for an I/O device to communicate with the CPU. The device indicates its readiness by setting certain bits in a status register, and the CPU can read these bits to get information about the device. Polling wastes a lot of CPU time and it is a very inefficient way of I/O operations. An improved way of polling is

to include a memory of suitable size with I/O devices. This memory is often called buffer. The CPU can use this buffer less often than polling. However, the disadvantage of using buffers is that when the buffer is filled up, the I/O operation may be halted as it will not be possible to add additional data to the buffer.
• Interrupts are used to demand attention from the CPU.
• Interrupts are asynchronous breaks in program flow that occur as a result of events outside the running program.
• Interrupts are usually hardware related, stemming from events such as a key or button press, timer expiration, or completion of a data transfer.
The basic purpose of interrupts is to divert CPU processing only when it is required. As an example let us consider the example of a user typing a document on word-processing software running on a multi tasking operating system. It is up to the software to display a character when the user presses a key on the keyboard. To fulfill this responsibility the processor can repeatedly poll the keyboard to check if the user has pressed a key. However, the average user can type
at most 50 to 60 words in a minute. The rate of input is much slower than the speed of the processor. Hence, most of the polling messages that the processor sends to the keyboard will be wasted. A significant fraction of the processor's cycles will be wasted checking for user input on the keyboard. It should also be kept in mind that there are usually multiple peripheral devices such as mouse, camera, LAN card, modem, etc. If the processor would poll each and every one of these devices for input, it would be wasting a large amount of its time. To solve this problem, interrupts are integrated into the system. Whenever a peripheral device has data to be exchanged with the processor, it interrupts the processor; the processor saves its state and then executes an interrupt handler routine (which basically exchanges data with the device).
Interrupt driven I/O is better than polling. In the case of polling a lot of time is wasted in questioning the peripheral devices whether it is ready for delivering the data or not. In the case of interrupt driven I/O the CPU time in polling is saved.
In interrupt driven I/O the I/O transfer depends upon the speed at which the processor tests and service a device. Also, many instructions are required for each I/O transfer. These factors become bottleneck when large blocks of data are to be transferred. While in the DMA technique the I/O transfers take place without the intervention by the CPU, rather CPU pauses for one bus cycle. So DMA technique is the most efficient technique for I/O transfers.

Question No: 16 (Marks: 10)

Assume a network with a bandwidth of 2500Mbits/sec. It has a sending overhead of 200µsec and a receiving overhead of 160µsec. Assume two machines connected together. It is required to send a 15,000 byte message from one machine to the other (including header), and the message format allows 15, 00 bytes in a single message. Calculate the total latency to send the message from one machine to another assuming they are 25m apart (as in a SAN). Next, perform the same calculation but assume the machines are 750m apart (as in a LAN).Finally, assume they are 1500Km apart (as in a WAN). Assume that signals propagate at 1/3 of the speed of light in a conductor, and that the speed of light is 300,000Km/sec.

Write different schemes related to virtual memory organization. 10 markas

Suppose we have 10 magnetic tapes, each containing 20GB. Assume that there are enough tape readers to keep any network busy. How long will it take to transmit the data over a distance of 3Km? The choices are category 5 twisted-pair wires at 100Mbits/sec, multimode fiber at 1500Mbits/sec and single-mode fiber at 3000Mbits/sec. 15 marks.

Consider a hard disk that rotates at 4000 rpm. The seek time to move the head between adjacent tracks is 2 ms. There are 64sectors per track stored in linear order.
Assume that the read/write head is initially at the start of sector 1 on track 7.
a. How long will it take to transfer sector 1 on track 6 to sector 1 on track 9?
b. How long will it take to transfer all the sectors on track 11 to corresponding sectors on track 13?

a. What should be the polling frequency for an I/O device if the average delay between the time when the device wants to make a request and the time when it is polled, is to be at most 12 ms?
b. If it takes 15,000 cycles to poll the I/O device, and the processor operates at 200MHz, what % of the CPU time is spent polling?
c. What should be the polling frequency if the system wants to provide an average delay of 3msec?

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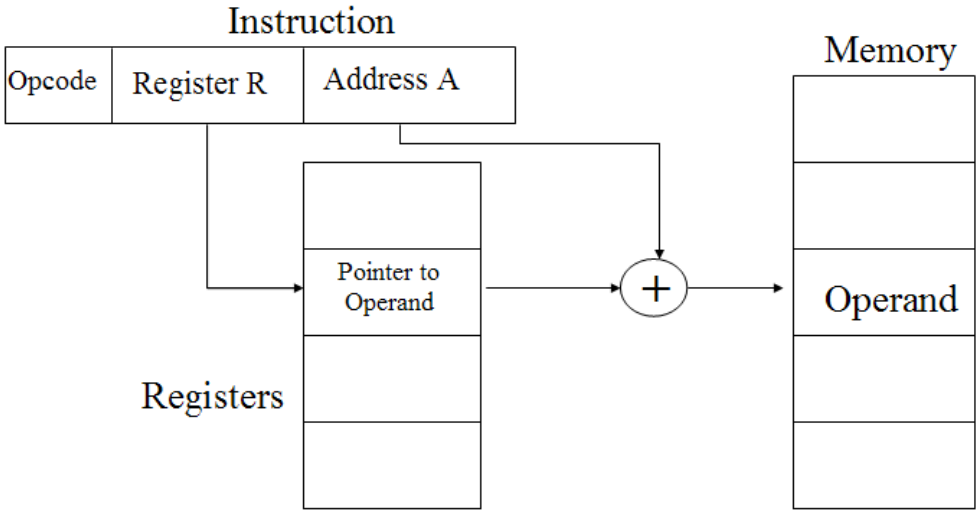
Set-12

Thu Mar 25, 2010 9:59 am
FINALTERM EXAMINATION
Fall 2009
CS501- Advance Computer Architecture

Time: 120 min
Marks: 75
Question No: 1 (Marks: 1) - Please choose one
The CPU includes three types of instructions, which have different operands and will need different representations.
Which one of the instructions requires two source registers?
► **Jump and branch format instructions Page 185**
► Immediate format instructions
► Register format instructions
► All of the above
In this figure, the constant value specified by the immediate field is added to the register value, and the resultant is the index of memory location that is referred i.e. Effective

Address = A + (content of R) .
Identify the addressing mode.



► **Displacement**
► Immediate
► Indexed
► Relative

Question No: 3 (Marks: 1) - Please choose one
In which one of the following addressing modes, the operand does not specify an address but it is the actual data to be used.
► Direct
► Indirect
► **Immediate**
► Relative

Question No: 4 (Marks: 1) - Please choose one
Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A and source register B) from the following example.
ADD R1, R2, R3
► Opcode= R1, DR=ADD, SA=R2, SB=R3
► Opcode= ADD, DR=R1, SA=R2, SB=R3
► Opcode= R2, DR=ADD, SA=R1, SB=R3
► **Opcode= ADD, DR=R3, SA=R2, SB=R1**

Question No: 5 (Marks: 1) - Please choose one
When the address of the subroutine is already known to the Microprocessor then it is called as --------- interrupt.
► Maskable
► Non-maskable
► **Non-vectored**
► vectored

Question No: 6 (Marks: 1) - Please choose one
The interrupts which are pre-programmed and the processor automatically finds the address of the ISR using interrupt vector table are
► Maskable
► Non-maskable
► Non-vectored
► **Vectored**

Question No: 7 (Marks: 1) - Please choose one
Which is the last instruction of the ISR that is to be executed when the ISR terminates?
► IRET
► IRQ
► INT
► NMI
Question No: 8 (Marks: 1) - Please choose one
When is the "Divide error interrupt" generated?
► When an attempt is made to divide by decimal number
► When an attempt is made to multiply by zero
► **When an attempt is made to divide by zero**
► When negative number is stored in a register
Question No: 9 (Marks: 1) - Please choose one
Identify the following type of serial communication error condition:
"The prior character that was received was not still read by the CPU and is over written by a new received character."
► Framing error
► Parity error
► **Overrun error page 242**
► Under-run error
Question No: 10 (Marks: 1) - Please choose one
Which one of the following is a term used to describe a storage systems' resilience to disk failure through the use of multiple disks and by the use of data distribution and correction techniques?
► Interrupt handling
► Programmed I/O
► Polling
► **RAID**
Question No: 11 (Marks: 1) - Please choose one
_____ is the time for first bit of the message to arrive at the receiver including delays.
► Transmission Time
► Latency
► Transport Latency
► **Time of Flight page 375**
Question No: 12 (Marks: 1) - Please choose one
For a request of data if the requested data is not present in the cache, it is called a _____
► **Cache Miss pg 349**
► Spatial Locality
► Temporal Locality
► Cache Hit
For a request for data, if the data is available in the cache it results in a cache hit. And if the requested data is not pres ent in the cache, it is called a cache miss
Question No: 13 (Marks: 1) - Please choose one
An entire _____ memory can be erased in one or a few seconds which is much faster than EPROM.
► PROM
► Cache
► EEPROM

► **Flash Memory pg 348**

Question No: 14 (Marks: 1) - Please choose one

A combination of parallel and sequential hardware used to build a multiplier is known as _____

► Parallel Array Multiplier
► Booth Recording
► **Series Parallel Multiplier page 336**
► None of the given

Question No: 15 (Marks: 1) - Please choose one

The _____ of an m digit number x is xc'=bm -1- x

► Radix Compliment
► **Diminished Radix Compliment page 331**
► Signed Magnitude Form
► Biased Representation

Question No: 16 (Marks: 1) - Please choose one

Along with information bits we add up another bit which is called the bit.

► CRC
► Hamming
► Error Detection
► **Parity**

Question No: 17 (Marks: 1) - Please choose one

Falcon-A Simulator loads a FALCON-A binary file with a _____ extension and presents its contents into different areas of the simulator.

► .bin
► **.binfa**
► .fa
► None of the given

Question No: 18 (Marks: 1) - Please choose one

In machines where instructions can be executed in parallel or out of order, two additional hazards can occur: WAW and ----------

► None fo the given
► WAR
► **RAW**
► RAR

Question No: 19 (Marks: 1) - Please choose one

---------- is the memory address of an interrupt handler.

► **Interrupt vector**
► Interrupt service routine
► Exception
► Mask

Question No: 20 (Marks: 1) - Please choose one

Why DMA is faster than Programmer I/O technique ?

• ► DMA transfers data directly using CPU.
• ► **DMA transfers data directly without using CPU**
• ► DMA uses buffers with CPU
• ► DMA uses interrupted driven I/O

Question No: 21 (Marks: 1) - Please choose one

For _____ of an error we just need to know that there exists an error.

► None of the given
► Correction
► Detection
► Both Correction and Detection

Question No: 22 (Marks: 1) - Please choose one
In _____ recording ,bits are encoded in pairs so there are only ' n/2' additions instead of 'n'.
► Booth Recording
► Bit Pair Recording
► Integer division
► None of the given

Question No: 23 (Marks: 1) - Please choose one
_____ are computed by the ALU and stored in processor status register.
► Condition codes
► Conditional Branches
► Fraction Division
► None of the given

Question No: 24 (Marks: 1) - Please choose one
In floating point representations _____ is also called mantissa.
► Sign
► Base
► Significand
► Exponent

Question No: 25 (Marks: 1) - Please choose one
Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)?
► Framing error
► Parity error
► Overrun error
► Under-run error

Question No: 26 (Marks: 1) - Please choose one
What should be the behavior of interrupts during critical sections?
► Must remain Disable
► Must remain Enable
► Can be either enable or disable
► Only important interrupts be enable.

Question No: 27 (Marks: 1) - Please choose one
The _____signal coming from the CPU tells the memory that some interaction is required between the CPU and memory.
► R/W
► COMPLETE
► None of the given
► REQUEST

Question No: 28 (Marks: 1) - Please choose one
_____ is the simplest form for representing a signed number
► Sign Magnitude Form

► None of the given
► Biased Representation

► Diminished Radix Compliment Form

Question No: 29 (Marks: 1) - Please choose one

Which of the instruction is used to load register from memory using a relative address?

► ld instruction

► ldr instruction

► lar instruction

► str instruction

Question No: 30 (Marks: 1) - Please choose one

_____ is/are defined as the number of instructions processed per second

► Throughput

► Latency

► Throughput and Latency

► None of the given

Question No: 31 (Marks: 1)

How many bits are included in one 1KByte ?

Question No: 32 (Marks: 1)

In which type of interrupts, the address of the service routine needs to be supplied externally by the device?

Answer: **Non-vectored**

Question No: 33 (Marks: 2)

What do you know about PROM ? Explain briefly

Question No: 34 (Marks: 2)

Share yours knowledge of interrupt vector in simple and precise paragraph.

Question No: 35 (Marks: 3)

What is a non-maskable interrupt (NMI) and what is its role?

Question No: 36 (Marks: 3)

Highlight the similarity and difference between RAID level 3 and RAID level 4.

Answer:

Similarities between RAID Levels 2 and 3

- Make use of parallel access techniques.
- All member disks participate in execution of every request.
- Spindles of the individual drives are synchronized
- Data striping is used.
- Strips are as small as a single byte or word.

Features of RAID Level 5

- Organized in a similar fashion to RAID 4
- The only difference is that RAID 5 distributes the parity strips across all disks.

RAID

RAID is a technology that is used to increase the performance and/or reliability of data storage. The abbreviation stands for *Redundant Array of Inexpensive Disks*. A RAID system consists of two or more disks working in parallel. These disks can be hard discs but there is a trend to also use the technology for solid state drives. There are different RAID levels, each optimized for a specific situation. These are not standardized by an industry group or standardisation committee. This explains why companies sometimes come up with their own unique numbers and implementations.

The software to perform the RAID-functionality and control the hard disks can either be located on a separate controller card (a hardware RAID controller) or it can simply be a driver. Some versions of Windows, such as Windows Server 2003, as well as Mac OS X include software RAID functionality. Hardware RAID controllers cost more than pure software but they also offer better performance.

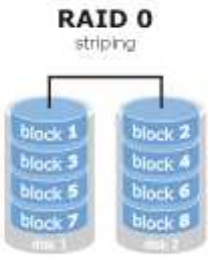
RAID-systems can be based with an number of interfaces, including SCSI, IDE, SATA or FC (fibre channel.) There are systems that use SATA disks internally but that have a FireWire or SCSI-interface for the host system.

Sometimes disks in a RAID system are defined as JBOD, which stands for *'Just a Bunch Of Disks'*. This means that those disks do not use a specific RAID level and acts as stand-alone disks. This is often done for drives that contain swap files or spooling data.

Below is an overview of the most popular RAID levels:

RAID level 0 – Striping

In a RAID 0 system data are split up in blocks that get written across all the drives in the array. By using multiple disks (at least 2) at the same time, this offers superior I/O performance. This performance can be enhanced further by using multiple controllers, ideally one controller per disk.



Advantages

- RAID 0 offers great performance, both in read and write operations. There is no overhead caused by parity controls.
- All storage capacity is used, there is no disk overhead.
- The technology is easy to implement.

Disadvantages

RAID 0 is not fault-tolerant. If one disk fails, all data in the RAID 0 array are lost. It should not be used on mission-critical systems.

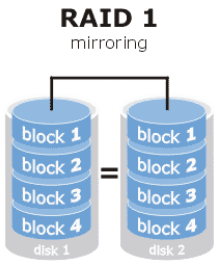
Ideal use

RAID 0 is ideal for non-critical storage of data that have to be read/written at a high speed, such as on a Photoshop image retouching station.

RAID level 1 – Mirroring

Data are stored twice by writing them to both the data disk (or set of data disks) and a mirror disk (or set of disks) . If a disk fails, the controller uses either the data drive or the

mirror drive for data recovery and continues operation. You need at least 2 disks for a RAID 1 array.



RAID 1 systems are often combined with RAID 0 to improve performance. Such a system is sometimes referred to by the combined number: a RAID 10 system.

Advantages

- RAID 1 offers excellent read speed and a write-speed that is comparable to that of a single disk.
- In case a disk fails, data do not have to be rebuild, they just have to be copied to the replacement disk.
- RAID 1 is a very simple technology.

Disadvantages

- The main disadvantage is that the effective storage capacity is only half of the total disk capacity because all data get written twice.
- Software RAID 1 solutions do not always allow a hot swap of a failed disk (meaning it cannot be replaced while the server keeps running). Ideally a hardware controller is used.

Ideal use

RAID-1 is ideal for mission critical storage, for instance for accounting systems. It is also suitable for small servers in which only two disks will be used.

RAID level 3

On RAID 3 systems, data blocks are subdivided (striped) and written in parallel on two or more drives. An additional drive stores parity information. You need at least 3 disks for a RAID 3 array.

Since parity is used, a RAID 3 stripe set can withstand a single disk failure without losing data or access to data.

Advantages

- RAID-3 provides high throughput (both read and write) for large data transfers.
- Disk failures do not significantly slow down throughput.

Disadvantages

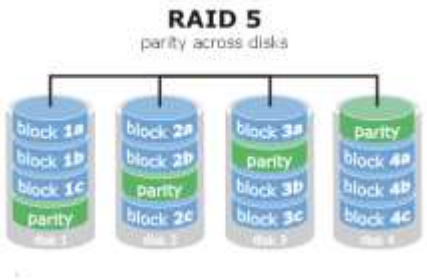
- This technology is fairly complex and too resource intensive to be done in software.
- Performance is slower for random, small I/O operations.

Ideal use

RAID 3 is not that common in prepress.

RAID level 5

RAID 5 is the most common secure RAID level. It is similar to RAID-3 except that data are transferred to disks by independent read and write operations (not in parallel). The data chunks that are written are also larger. Instead of a dedicated parity disk, parity information is spread across all the drives. You need at least 3 disks for a RAID 5 array. A RAID 5 array can withstand a single disk failure without losing data or access to data. Although RAID 5 can be achieved in software, a hardware controller is recommended. Often extra cache memory is used on these controllers to improve the write performance.



Advantages

Read data transactions are very fast while write data transaction are somewhat slower (due to the parity that has to be calculated).

Disadvantages

- Disk failures have an effect on throughput, although this is still acceptable.
- Like RAID 3, this is complex technology.

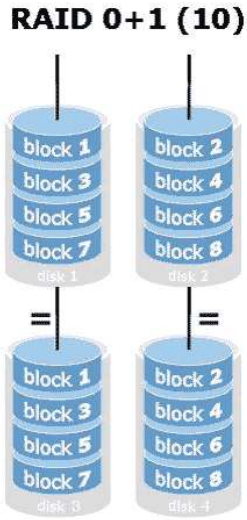
Ideal use

RAID 5 is a good all-round system that combines efficient storage with excellent security and decent performance. It is ideal for file and application servers.

RAID level 10 – Combining RAID 0 & RAID 1

RAID 10 combines the advantages (and disadvantages) of RAID 0 and RAID 1 in one single system. It provides security by mirroring all data on a secondary set of disks (disk

3 and 4 in the drawing below) while using striping across each set of disks to speed up data transfers.



What about RAID levels 2, 4, 6 and 7?

These levels do exist but are not that common, at least not in prepress environments. This is just a simple introduction to RAID-system. You can find more in-depth information on the pages of **wikipedia** or **ACNC**.

RAID is no substitute for back-up!

All RAID levels except RAID 0 offer protection from a single drive failure. A RAID 6 system even survives 2 disks dying simultaneously. For complete security you do still need to back-up the data from a RAID system.

- That back-up will come in handy if all drives fail simultaneously because of a power spike.
- It is a safeguard if the storage system gets stolen.
- Back-ups can be kept off-site at a different location. This can come in handy if a natural disaster or fire destroys your workplace.
- The most important reason to back-up multiple generations of data is user error. If someone accidentally deletes some important data and this goes unnoticed for several hours, days or weeks, a good set of back-ups ensure you can still retrieve those files.

a) What is Direct Memory Access(DMA)?Explain the reason for choosing DMA.Also discuss the Data Transfer
using DMA.

Direct Memory Access (DMA):

Direct Memory Access is a technique which allows a peripheral to read from and/or write to memory without intervention by the CPU. It is a simple form of bus mastering where the I/O device is set up by the CPU to transfer one or more contiguous blocks of memory. After the transfer is complete, the I/O device gives control back to the CPU.
The following DMA transfer combinations are possible:

□□Memory to memory
• Memory to peripheral
• Peripheral to memory
• Peripheral to peripheral
•

Reason for DMA:
The instruction **load [2], [9]** is illegal. The symbols [2] and [9] represent memory locations. This transfer has to be done in two steps:
• **load r1,[9]**
• **store r1,bx**

Thus, it is not possible to transfer from one memory location to another without involving the CPU. The same applies to transfer between memory and peripherals connected to I/O ports. e.g., we cannot have **out [6], datap.** It has to be done in two steps:
• **load r1,[6]**
• **out r1, datap**

Similar comments apply to the **in** instruction.
Thus, the real cause of the limited transfer rate is the CPU itself. It acts as an unnecessary "middleman". The above discussion also implies that, in general, every data word travels over the system bus twice.

Question No: 37 (Marks: 3)
What do you know about EEPROM? Discuss briefly.
EEPROM
EEPROM stands for Electrically Erasable Programmable Read-only Memory. This is a read-mostly memory that can be written into at any time without erasing prior contents; only the byte or bytes addr essed are updated. The write op eration takes considerably longer than the read operation. It is more expensive than EPROM.

Read Only Memory (ROM)
ROM is the read-only memory which contains permanent pattern of data that cannot be changed. ROM is nonvolatile i.e. it retains th e information in it when power is removed from it. Different types of ROMs are discussed below.

PROM
he PROM stands for Programmable Read only Memory. It is also nonvolatile and may be written into only once. For PROM, the writ ing process is performed electrically in the field. PROMs provide flexib ility and convenience.
EPROM
Erasable Programmable Read-only Memory or EPROM chips have quartz windows and by applying ultraviolet light erase the data can be erased from the EPROM. Data can be restored in an EPROM after erasure. EPRO Ms are more expensive than PROMs and are generally used for prototyping or sm all-quantity, special purpose work.
Flash Memory

An entire flash memory can be erased in one or a few seconds, which is much faster than
EPROM. In addition, it is possibl e to erase just blocks of memory rather than an entire chip.
Cache
Cache by definition is a place for safe storage and provides the fastest possible storage after the registers. The cache contains a c opy of portions of the main memory. When the CPU attempts to read a word from memory, a check is made to determine if the word is in the cache. If so, the word is delivered to the CPU. If not, a block of the main memory, consisting of some fixed number of words, is read into the cache and then the word is delivered to the CPU.

Question No: 38 (Marks: 5)
Discuss the two main issues in error control
Answer:
NOT FOUND

Question No: 39 (Marks: 5)
How are shift instructions useful? When do we use them?
Answer: SHIFT instructions move a bit string (or operand treated as a bit string) to the right or left, with excess bits discarded (although one or more bits might be preserved in flags). SHIFT instructions are useful in many ways. e.g., if you multiply two 16 bit numbers the result will be of 32 bit number, so shift is used to adjust the result in the two 16 bit registers. Also, as to multiply or divide by 2, SHIFT Left or SHIFT Right instructions are used.

Question No: 40 (Marks: 10)
Assume a network with a bandwidth of 2000Mbits/sec. It has a sending overhead of 100µsec and a receiving overhead of 150µsec. Assume two machines connected together. It is required to send a 20,000 byte message from one machine to the other (including header), and the message format allows 15, 00 bytes in a single message. Calculate the total latency to send the message from one machine to another assuming they are 20m apart (as in a SAN). Next, perform the same calculation but assume the machines are 800m apart (as in a LAN). Finally, assume they are 2000Km apart (as in a WAN). Assume that signals propagate at 66% of the speed of light in a conductor, and that the speed of light is 300,000Km/sec.

Question No: 41 (Marks: 10)
What is an address decoder? Draw the block diagram of an address decoder.
What steps do you suggest for an address decoder design?

==========

Set-13

The _____RTN describes the overall effect of instructions on the programmer visible registers.

Abstract
Concrete
Absolute Basic

Question No: 2

The instruction set is of _____importance in governing the structure and function of the pipeline.

Least Primary
Secondary No

Question No: 3

_____is the most general and least useful performance metrics for RISC machines.

MIPS
Instruction Count
Number of registers
Clock Speed

Question No: 4

A _____provides four functions: Select, DataIn, DataOut and Read/Write.

ALU Bus
Register
Memory Cell

Question No: 5

We can classify or partition the SRC instructions by their overall _behavior.

Register transfer
Memory transfer
Execution
Logical

Question No: 6

The _____RTN describes detailed register transfer steps in the data path that produce
the overall effect.

Abstract
Concrete
Absolute Basic

All members of the MC68000 family are __processors. 32-bit
16-bit
64-bit
8-bit

Question No: 8

_____Operations refers to a processor that can issue more than one instruction

simultaneously.

Macro Micro
Scalar
Superscalar

Question No: 9

Exceptions which are _occur in response to events that are paced by the internal processor clock.

Asynchronous
Synchronous Internal
External

Question No: 10

In the hazard detection by hardware, resolved by pipeline stalls, if the instructions are in the
adjoining stages, then the hazard must be detected in stage _____.

4
2
3
1

Question No: 11

16k x4 static RAM Chip is arranged in the form of four _____cells.

16x512
32x512
256x512
64x256

Question No: 12

In a DRAM cell, the storage capacitor will discharge in around ____

4 -15 ms
2 - 10 ms 5-20 ms 10-25 ms

1-bit sign, 8-bit exponent, 23-bit fraction and a bias of 127 is used for __Binary Floating Point Representation

- Double precision Single Precision
- All of above

Half Precision

In Single-Precision Binary Floating Point Representation , the exponent is _____

8 bit
11 bit
1 bit
23 bit

The 32 floating-point registers can hold 32 single-precision (32 bits), 16 double-precision (64 bits), or 8 extended-precision (128 bits) floating- point numbers

Question No: 1

The average rotational latency if the disk rotated at 20,000rpm is

0.5 ms
3.5 ms
2.5 ms
1.5 ms

Question No: 14

A hard disk with 5 platters has 1024 tracks per platter, 512 sectors per track and 512
bytes/sector. What is the total capacity of the disk?

1.5 GB
1 GB
2 GB
3 GB

Question No: 15

The CPU includes three types of instructions, which have different operands and will need
different representations. Which one of the instructions requires two source registers?

Jump and branch format
instructions Immediate format
instructions Register format
instructions
All of the above

Question No: 16

In this figure, the constant value specified by the immediate field is added to the register value,
and the resultant is the index of memory location that is referred i.e.
Effective Address = A + (content of R).
Identify the addressing mode.

Displacement
Immediate Indexed
Relative

is the actual data to be used.

Direct Indirect
Immediate
Relative

Question No: 18

Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A
and source register B) from the following example. **ADD R1, R2, R3**

Opcode= R1, DR=ADD, SA=R2, SB=R3
Opcode= ADD, DR=R1, SA=R2, SB=R3
Opcode= R2, DR=ADD, SA=R1, SB=R3
Opcode= ADD, DR=R3, SA=R2, SB=R1

Question No: 19

When the address of the subroutine is already known to the Microprocessor then it is called as -

-------- interrupt.

Maskable
Non-maskable Non-vectored Vectored

Question No: 20

The interrupts which are pre-programmed and the processor automatically finds the address of the ISR using interrupt vector table are

Maskable
Non-maskable Non-vectored Vectored

Question No: 21

Which is the last instruction of the ISR that is to be executed when the ISR TERMINATES?

IRET IRQ
INT NMI

Question No: 22

When the "**Divide error interrupts**" is generated

When an attempt is made to divide by decimal number

- When an attempt is made to multiply by zero
- When an attempt is made to divide by zero
- When negative number is stored in a register

Identify the following type of serial communication error condition:

"The prior character that was received was not still read by the CPU and is over written by a new received character."

Framing error Parity error Overrun error
Under-run error

Question No: 24

Which one of the following is a term used to describe a **storage systems'** resilience to disk failure through the use of multiple disks and by the use of data distribution and correction techniques

Interrupt handling
Programmed I/O Polling
RAID

Question No: 25

_____is the time for first bit of the message to arrive at the receiver including delays.

Transmission Time
Latency
Transport Latency

Time of Flight

Question No: 26

For a request of data if the requested data is not present in the cache, it is called a _____

Cache Miss Spatial
Locality Temporal
Locality Cache Hit

Question No: 27

An entire
EPROM.

memory can be erased in one or a few seconds which is much faster than

PROM Cache
EEPROM
Flash Memory

Question No: 28

A combination of parallel and sequential hardware used to build a multiplier is known as

_____

Parallel Array Multiplier
Booth Recording
Series Parallel Multiplier
None of the given

The _____of an m digit number x is xc'=bm -1- x

Radix Compliment
Diminished Radix Compliment
Signed Magnitude Form
Biased Representation

Question No: 30

Along with information bits we add up another bit which is called the bit.

CRC Hamming
Error Detection
Parity

Question No: 31

Falcon-A Simulator loads a FALCON-A binary file with a contents into different areas of the simulator.

.bin
.binfa
.fa
None of the given

extension and presents its

Question No: 32

In machines where instructions can be executed in parallel or out of order, two additional
hazards can occur: WAW and ----------
None fo the given WAR
RAW RAR

Question No: 33

---------- is the memory address of an interrupt handler.
Interrupt vector Interrupt
service routine Exception
Mask

Question No: 34

Why DMA is faster than Programmer I/O technique
DMA transfers data directly using CPU.
DMA transfers data directly without using CPU
DMA uses buffers with CPU
DMA uses interrupted driven I/O
None of the given
Correction
Detection
Both Correction and Detection

Question No: 36

In ____recording, bits are encoded in pairs so there are only ' n/2' additions instead of 'n'.
Booth Recording Bit Pair
Recording Integer
division None of the
given

Question No: 37

_____are computed by the ALU and stored in processor status register.
Condition codes
Conditional Branches
Fraction Division None of
the given

Question No: 38

In floating point representations
Sign Base Significant Exponent

is also called mantissa.

Question No: 39

Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)
Framing error
Parity error Overrun
error Under-run error

Question No: 40

What should be the behavior of interrupts during critical sections?

- Must remain Disable
- Must remain Enable
- Can be either enable or disable
- Only important interrupts be enable.

The _____signal coming from the CPU tells the memory that some interaction is required between the CPU and memory.

- R/W COMPLETE
- None of the given
- REQUEST

Question No: 42

_____is the simplest form for representing a signed number

- Sign Magnitude Form None
- of the given Biased
- Representation
- Diminished Radix Compliment Form

Question No: 43

Which of the instruction is used to load register from memory using a relative address?

- ld instruction ldr
- instruction lar
- instruction str
- instruction

Question No: 44

_____is/are defined as the number of instructions processed per second

- Throughput
- Latency
- Throughput and Latency
- None of the given

Given a 16-bit parallel output port attached with the FALCON-A CPU as shown in the figure below. The port is mapped onto address C9h of the FALCON-A's I/O space. Sixteen LED branches are
used to display the data being received from the FALCON-A's data bus. Every LED branch is wired in such a way that when a 1 appears on the particular data bus bit, it turns the LED on; a 0 turns it off.

a) Which LEDs will be ON when the instruction out r5, 201 executes on the CPU Assume r5
contains BC69h. Briefly explain your answer.

b) Identify the changes needed to map the above output port at address ABh and ACh of the
FALCON-A's I/Ospace (instead of C9h and CAh)

Question No: 46

Give control signals for the **addi** instructions.

Note: Fill the given table only. If you require other control signals to complete the table, do it as rough work. Marks will be given only for the required fields in the table.

Address	PC out	Cout	MBRout	R2Bus	LMAR	LC	LPC	LIR	LA	Bus2R	INC4	Read	LMBR	MARout	ADD	RAE	RBE	RCE	END	c2out
100	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0
101	0	1	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	0	0	0
102	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
203	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0
204	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	1
205	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0

Explain the complications related to pipelining

Question No: 48

Write the parameters and the classification of networks.

Question No: 49

Perform multiplication by bit- pair recording.

-7 x -6

Question No: 50

Consider a hard disk that rotates at 4000 rpm. The seek time to move the head between adjacent tracks is 2 ms. There are 64sectors per track stored in linear order. Assume that the read/write head is initially at the start of sector 1 on track 7.

a) How long will it take to transfer sector 1 on track 6 to sector 1 on track 9

b) How long will it take to transfer all the sectors on track 11 to corresponding sectors on track 13?

Answer:

NOT FOUND

Question No: 51

a) What should be the polling frequency for an I/O device if the average delays between the time when the device wants to make a request and the time when it is polled, is to be at most 12 ms

b) If it takes 15,000 cycles to poll the I/O device, and the processor operates at 200MHz, what % of the CPU time is spent polling

c) What should be the polling frequency if the system wants to provide an average delay of msec

Question No: 52

Assume that three I/O devices are connected to a 32-bit, 10 MIPS CPU. The first device is a hard

drive with a maximum transfer rate of 2MB/sec. It has a 32-bit bus. The second device is a floppy drive with a transfer rate of 30KB/sec over a 16-bit bus, and the third device is a keyboard that must be polled thirty five times per second. Assuming that the polling operation requires 15 instructions for each I/O device, determine the percentage of CPU time required to poll each device.

Idea Answer:
Example # 1
23
Assume that three I/O devices are connected to a 32-bit, 10 MIPS CP U. The first device is a hard drive with a maximum transfer rate of 1MB/sec. It has a 32-bit bus. The second
device is a floppy drive with a transfer rate of 25KB/sec over a 16-bit bus, and the third device is a keyboard that must be polled thirty times per second. Assuming that the polling operation requires 20 instructions for each I/O device, determine the percentage of CPU time required to poll each device.
Solution:
The hard drive can transfer 1MB/sec or 250 K 32-bit words every second. Thus, this hard
drive should be polled using at least this rate.
Using $1K=2^{10}$,
the number of CPU instructions required would be
250×2^{10}
x 20 = 5120000 instructions per second.
Percentage of CPU time required for polling is
(5.12 x 10
6
)/ (10 x10
6
) = 51.2%
The floppy disk can transfer 25K/2= 12.5 x 2
10
half-words per second. It should be
polled with at least this rate. The number of CPU instructions required will be 12.5 x 2
10
x 20 = 256,000 instructions per second.
Therefore, the percentage of CPU time required for polling is
(0.256 x 10
6
)/ (10 x 10
6
) = 2.56%.
For the keyboard, the number of inst ructions required for polling is
30 x 20 = 600 instructions per second.
Therefore, the percentage of CPU time spent in polling is
600 / (10 x 10
6
) = 0.006%
See Page 309

Question No: 53

Write different schemes related to virtual memory organization.

Question No: 54

Suppose we have 10 magnetic tapes, each containing 20GB. Assume that there are enough tape
readers to keep any network busy. How long will it take to transmit the data over a distance of 3Km The choices are category 5 twisted-pair wires at 100Mbits/sec, multimode fiber at 1500Mbits/sec and single- mode fiber at 3000Mbits/sec.

Question No: 55

Explain all categories in classification of hazards.

Convert the following decimal numbers to IEEE single precision floating- point numbers. Report the results as hexadecimal values. You need not extend the calculations of the significant value beyond its most significant 8 bit. **-0.5625**

Question No: 57

What are the approaches used to design a Control unit briefly compare them. [5]

Question No: 58

Evaluate the instruction z = 16(a -b) + 32(c+58) with the 3 address machine.[5]

Question No: 59

What is the difference between "branch" and "branch link" instructions of SRC [5]

Question No: 60

A hard disk with 5 platters has 1024 tracks per platter, 512 sectors per track and 512
bytes/sector.

a) What is the total capacity of the disk?
b) How many platters are required for an 80GB disk if there are 1024 bytes/sector, 2048 sectors per track and 4096 tracks per platter?

Question No: 61

Consider a memory system having the following specifications. Find its total cost and cost per byte of memory.

Memory type	Total bytes	Cost per byte
SRA	512	50$ per MB
DRA	256	2$ per MB
Dis	3	10$ per GB

Question No: 62

Give comparison of advantages and disadvantages of serial and parallel transfer of data
between the CPU and an I/O device.

Question No: 63

What are different I/O techniques briefly describe the comparison of Interrupt driven I/O and
Polling.

Question No: 64

Define an I/O port. Which functions are performed by it?

Question No: 65

Assume a network with a bandwidth of 2500Mbits/sec. It has a sending overhead of 200ìsec and a receiving overhead of 160ìsec. Assume two machines connected together. It is required to send a 15,000 byte message from one machine to the other (including header), and the message format allows 15, 00 bytes in a single message. Calculate the total latency to send the message from one machine to another assuming they are 25m

apart (as in a SAN). Next, perform the same calculation but assume the machines are 750m apart (as in a LAN).Finally, assume they are 1500Km apart (as in a WAN). Assume that signals propagate at 1/3 of the speed of light in a conductor, and that the speed of light is 300,000Km/sec.
Answer:

Question No: 67

Consider a hard disk that rotates at 6000 rpm. The seek time to move the head between
adjacent tracks is 1 ms. There are 64 sectors per track stored in linear order. Assume that the read/write head is initially at the start of sector 1 on track 7.

a) How long will it take to transfer sector 1 on track 7 to sector 1 on track 9
b) How long will it take to transfer all the sectors on track 12 to corresponding sectors on track 13

Answer : See axample at Page Number 324

Example 5

Consider a hard disk that rotates at 3000 rpm. The seek time to move the head between adjacent tracks is 1 ms. There are 64sectors per track stored in linear order.
Assume that the read/write head is initially at the start of sector 1 on track 7.
a. How long will it take to transfer sector 1 on track 7 to sector 1 on track 9?
b. How long will it take to transfer all the sectors on track 12 to corresponding sectors on track 13?

Solution

Time for one revolution=60/3000=20ms

a. Total transfer time=sector read time+head movement time+rotational delay+sector write time
Time to read or write on sector=20/64=0.31ms/sector
Head movement time from track 7 to track 9=1msx2=2ms
After reading sector 1 on track 7, which takes .31ms, an additional 19.7 ms of rotational delay is needed for the head to line up with sector 1 again.
The head movement time of 2 ms gets included in the19.7 ms. Total transfer time=0.31ms+19.7ms+0.31ms=20.3ms

b. The time to transfer all the sectors of track 12 to track 13 can be computed in the
similar way. Assume that the memory buffer can hold an entire track. So the time to read or write an entire track is simply the rotational delay for a track, which is 20 ms. The head movement time is 1ms, which is also the time for 1/0.3=3.3≈ 4 sectors to pass under the head. Thus after reading a track and repositioning the head, it is now on track 13, at four sectors past the initial sector that was read on track 12. (Assuming track 13 is written starting at sector 5)
therefore total transfer time= 20+1+20=41ms.
If writing of track 13 start at the first sector, an additional 19 ms should be added, giving a total transfer time= 60 ms

Question No: 68

a) Drawing a timing diagram, briefly explain the sequence of steps that take place during a
synchronous transfer between a master device and a slave device.
b) List one advantage and one disadvantage of DMA

Question No: 69

Consider a DRAM with 2048 rows and a refresh time of 20ms.
a) Find the frequency of row refresh operations.
b) What fraction of the DRAM's time is spent on refreshing if each refresh takes 100ns?

Question No: 70

Find the bandwidth of a memory system that has a latency of 30ns, a pre charge time of 10ns and transfers 3 bytes of data per access.

Question No: 71

Write the code to implement the following expressions on 3, 2, 1, and 0 address machines.

A= B + C x D

Question No: 72

A magnetic disk has an average seek time of 8 ms. The transfer rate is 50 MB/sec. The disk rotates at 10,000 rpm and the controller overhead is 0.3 msec. Find the average time to read or write
1024 bytes.

Question No: 73

a) Briefly describe the following errors with respect to serial communication.
Frame error
- Parity
- Overrun

b) List down the advantages of Virtual Memory
How many bits are included in one 1KByte

Question No: 75

In which type of interrupts, the address of the service routine needs to be supplied externally by the device

Question No: 76

What do you know about **PROM** Explain Briefly?

Question No: 77

Share your knowledge of interrupt vector in simple and precise paragraph.

Question No: 78

What is a non-maskable interrupt (NMI) and what is its role

Question No: 79

Highlight the similarity and difference between RAID level 3 and RAID level 4.

Question No: 80

What do you know about **EEPROM** Discuss briefly?

Question No: 81

Discuss the two main issues in error control

Question No: 82

How are shift instructions useful When do we use them

Question No: 83

Assume a network with a bandwidth of 2000Mbits/sec. It has a sending overhead of 100µ secand a receiving overhead of 150µ sec. Assume two machines connected together. It is required to send a 20,000 byte message from one machine to the other (including header), and the message format allows 15, 00 bytes in a single message. Calculate the total latency to send the message from one machine to another assuming they are 20m apart (as in a SAN). Next, perform the same calculation but assume the machines are 800m apart (as in a LAN). Finally, assume they are 2000Km apart (as in a WAN). Assume that signals propagate at 66% of the speed of light in a conductor, and that the speed of light is
300,000Km/sec.

Question No: 84

What is an address decoder Draw the block diagram of an address decoder? What steps do you suggest for an address decoder design?

==========

Set-14

Question:

Answer:

==========

Set-15

Question:

Answer:

==========

Set-16

BY

($$)

FINALTERM EXAMINATION

Fall 2008

CS501- Advance Computer Architecture (Session - 1)

Marks: 75

Question No: 1 (Marks: 1) - Please choose one

Which one of the following is the memory organization of **SRC processor?**

- 28 * 8 bits
- 2^{16} * 8 bits

2^{32} * 8 bits

- 2^{64} * 8 bits

Question No: 2 (Marks: 1) - Please choose one

Type A format of SRC uses ----------instructions

two

- three
- four
- five

Question No: 3 (Marks: 1) - Please choose one

The instruction ----------will **load** the register R3 with the contents of the memory location M [PC+56]

- Add R3, 56
- lar R3, 56

ldr R3, 56

- str R3, 56

Question No: 4 (Marks: 1) - Please choose one

Which format of the instruction is called the accumulator?

- 3-address instructions
- 3-address instructions
- 2-address instructions

1-address instructions

- 0-address instructions

Question No: 5 (Marks: 1) - Please choose one

Which one of the following are the **code size** and the **Number of memory bytes** respectively for a 2-address instruction?

- 4 bytes, 7 bytes

7 bytes, 16 bytes

- 10 bytes, 19 bytes
- 13 bytes, 22 bytes

Question No: 6 (Marks: 1) - Please choose one

Which operator is used to name registers, or part of registers, in the Register Transfer Language?

:=

- &
- %
- ©

Question No: 7 (Marks: 1) - Please choose one

The transmission of data in which each character is self-contained units with itsown start and stop bits is ----------

- Asynchronous
- Synchronous

- Parallel
- All of the given options

Question No: 8 (Marks: 1) - Please choose one

Circuitry that is used to move data is called ----------

Bus

- Port
- Disk
- Memory

Question No: 9 (Marks: 1) - Please choose one

Which one of the following is **NOT** a technique used when the CPU wants to exchange data with a peripheral device?

- Direct Memory Access (DMA).
- Interrupt driven I/O
- Programmed I/O

Virtual Memory

Question No: 10 (Marks: 1) - Please choose one

Every time you press a key, an interrupt is generated.

This is an example of

Hardware interrupt

- Software interrupt
- Exception
- All of the given

Question No: 11 (Marks: 1) - Please choose one

The interrupts which are pre-programmed and the processor automatically finds the address of the ISR using interrupt vector table are

- Maskable
- Non-maskable
- Non-vectored

Vectored

Question No: 12 (Marks: 1) - Please choose one

Which is the last instruction of the ISR that is to be executed when the ISR terminates?

IRET

- IRQ
- INT
- NMI

Question No: 13 (Marks: 1) - Please choose one

If NMI and INTR both interrupts occur simultaneously, then which one has the precedence over the other

NMI

- INTR
- IRET
- All of the given

Question No: 14 (Marks: 1) - Please choose one

Identify the following type of serial communication error condition:

The prior character that was received was not still read by the CPU and is over written by a new received character.

- Framing error
- Parity error
- **Overrun error Page 242**
- Under-run error

Question No: 15 (Marks: 1) - Please choose one

----------the device usually means reading its status register every so often untilthe device's status changes to indicate that it has completed the request.

- Executing
- Interrupting
- Masking

Polling

The process of periodically checking the status of a device to see if it is ready for the next I/O operation is called "polling". Page 270

Question No: 16 (Marks: 1) - Please choose one

Which I/O technique will be used by a sound card that may need to access datastored in the computer's RAM?

Programmed I/O

- Interrupt driven I/O
- Direct memory access(DMA)
- Polling

Question No: 17 (Marks: 1) - Please choose one

For increased and better performance we use _____ which are usually made of glass.

- Coaxial Cables
- Twisted Pair Cables

Fiber Optic Cables

- Shielded Twisted Pair Cables

Question No: 18 (Marks: 1) - Please choose one

In _____ if we find some call party busy we can have provision of call waiting.

Delay System Page 368

- Loss System
- Single Server Model
- None of the given

Question No: 19 (Marks: 1) - Please choose one

In ____ technique memory is divided into segments of variable sizes depending upon the requirements.

- Paging

Segmentation

- Fragmentation
- None of the given

Question No: 20 (Marks: 1) - Please choose one

For a request of data if the requested data is not present in the cache, it is called a _____

Cache Miss Page 349

- Spatial Locality
- Temporal Locality
- Cache Hit

Question No: 21 (Marks: 1) - Please choose one

An entire _____ memory can be erased in one or a few seconds which is much faster than EPROM.

- PROM
- Cache
- EEPROM

Flash Memory

Question No: 22 (Marks: 1) - Please choose one

_____chips have quartz windows and by applying ultraviolet light data can be erased from them.

- PROM
- Flash Memory

EPROM Page 348

- EEPROM

Question No: 23 (Marks: 1) - Please choose one

The _____signal coming from the CPU tells the memory that some interaction is required between the CPU and memory.

REQUEST page 344

- COMPLETE

None of the given

In this cas e, the REQUEST signal coming from the CPU telling the memory that some interaction is required between the CPU and memory. As a result of this request (either read/write), along with the signal on the control and the address on the address bus, we might have the corresponding data on the data bus for a read operation and after the operation is complete, the memory would issue a control signal which corresponds in this case to COMPLETE.

Question No: 24 (Marks: 1) - Please choose one

_____ is a combination of arithmetic, logic and shifter unit along with some multiplexers and control unit.

- Barrel Rotator
- Control Unit
- Flip Flop

ALU Page 341

Question No: 25 (Marks: 1) - Please choose one

1. In Multiple Interrupt Line, a number of interrupt lines are provided between the _____ module.

CPU and the I/O Page 283

- CPU and Memory
- Memory and I/O
- None of the given

Question No: 26 (Marks: 1) - Please choose one

The data movement instructions _____ data within the machine and to or from input/output devices.

- Store
- Load
- Move
- None of given

Question No: 27 (Marks: 1) - Please choose one

CRC has ---------- overhead as compared to Hamming code.

Equal

- Greater
- Lesser
- None of the given

Question No: 28 (Marks: 1) - Please choose one

The _____ is w-bit wide and contains a data word, directly connected to the data bus which is b-bit wide memory address register (MAR) .

- Instruction Register(IR)
- memory address register (MAR)

memory Buffer Register(MBR) Page 344

- Program counter (PC)

The memory address register (MAR) is m- bits wide and contains memory address generated by the CPU directly connected to the m-bit wide address bus. The memory buffer register (MBR) is w-bit wide and contains a data word, directly connected to the data bus which is b-bit wide.

Question No: 29 (Marks: 1) - Please choose one

In_____technique, a particular block of data from main memory can be placed in only one location into the cache memory .

- Set Associative Mapping

Direct Mapping page 350

- Associative Mapping
- Block Placement

Question No: 30 (Marks: 1) - Please choose one

_____ indicate the availability of page in main memory.

- Access Control Bits
- Used Bits

Presence Bits Page 356

- None of the given

Control Field: This includes the following bits.

- Access control bits: These bits are used to specify read/write, and execute permissions.
- Presence bits: Indicates the availabili ty of page in the main memory.
- Used bits: These bits are set upon a read/ write.

CS501-Advance Computer Architecture
Midterm Special 2006

_____all memory systems are dumb, in that they respond to only two commands: read or write
Virtually
Logically
Physically
None of These

Q 3
To access an operand in memory, the CPU must first generate an address, which it then issues to the _____
MEMORY
REGISTER
DATA BUS
ALL OF ABOVE
Q 4
_____ or Branch instructions affect the order in which instructions are performed, or control the flow of the program
Control
DATA MOVMENT
Arithmetic
LOGICAL
Q5
Reverse assemble the following SRC machine language instructions:
[10]
68C2003A h

Q6
An instruction that specifies one operand in memory and one operand in a register would be known as a _____ address instruction.
2-1/2
1-1/2
0
2
Q7
The data movement instructions _____ data within the machine and to or from input/output devices
Store
LOAD
MOVE
NONE OF ABOVE.
==========

Set-17

BY Memoona Latif

Question # 1 of 10 (Start time: 09:48:03 PM) Total Marks: 1
_____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.
Select correct option:
INC4
LPC
PCout
TRUE
LC

Question # 2 of 10 (Start time: 09:48:58 PM) Total Marks: 1
_____ enable the input to the PC for receiving a value that is currently on the internal processor bus.
Select correct option:
LPC
TRUE
BY

INC4
LC
Cout

Question # 3 of 10 (Start time: 09:49:44 PM) Total Marks: 1
Which one of the following registers stores a previously calculated value or a value loaded from the main memory?
Select correct option:
Accumulator
Address Mask
Instruction Register
Program Counter
TRUE

Question # 4 of 10 (Start time: 09:50:20 PM) Total Marks: 1
Which one of the following registers holds the instruction that is being executed?
Select correct option:
Accumulator
Address Mask
Instruction Register
TRUE
Program Counter

Question # 5 of 10 (Start time: 09:51:19 PM) Total Marks: 1
For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required; which may
be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate

memory location.
Select correct option:
Registers
BY

Control signals
TRUE
Memory
None of the given

Question # 7 of 10 (Start time: 09:52:34 PM) Total Marks: 1
Which one of the following registers holds the address of the next instruction to be executed?
Select correct option:
Accumulator
Address Mask
Instruction Register
Program Counter
TRUE

Question # 8 of 10 (Start time: 09:53:14 PM) Total Marks: 1
The external interface of FALCON-A consists of a _____address bus and a _____ data bus.
Select correct option:
8-bit , 8-bit
16-bit , 16-bit
TRUE
16-bit , 24-bit
16-bit , 32-bit

Question # 9 of 10 (Start time: 09:54:31 PM) Total Marks: 1
Which one of the following register(s) that is/are programmer invisible and is/are required to hold an operand or result value
while the bus is busy transmitting some other value?
Select correct option:
Instruction Register
Memory address register
Memory Buffer Register
Registers A and C
TRUE

==========

Set-18

Question:

Answer:

==========

Final Multiple Choice Question

Set-01 (Mid-Term)

Question # 1 of 10 (Start time: 10:48:22 PM) Total Marks: 1
Keyboard Interrupt (INT 9) is an example of ----- interrupt.
Select correct option:

Hardware
TRUE
Software

Question # 2 of 10 (Start time: 10:49:48 PM) Total Marks: 1
Shifting of the radix point towards left or right is called _____
Select correct option:
Shifting
Logical Shift
Right Shift
Scaling
TRUE

Question # 3 of 10 (Start time: 10:50:27 PM) Total Marks: 1
For _____ of an error we just need to know that there exists an error.
Select correct option:
Detection
TRUE
Correction
Both Correction and Detection
None of the given

Question # 4 of 10 (Start time: 10:51:00 PM) Total Marks: 1
A user program has to delete a file. The user program will be executing in the user mode. When it makes the specific system
call to delete the file, an interrupt will be generated, this will cause the processor to halt its current activity and switch to
supervisor mode. Once in supervisor mode, the operating system will delete the file and then control will return to the user
program. This is an example of
Select correct option:
Hardware interrupt
Software interrupt
TRUE
Exception
All of the given

Question # 5 of 10 (Start time: 10:52:14 PM) Total Marks: 1
By which file extension does the FALCON-A Assembler loads a FALCON-A assembly file?
Select correct option:
.asmfa
TRUE

.org
.exe
.src

Question # 6 of 10 (Start time: 10:53:17 PM) Total Marks: 1
All ----------interrupts have priority over all ---------interrupts
Select correct option:
internal, external
TRUE
external,internal

Question # 7 of 10 (Start time: 10:53:41 PM) Total Marks: 1
Given an m-digit base b number x, the _____ of x is xc = (bm– x) mod bm
Select correct option:
Radix Compliment
TRUE
Diminished Radix Compliment
Signed Magnitude Form
Biased Representation

Question # 8 of 10 (Start time: 10:54:45 PM) Total Marks: 1
The ------- can also be used anywhere in the source file to force code at a particular address in the memory.
Select correct option:
.end directive
.start directive
.label directive
.org directive
TRUE

Question # 9 of 10 (Start time: 10:55:11 PM) Total Marks: 1
Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?
Select correct option:
Daisy-Chaining Priority
Asynchronous Priority
Parallel Priority
TRUE
Semi-synchronous Priority

Question # 10 of 10 (Start time: 10:56:26 PM) Total Marks: 1
An ---------- is the memory address of an interrupt handler.
Select correct option:
Interrupt vector
TRUE
Interrupt service routine
Exception
Mask

==========

Set-04

Question # 1 of 10 (Start time: 08:43:45 PM) Total Marks: 1
When the address of the subroutine is already known to the Microprocessor then it is called as ---------
interrupt.
Select correct option:
Maskable
Non-maskable
Non-vectored
Vectored

Question # 2 of 10 (Start time: 08:45:10 PM) Total Marks: 1
Identify the following type of serial communication error condition in which no character is available at
the beginning of an interval.
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

Question # 3 of 10 (Start time: 08:46:26 PM) Total Marks: 1
_____ is the simplest form for representing a signed number
Select correct option:
Biased Representation
Diminished Radix Compliment Form
Sign Magnitude Form
None of the given
Question # 4 of 10 (Start time: 08:47:21 PM) Total Marks: 1
How Interrupt driven I/O is better than polling because?
Select correct option:
Interrupt driver I/O is easy to design
Interrupt driver I/O is enhanced version of polling.
Interrupt driver I/O does not waste time on checking which device is available.
Interrupt driven I/O is easy to program.

Question # 5 of 10 (Start time: 08:48:50 PM) Total Marks: 1
---------- is the time needed by the CPU to recognize (not service) an interrupt request.
Select correct option:
Interrupt Latency
Response Deadline
Timer delay
Throughput

Question # 6 of 10 (Start time: 08:49:49 PM) Total Marks: 1
---------- allows a peripheral to read and write memory without intervention by the CPU.
Select correct option:

o Programmed I/O
o Interrupt driven I/O
o Direct memory access(DMA)
o Polling

Question # 7 of 10 (Start time: 08:51:03 PM) Total Marks: 1
Identify the type of serial communication error condition in which A 0 is received instead of a stop bit
(which is always a 1)?
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

Question # 8 of 10 (Start time: 08:52:04 PM) Total Marks: 1
Taking control of the system bus for a few bus cycles is known as _____.
Select correct option:
Bus Stealing
Cycle Stealing
Cycle Transfering

Question # 9 of 10 (Start time: 08:53:12 PM) Total Marks: 1
The main issue/s in error control is/are_____.
Select correct option:
Detection and correction of Error
Detection of Error
Correction of Error
Avoidance of Error

Question # 10 of 10 (Start time: 08:53:59 PM) Total Marks: 1
Along with information bits we add up another bit which is called the_____bit.
Select correct option:
CRC
Hamming
Error Detection
Parity
None of given

==========

Set-05

Quiz
What happens when the microprocessor is interrupted?
It suspends the currently executing program and jumps to (ISR) to respond to the incoming interrupt
It suspends the incoming interrupt and keeps executing current program.

It makes a queue for all such incoming interrupts so as to respond to them after system restart.
All of the given options

In which one of the following interrupts the device have to supply the address of the subroutine to the Microprocessor
Maskable
Non-maskable
Non-vectored
Vectored

If an interrupt is set by the timer component or by the peripheral device then how would you categorize it?
Hardware
Software
Exception
All of the given options

A user program has to delete a file. The user program will be executing in the user mode. When it makes the specific system call to delete the file, an interrupt will be generated, this will cause the processor to halt its current activity and switch to supervisor mode. Once in supervisor mode, the operating system will delete the file and then control will return to the user program.
This is an example of
Hardware interrupt
Software interrupt
Exception
All of the given

Every time you press a key, an interrupt is generated.
This is an example of
Hardware interrupt
Software interrupt
Exception
All of the given
An ---------- is the memory address of an interrupt handler.
Interrupt vector
Interrupt service routine
Exception
Mask

Which is the last instruction of the ISR that is to be executed when the ISR terminates?
IRET
IRQ

INT
NMI

When is the **"Divide error interrupt"** generated?
When an attempt is made to divide by decimal number
When an attempt is made to multiply by zero
When an attempt is made to divide by zero
When negative number is stored in a register

The interrupts in which we write the address of the interrupt service routine (ISR) in the interrupt instruction itself are
Maskable
Non-maskable
Non-vectored
Vectored

The interrupts which are pre-programmed and the processor automatically finds the address of the ISR using interrupt vector table are
Maskable
Non-maskable
Non-vectored
Vectored

==========

Set-06

Quiz Start Time: 11:10 AM Time Left 90
sec(s)
Question # 1 of 10 (Start time: 11:10:25 AM) Total Marks: 1
The external interface of FALCON-A consists of a _____address bus and a _____ data bus.
Select correct option:
8-bit , 8-bit
16-bit , 16-bit (p #167)
16-bit , 24-bit
16-bit , 32-bit
==========
Question # 2 of 10 (Start time: 11:11:41 AM) Total Marks: 1
_____ control signal enable the input to the PC for receiving a value that is currently on the internal processor bus.
Select correct option:
LPC (172)
INC4
LC
Cout
==========

Question # 3 of 10 (Start time: 11:12:54 AM) Total Marks: 1
Which one of the following is the memory organization of EAGLE processor?
Select correct option:
2^8 * 8 bits
2^16 * 8 bits (112)
2^32 * 8 bits
2^64 * 8 bits
==========
Question # 4 of 10 (Start time: 11:14:21 AM) Total Marks: 1
Motorola MC68000 is an example of ---------microprocessor.
Select correct option:
CISC (148)
RISC
SRC
FALCON
==========
Question # 5 of 10 (Start time: 11:15:13 AM) Total Marks: 1
Which one of the following registers stores a previously calculated value or a value loaded from the main memory?
Select correct option:
Accumulator
Address Mask
Instruction Register
Program Counter
==========
Question # 6 of 10 (Start time: 11:16:34 AM) Total Marks: 1
FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is _____ wide.
Select correct option:
8-bits
16-bits
32-bits (157)
64-bits
==========
Question # 7 of 10 (Start time: 11:17:12 AM) Total Marks: 1
What is the size of the memory space that is available to FALCON-A processor?
Select correct option:
2^8 bytes
2^16 bytes
2^32 bytes
2^64 bytes
==========
Question # 8 of 10 (Start time: 11:18:25 AM) Total Marks: 1
For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.
Select correct option:
Registers

Control signals (171)
Memory
None of the given
==========
Question # 9 of 10 (Start time: 11:19:30 AM) Total Marks: 1
What is the instruction length of the FALCON-E processor?
Select correct option:
8 bits
16 bits
32 bits
64 bits
==========
Question # 10 of 10 (Start time: 11:20:57 AM) Total Marks: 1
How can we refer to an instruction register (IR), of 16 bits (numbered 0 to 15) using RTL?
Select correct option:
IR<16..0>
IR<15..0> (105)
IR<16..1>
IR<15..1>
==========
Question # 1 of 10 (Start time: 11:26:02 AM) Total Marks: 1
Which one of the following is the memory organization of EAGLE processor?
Select correct option:
2^8 * 8 bits
2^16 * 8 bits
2^32 * 8 bits
2^64 * 8 bits
==========
Question # 2 of 10 (Start time: 11:27:13 AM) Total Marks: 1
"If P = 1, then load the contents of register R1 into register R2". This statement can be written in RTL as:
Select correct option:
R1 <- R2
P: R1 <- R2 NOT SURE
P: R2 <- R1
P: R2 <- R1, P: R1 <- R2
==========
Question # 3 of 10 (Start time: 11:28:38 AM) Total Marks: 1
What is the instruction length of the FALCON-A processor?
Select correct option:
8 bits
16 bits
32 bits
64 bits
==========
Question # 4 of 10 (Start time: 11:29:18 AM) Total Marks: 1
How can we refer to an instruction register (IR), of 16 bits (numbered 0 to 15) using RTL?

Select correct option:
IR<16..0>
IR<15..0>
IR<16..1>
IR<15..1>
==========
Question # 5 of 10 (Start time: 11:29:35 AM) Total Marks: 1
Which one of the following registers holds the address of the next instruction to be executed?
Select correct option:
Accumulator
Address Mask
Instruction Register
Program Counter (151)
==========
Question # 6 of 10 (Start time: 11:30:41 AM) Total Marks: 1
In----------address mode, the actual data is stored in the instruction.
Select correct option:
Direct
Indirect (not sure)
Immediate
Relative
==========
Question # 7 of 10 (Start time: 11:32:09 AM) Total Marks: 1
Which one of the following registers stores a previously calculated value or a value loaded from the main memory?
Select correct option:
Accumulator
Address Mask
Instruction Register (not sure)
Program Counter
==========
Question # 8 of 10 (Start time: 11:33:56 AM) Total Marks: 1
Which notation do we use to name different fields of a register in RTL?
Select correct option:
()
<-
+
:=
(CAN'T FIND THE ANSWER :( )
==========
Question # 10 of 10 (Start time: 11:35:34 AM) Total Marks: 1
What is the instruction length of the FALCON-E processor?
Select correct option:
8 bits
16 bits
32 bits
64 bits
==========

Question # 1 of 10 (Start time: 11:43:13 AM) Total Marks: 1
Which one of the following registers holds the address of the next instruction to be executed?
Select correct option:
Accumulator
Address Mask
Instruction Register
Program Counter (151)

EAGLE	FALCON-A	FALCON-E	SRC
Fixed 16 bits	Fixed 16 bits	Fixed 32 bits	Fixed 32 bits

==========
Question # 2 of 10 (Start time: 11:43:56 AM) Total Marks: 1
_____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.
Select correct option:
INC4
LPC
PCout (172)
LC
==========
Question # 3 of 10 (Start time: 11:44:41 AM) Total Marks: 1
What is the instruction length of the FALCON-E processor?
Select correct option:
8 bits
16 bits
32 bits
64 bits
==========
Question # 4 of 10 (Start time: 11:44:52 AM) Total Marks: 1
For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.
Select correct option:
Registers
Control signals (171)
Memory
None of the given
==========
Question # 5 of 10 (Start time: 11:45:47 AM) Total Marks: 1
What is the instruction length of the FALCON-A processor?
Select correct option:
8 bits
16 bits
32 bits

64 bits
==========
Question # 6 of 10 (Start time: 11:46:37 AM) Total Marks: 1
Which one of the following portions of an instruction represents the operation to be performed?
Select correct option:
Address
Instruction code
Opcode
Operand
==========
Question # 7 of 10 (Start time: 11:48:09 AM) Total Marks: 1
In----------address mode, the actual data is stored in the instruction.
Select correct option:
Direct
Indirect
Immediate
Relative
==========
Question # 8 of 10 (Start time: 11:49:05 AM) Total Marks: 1
The external interface of FALCON-A consists of a _____address bus and a _____ data bus.
Select correct option:
8-bit , 8-bit
16-bit , 16-bit (167)
16-bit , 24-bit
16-bit , 32-bit
==========
Question # 9 of 10 (Start time: 11:50:33 AM) Total Marks: 1
Which notation do we use to name different fields of a register in RTL?
Select correct option:
()
<-
+
:=
==========
Question # 10 of 10 (Start time: 11:50:42 AM) Total Marks: 1
How can we refer to an instruction register (IR), of 16 bits (numbered 0 to 15) using RTL?
Select correct option:
IR<16..0>
IR<15..0>
IR<16..1>
IR<15..1>

==========

Set-07

Question # 1 of 10 (Start time: 07:23:43 PM) Total Marks: 1

Which one of the following register(s) that is/are programmer invisible and is/are required to hold an operand or result value while the bus is busy transmitting some other value?
Select correct option:
Instruction Register
Memory address register
Memory Buffer Register
Registers A and C (P # 153)
Question # 2 of 10 (Start time: 07:25:00 PM) Total Marks: 1
For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.
Select correct option:
Registers
Control signals (P # 173)
Memory
None of the given
Question # 3 of 10 (Start time: 07:26:05 PM) Total Marks: 1
In which one of the following techniques, the time a processor spends waiting for instructions to be fetched from memory is minimized?
Select correct option:
Perfecting
Pipelining
Superscalar operation
Speedup
Question # 4 of 10 (Start time: 07:26:52 PM) Total Marks: 1
FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is _____ wide.
Select correct option:
8-bits
16-bits
32-bits (159)
64-bits
Question # 5 of 10 (Start time: 07:27:48 PM) Total Marks: 1
---------- performs the data operations as commanded by the program instructions.
Select correct option:
Control
Datapath
Structural RTL
Timing
Question # 6 of 10 (Start time: 07:28:47 PM) Total Marks: 1
The external interface of FALCON-A consists of a _____address bus and a _____ data bus.
Select correct option:
8-bit , 8-bit
16-bit , 16-bit (P # 169)
16-bit , 24-bit
16-bit , 32-bit

Question # 7 of 10 (Start time: 07:30:02 PM) Total Marks: 1
Which one of the following registers stores a previously calculated value or a value loaded from the main memory?
Select correct option:
Accumulator
Address Mask
Instruction Register
Program Counter
Question # 8 of 10 (Start time: 07:31:29 PM) Total Marks: 1
Computer system performance is usually measured by the ----------
Select correct option:
Time to execute a program or program mix
The speed with which it executes programs
Processor's utilization in solving the problems
Instructions that can be carried out simultaneously
Question # 9 of 10 (Start time: 07:31:54 PM) Total Marks: 1
Which one of the following registers holds the address of the next instruction to be executed?
Select correct option:
Accumulator
Address Mask
Instruction Register
Program Counter
Question # 10 of 10 (Start time: 07:33:26 PM) Total Marks: 1
_____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.
Select correct option:
INC4
LPC
PCout (P # 174)
LC
Question # 1 of 10 (Start time: 07:02:29 PM) Total Marks: 1
The external interface of FALCON-A consists of a _____ address bus.
Select correct option:
8-bit
16-bit
24-bit
32-bit
Question # 2 of 10 (Start time: 07:03:47 PM) Total Marks: 1
Computer system performance is usually measured by the ----------
Select correct option:
Time to execute a program or program mix
The speed with which it executes programs
Processor's utilization in solving the problems (not sure)
Instructions that can be carried out simultaneously
Question # 3 of 10 (Start time: 07:05:03 PM) Total Marks: 1
The external interface of FALCON-A consists of a _____ data bus.
Select correct option:
8-bit

16-bit
24-bit
32-bit
Quiz Start Time: 07:02 PM
Time Left 89
sec(s)
Question # 4 of 10 (Start time: 07:05:54 PM) Total Marks: 1
In which one of the following techniques, the time a processor spends waiting for instructions to be fetched from memory is minimized?
Select correct option:
Perfecting
Pipelining
Superscalar operation
Speedup
Question # 5 of 10 (Start time: 07:07:23 PM) Total Marks: 1
_____ control signal allows the contents of the Program Counter register to be written onto the internal processor bus.
Select correct option:
INC4
LPC
PCout (P # 174)
LC
Question # 6 of 10 (Start time: 07:08:09 PM) Total Marks: 1
----------is the ability of application software to operate on models of equipment newer than the model for which it was originally developed.
Select correct option:
Backward compatibility
Data migration
Reverse engineering
Upward compatibility
Question # 7 of 10 (Start time: 07:09:35 PM) Total Marks: 1
---------- performs the data operations as commanded by the program instructions.
Select correct option:
Control
Datapath
Structural RTL (not sure)
Timing
Question # 8 of 10 (Start time: 07:10:57 PM) Total Marks: 1
The external interface of FALCON-A consists of a _____address bus and a _____ data bus.
Select correct option:
8-bit , 8-bit
16-bit , 16-bit
16-bit , 24-bit
16-bit , 32-bit
Question # 9 of 10 (Start time: 07:11:17 PM) Total Marks: 1
Motorola MC68000 is an example of ---------microprocessor.
Select correct option:
CISC (P # 149)

RISC
SRC
FALCON
Question # 10 of 10 (Start time: 07:12:12 PM) Total Marks: 1
_____ enable the input to the PC for receiving a value that is currently on the internal processor bus.
Select correct option:
LPC (P # 174)
INC4
LC
Cout

==========

Set-08

Question # 1 of 10 (Start time: 10:37:35 AM) Total Marks: 1
A collection of ----------is called a micro program.
Select correct option:
large scale operations
Registers
DMA
Microinstructions.

Question # 2 of 10 (Start time: 10:38:31 AM) Total Marks: 1
---------- is the time needed by the CPU to recognize (not service) an interrupt request.
Select correct option:
Interrupt Latency
Response Deadline
Timer delay
Throughput

Question # 3 of 10 (Start time: 10:39:11 AM) Total Marks: 1
_____ controls the sequence of the flow of microinstructions.
Select correct option:
Multiplexer
Micro program controller
DMA Controller
Virtual Memory

Question # 4 of 10 (Start time: 10:39:42 AM) Total Marks: 1
Which one of the following is NOT a technique used when the CPU wants to exchange data with a
peripheral device?
Select correct option:
Direct Memory Access (DMA)
Interrupt driven I/O
Programmed I/O
` Virtual Memory (268)

Question # 5 of 10 (Start time: 10:40:33 AM) Total Marks: 1
Identify the following type of serial communication error condition: “The prior character that was
received was not still read by the CPU and is over written by a new received character.”
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

Question # 6 of 10 (Start time: 10:41:38 AM) Total Marks: 1
In which one of the following methods, does the CPU poll to identify the interrupting module and
branches to an interrupt service routine on detecting an interrupt?
Select correct option:
Daisy Chain
Software Poll
Multiple interrupt lines
All of the given options

Question # 7 of 10 (Start time: 10:42:50 AM) Total Marks: 1
An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
Select correct option:
Flip Flops
Memory
Peripheral devices
Multiplexers

Question # 8 of 10 (Start time: 10:43:23 AM) Total Marks: 1
In _____, a separate address space of the CPU is reserved for I/O operations.
Select correct option:
Isolated I/O
Memory Mapped I/O
All of above
None of above

Question # 9 of 10 (Start time: 10:43:53 AM) Total Marks: 1
In which one of the following methods for resolving the priority, the device with the highest priority is
placed in the first position, followed by lower-priority devices up to the device with the lowest priority,
which is placed last in the series?
Select correct option:
Asynchronous
Daisy-Chaining Priority
Parallel
Semi-synchronous

Question # 10 of 10 (Start time: 10:45:12 AM) Total Marks: 1
Every time you press a key, an interrupt is generated. This is an example of
Select correct option:
Hardware interrupt
Software interrupt
All of the given (not sure)
None of the given

Question # 1 of 10 (Start time: 10:48:56 AM) Total Marks: 1
_____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.
Select correct option:
Microprogramming
Instruction pre-fetching
Pipelining
` Partial decoding

Question # 2 of 10 (Start time: 10:49:43 AM) Total Marks: 1
An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
Select correct option:
Flip Flops
Memory
` Peripheral devices
Multiplexers

Question # 3 of 10 (Start time: 10:50:14 AM) Total Marks: 1
_____ is an electrical pathway through which the processor communicates with the internal and external
devices attached to the computer.
Select correct option:
Computer Bus
Hazard
Memory
Disk

Question # 4 of 10 (Start time: 10:51:37 AM) Total Marks: 1
Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)?
Select correct option:
``````Framing error
Parity error
Overrun error
Under-run error

Question # 5 of 10 (Start time: 10:53:07 AM) Total Marks: 1
How can you define an interrupt?
Select correct option:

A process where an external device can speedup the working of the microprocessor
A process where memory can speed up programs execution speed
``````A process where an external device can get the attention of the microprocessor
A process where input devices can takeover the working of the microprocessor
---
Question # 6 of 10 (Start time: 10:54:28 AM) Total Marks: 1
In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?
Select correct option:
Asynchronous
Daisy-Chaining Priority
Parallel
Semi-synchronous

Question # 7 of 10 (Start time: 10:55:13 AM) Total Marks: 1
In which one of the following methods, does the CPU poll to identify the interrupting module and branches to an interrupt service routine on detecting an interrupt?
Select correct option:
Daisy Chain
` Software Poll
Multiple interrupt lines
All of the given options

Question # 8 of 10 (Start time: 10:55:45 AM) Total Marks: 1
_____ controls the sequence of the flow of microinstructions.
Select correct option:
Multiplexer
`` Micro program controller
DMA Controller
Virtual Memory

Question # 9 of 10 (Start time: 10:56:14 AM) Total Marks: 1
A software routine performed when an interrupt is received by the computer is called as ---
Select correct option:
Interrupt
````Interrupt handler (not sure)
Exception
Trap

Question # 10 of 10 (Start time: 10:57:28 AM) Total Marks: 1
Identify the following type of serial communication error condition: “The prior character that was received was not still read by the CPU and is over written by a new received character.”
Select correct option:
Framing error
Parity error

Overrun error

Under-run error

==========

Set-09

What is the instruction length of the SRC processor?

► 8 bits

► *16 bits*

► **32 bits**

► *64 bits*

Question No: 2 (Marks: 1) - Please choose one

Which one of the following is the memory organization of ***FALCON-E processor?***

► 2^8 * 8 bits

► 2^{16} * 8 bits

► **2^{32} * 8 bits**

► 2^{64} * 8 bits

Question No: 3 (Marks: 1) - Please choose one

"If P = 1, then load the contents of register R1 into register R2".

This statement can be written in RTL as:

► *R1 ¬ R2*

► *P: R1 ¬ R2*

► **P: R2 ¬ R1**

► *P: R2 ¬ R1, P: R1 ¬ R2*

Question No: 4 (Marks: 1) - Please choose one

The instruction ----------will ***load*** *the register R3 with the contents of the memory location M [PC+56]*

► *Add R3, 56*

► *lar R3, 56*

► **ldr R3, 56**

► *str R3, 56*

Question No: 5 (Marks: 1) - Please choose one

----------are faster than cache memory

□□□□□□□►□*Accumulator register*

□□□□□□□►□**CPU registers**

□□□□□□□►□*I/O devices*

□□□□□□□►□*ROM*

Question No: 6 (Marks: 1) - Please choose one

P: R3 ¬ R5

MAR ¬ IR

These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?

- ▶ *Arrow ¬*
- ▶ *Colon :*
- ▶ **Comma ,**
- ▶ *Parentheses ()*

Question No: 7 (Marks: 1) - Please choose one

Prefetching can be considered a primitive form of----------

- ▶ **Pipelining**
- ▶ *Multi-processing*
- ▶ *Self-execution*
- ▶ *Exception*

Question No: 8 (Marks: 1) - Please choose one

The processor must have a way of saving information about its state or context so that it can be restored upon return from the ----------

- ▶ **Exception**
- ▶ *Function*
- ▶ *Stack*
- ▶ *Thread*

Question No: 9 (Marks: 1) - Please choose one

Which one of the following circuit design levels is called the gate level?

- □□□□□□□▶□**Logic Design Level**
- □□□□□□□▶□*Circuit Level*
- □□□□□□□▶□*Mask Level*
- □□□□□□□▶□*None of the given*

Question No: 10 (Marks: 1) - Please choose one

_____ enable the input to the PC for receiving a value that is currently on the internal processor bus.

- ▶ **LPC**
- ▶ *INC4*
- ▶ *LC*
- ▶ *Cout*

Question No: 11 (Marks: 1) - Please choose one

_____ operation is required to change the processor's state to a known, defined value.

- ▶ *Change*
- ▶ **Reset**
- ▶ *Update*
- ▶ *None of the given*

Question No: 12 (Marks: 1) - Please choose one

There are _____ types of reset operations in SRC

- ▶ **Two**
- ▶ *Three*

► *Four*
► *Five*

Question No: 13 (Marks: 1) - Please choose one
_____ controller controls the sequence of the flow of microinstructions.
► *Multiplexer*
► **Microprogram**
► *ALU*
► *None of the given*

Question No: 14 (Marks: 1) - Please choose one
FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is _____ wide.
► *8-bits*
► *24-bits*
► **32-bits**
► *64-bits*

Question No: 15 (Marks: 1) - Please choose one
Which of the following statement(s) is/are correct about Reduced Instruction Set Computer (RISC) architectures.
(i) The typical RISC machine instruction set is small, and is usually a subject of a CISC instruction set.
(ii) No arithmetic or logical instruction can refer to the memory directly.
(iii) A comparatively large number of user registers are available.
(iv) Instructions can be easily decoded through hard-wired control units.
► *(i) and (iii) only*
► **(i), (iii) and (iv)**
► *(i), (ii) and (iii) only*
► *(i),(ii),(iii) and (iv)*

Question No: 16 (Marks: 1) - Please choose one
Which one of the following register holds the instruction that is being executed?
► *Accumulator*
► *Address Mask*
► **Instruction Register**
► *Program Counter*

==========

Set-10

Question # 2 of 10 (Start time: 07:19:55 PM) Total Marks: 1
Which operator is used to „name" registers, or part of registers, in the Register Transfer Language?
Select correct option:
:=
&
%

©

Question # 3 of 10 (Start time: 07:21:14 PM) Total Marks: 1
The data movement instructions _____ data within the machine and to or from input/output devices.
Select correct option:
Store
Load
Move
None of given

Question # 4 of 10 (Start time: 07:22:15 PM) Total Marks: 1
Which one of the following is the memory organization of EAGLE processor?
Select correct option:
2^8 * 8 bits
2^16 * 8 bits
2^32 * 8 bits
2^64 * 8 bits

Question # 5 of 10 (Start time: 07:23:33 PM) Total Marks: 1
Which field of the machine language instruction is the "type of operation" that is to be performed?
Select correct option:
Op-code (or the operation code)
CPU registers
Memory cells
I/O locations

Question # 6 of 10 (Start time: 07:24:42 PM) Total Marks: 1
Which one of the following circuit design levels is called the gate level?
Select correct option:
Logic Design Level
Circuit Level
Mask Level
None of the given

Question # 7 of 10 (Start time: 07:26:07 PM) Total Marks: 1
Which one of the following is the highest level of abstraction in digital design in which the computer architect views
the system for the description of system components and their interconnections?
Select correct option:
Processor-Memory-Switch level (PMS level)
Instruction Set Level
Register Transfer Level
None of the given

Question # 8 of 10 (Start time: 07:27:23 PM) Total Marks: 1
What functionality is performed by the instruction “lar R3, 36” of SRC?
Select correct option:

It will load the register R3 with the contents of the m
It will load the register R3 with the relative address it
It will store the register R3 contents to the memory l
No operation

Question # 9 of 10 (Start time: 07:28:47 PM) Total Marks: 1
What is the working of Processor Status Word (PSW)?
Select correct option:
To hold the current status of the processor.
To hold the address of the current process
To hold the instruction that the computer is currently
To hold the address of the next instruction in memor

Quiz Start Time: 07:19 PM
Question # 10 of 10 (Start time: 07:30:15 PM) Total Marks: 1
Which one of the following portions of an instruction represents the operation to be performed?
Select correct option:
Address
Instruction code
Opcode
Operand

==========

Set-11

Question # 1 of 10 (Start time: 08:16:39 PM) Total Marks: 1
----------is the ability of application software to operate on models of equipment newer than the model for which it
was originally developed.
Select correct option:
Backward compatibility
Data migration
Reverse engineering
Upward compatibility

Question # 2 of 10 (Start time: 08:17:18 PM) Total Marks: 1
For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required;
which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers,
or the appropriate memory location.
Select correct option:
Registers
Control signals
Memory
None of the given

Question # 3 of 10 (Start time: 08:18:19 PM) Total Marks: 1

FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is _____ wide.
Select correct option:
8-bits
16-bits
32-bits
64-bits

Question # 4 of 10 (Start time: 08:19:38 PM) Total Marks: 1
Which one of the following register(s) contain(s) the address of the place the CPU wants to work with in the main
memory and is/are directly connected to the RAM chips on the motherboard?
Select correct option:
Instruction Register
Memory address register
Memory Buffer Register
Registers A and C

Question # 5 of 10 (Start time: 08:20:15 PM) Total Marks: 1
The external interface of FALCON-A consists of a _____ address bus.
Select correct option:
8-bit
16-bit
24-bit
32-bit

Question # 6 of 10 (Start time: 08:21:18 PM) Total Marks: 1
_____ control signal allows the contents of the Program Counter register to be written onto the internal processor
bus.
Select correct option:
INC4
LPC
PCout
LC

Question # 7 of 10 (Start time: 08:22:29 PM) Total Marks: 1
Computer system performance is usually measured by the ----------
Select correct option:
Time to execute a program or program mix
The speed with which it executes programs
Processor's utilization in solving the problems
Instructions that can be carried out simultaneously

Question # 8 of 10 (Start time: 08:22:51 PM) Total Marks: 1
Motorola MC68000 is an example of ---------microprocessor.
Select correct option:
CISC
RISC

SRC
FALCON

Question # 9 of 10 (Start time: 08:23:19 PM) Total Marks: 1
The external interface of FALCON-A consists of a _____ data bus.
Select correct option:
8-bit
16-bit
24-bit
32-bit

Question # 10 of 10 (Start time: 08:24:07 PM) Total Marks: 1
In which one of the following techniques, the time a processor spends waiting for instructions to be fetched from
memory is minimized?
Select correct option:
Perfecting
Pipelining
Superscalar operation
Speedup

==========

Set-12

Question # 1 of 10 (Start time: 11:38:36 PM) Total Marks: 1
Which one of the following is the memory organization of EAGLE processor?
Select correct option:
2^8 * 8 bits
2^16 * 8 bits==========ans
2^32 * 8 bits
2^64 * 8 bits

Question # 2 of 10 (Start time: 11:40:06 PM) Total Marks: 1
Which one of the following registers holds the address of the next instruction to be executed?
Select correct option:
Accumulator
Address Mask
Instruction Register
Program Counter==========ans

Question # 3 of 10 (Start time: 11:41:32 PM) Total Marks: 1
FALCON-A processor bus has 16 lines or is 16-bits wide while that of SRC is _____ wide.
Select correct option:
8-bits
16-bits
32-bits ==========ans
64-bits

Question # 4 of 10 (Start time: 11:42:41 PM) Total Marks: 1
What is the instruction length of the FALCON-E processor?
Select correct option:
8 bits
16 bits
32 bits ==========ans
64 bits

Question # 5 of 10 (Start time: 11:43:34 PM) Total Marks: 1
In----------address mode, the actual data is stored in the instruction.
Select correct option:
Direct
Indirect
Immediate ==========ans
Relative

Question # 6 of 10 (Start time: 11:45:02 PM) Total Marks: 1
Motorola MC68000 is an example of ---------microprocessor.
Select correct option:
CISC ==========ans
RISC
SRC
FALCON

Question # 7 of 10 (Start time: 11:46:11 PM) Total Marks: 1
Computer system performance is usually measured by the ----------
Select correct option:
Time to execute a program or program**mix==========ans**
The speed with which it executes programs
Processor's utilization in solving the problems
Instructions that can be carried out simultaneously

Question # 8 of 10 (Start time: 11:47:32 PM) Total Marks: 1
Which one of the following registers holds the instruction that is being executed?
Select correct option:
Accumulator
Address Mask
Instruction Register ==========ans
Program Counter

Question # 9 of 10 (Start time: 11:48:40 PM) Total Marks: 1
For any of the instructions that are a part of the instruction set of the SRC, there are certain _____ required; which may be used to select the appropriate function for the ALU to be performed, to select the appropriate registers, or the appropriate memory location.
Select correct option:
Registers
Control signals ==========ans
Memory

None of the given

Question # 10 of 10 (Start time: 11:50:11 PM) Total Marks: 1
Which one of the following register(s) contain(s) the address of the place the CPU wants to work with in the main memory and is/are directly connected to the RAM chips on the motherboard?
Select correct option:
Instruction Register
Memory address register
Memory Buffer Register
Registers A and C ==========ans

==========

Set-13

==========

Set-17

Question # 1 of 10 (Start time: 07:15:10 PM) Total Marks: 1
In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?
Select correct option:

Arithmetic/logic
Load/store
Test/branch
None of the given

Question # 2 of 10 (Start time: 07:16:06 PM) Total Marks: 1
Which one of the following circuit design levels is called the gate level?
Select correct option:

Logic Design Level

Circuit Level
Mask Level
None of the given

Question # 3 of 10 (Start time: 07:17:26 PM) Total Marks: 1
What does the RTL expression [M(1234)] means?
Select correct option:

The contents of memory whose address is 1234.
The contents of data register 1234

The effective address of register 1234
The address of memory whose address is 1234.

Question # 4 of 10 (Start time: 07:19:00 PM) Total Marks: 1
Which type of instructions load data from memory into registers, or store data from registers into memory and transfer data between different kinds of special-purpose registers?
Select correct option:

Arithmetic
Control
Data transfer
Floating point

Question # 5 of 10 (Start time: 07:20:00 PM) Total Marks: 1
Which type of instructions enables mathematical computations?
Select correct option:

Arithmetic
Control
Data transfer
Floating point

Question # 6 of 10 (Start time: 07:21:00 PM) Total Marks: 1
What is the instruction length of the FALCON-E processor?
Select correct option:

8 bits
16 bits
32 bits
64 bits

Question # 7 of 10 (Start time: 07:22:33 PM) Total Marks: 1
Which one of the following is the memory organization of EAGLE processor?
Select correct option:

2^8 * 8 bits
2^16 * 8 bits
2^32 * 8 bits
2^64 * 8 bits

Question # 8 of 10 (Start time: 07:23:56 PM) Total Marks: 1
Type A of SRC has which of the following instructions? a) andi,

instruction b) No operation or nop instruction c) lar instruction d) ldr instruction e) Stop operation or stop instruction
Select correct option:

(a)& (b)
(b)&(c)
(a)&(e)
(b)&(e)

Question # 9 of 10 (Start time: 07:25:30 PM) Total Marks: 1
Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A and source register B) from the following example. ADD R1, R2, R3
Select correct option:

Opcode= R1, DR=ADD, SA=R2, SB=R3
Opcode= ADD, DR=R1, SA=R2, SB=R3
Opcode= R2, DR=ADD, SA=R1, SB=R3
Opcode= ADD, DR=R3, SA=R2, SB=R1

Question # 1 of 10 (Start time: 07:31:22 PM) Total Marks: 1
Which instruction is used to store register to memory using relative address?
Select correct option:

ld instruction
ldr instruction
lar instruction
str instruction

Question # 2 of 10 (Start time: 07:32:11 PM) Total Marks: 1
Which one of the following languages presents a simple, human-oriented language to specify the operations, register communication and timing of the steps that take place within a CPU to carry out higher level (user programmable) instructions?
Select correct option:

Assembly Language
OOP(Object Oriented Language)
RTL (Register Transfer Language)
UML(Unified Modeling language)

Question # 3 of 10 (Start time: 07:33:40 PM) Total Marks: 1
Which one of the following instructions is used to load register from

memory using a relative address?
Select correct option:

la
lar
ldr
str

Question # 4 of 10 (Start time: 07:34:15 PM) Total Marks: 1
Which field of the machine language instruction is the "type of operation" that is to be performed?
Select correct option:

Op-code (or the operation code)
CPU registers
Memory cells
I/O locations

Question # 5 of 10 (Start time: 07:35:43 PM) Total Marks: 1
What is the instruction length of the FALCON-A processor?
Select correct option:

8 bits
16 bits
32 bits
64 bits

Question # 6 of 10 (Start time: 07:37:17 PM) Total Marks: 1
Which one of the following are the code size and the Number of memory bytes respectively for a 3-address instruction?
Select correct option:

0 bytes, 10 bytes
4 bytes, 7 bytes
7 bytes, 16 bytes
10 bytes, 19 bytes

Question # 7 of 10 (Start time: 07:38:47 PM) Total Marks: 1
The data movement instructions _____ data within the machine and to or from input/output devices.
Select correct option:

Store

Load
Move
None of given

Question # 8 of 10 (Start time: 07:40:20 PM) Total Marks: 1
In----------address mode, the actual data is stored in the instruction.
Select correct option:

Direct
Indirect
Immediate
Relative

Question # 9 of 10 (Start time: 07:41:44 PM) Total Marks: 1
Which one of the following are the code size and the Number of memory bytes respectively for a 2-address instruction?
Select correct option:

4 bytes, 7 bytes
7 bytes, 16 bytes
10 bytes, 19 bytes
13 bytes, 22 bytes

Question # 10 of 10 (Start time: 07:42:43 PM) Total Marks: 1
Which type of instructions enables mathematical computations?
Select correct option:

Arithmetic
Control
Data transfer
Floating point

==========

Set-18

Question # 1 of 10 (Start time: 07:13:18 PM) Total Marks: 1
Which one of the following methods for resolving the priority makes use of individual bits of a priority encoder?
Select correct option:
Daisy-Chaining Priority
Asynchronous Priority
Parallel Priority
Semi-synchronous Priority

Question # 2 of 10 (Start time: 07:13:50 PM) Total Marks: 1
Identify the type of serial communication error condition in which a 0 is received instead of a stop bit (which is always a 1)?
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

Question # 3 of 10 (Start time: 07:14:25 PM) Total Marks: 1
What happens when the microprocessor is interrupted?
Select correct option:
It suspends the currently executing program and jumps to ISR to respond to the incoming interrupt
It suspends the incoming interrupt and keeps executing current program.
It makes a queue for all such incoming interrupts so as to respond to them after system restart.
All of the given options

Question # 4 of 10 (Start time: 07:15:24 PM) Total Marks: 1
CRC has ---------- overhead as compared to Hamming code.
Select correct option:
Equal
Greater
Lesser
None of the given

Question # 5 of 10 (Start time: 07:16:43 PM) Total Marks: 1
Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)?
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

Question # 6 of 10 (Start time: 07:17:17 PM) Total Marks: 1
The ------- can also be used anywhere in the source file to force code at a particular address in the memory.
Select correct option:
.end directive
.start directive
.label directive
.org directive

Question # 7 of 10 (Start time: 07:18:04 PM) Total Marks: 1
If NMI and INTR both interrupts occur simultaneously, then which one has the precedence over the other.

Select correct option:
NMI
INTR
INTR
All of the given

Question # 8 of 10 (Start time: 07:19:17 PM) Total Marks: 1
Select the parts of a hard disk.
Select correct option:
Header only
Data section and a trailer
Data section only
Header, data section and a trailer.

Question # 9 of 10 (Start time: 07:20:19 PM) Total Marks: 1
Identify the following type of serial communication error condition in which no character is available at the beginning of an interval.
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

Question # 10 of 10 (Start time: 07:21:12 PM) Total Marks: 1
How can you define an interrupt?
Select correct option:
A process where an external device can speedup the working of the microprocessor
A process where memory can speed up programs execution speed
A process where an external device can get the attention of the microprocessor
A process where input devices can takeover the working of the microprocessor

Question # 1 of 10 (Start time: 07:25:23 PM) Total Marks: 1
CRC has ---------- overhead as compared to Hamming code.
Select correct option:
Equal
Greater
Lesser
None of the given

Question # 2 of 10 (Start time: 07:26:34 PM) Total Marks: 1
All ----------interrupts have priority over all ---------interrupts
Select correct option:
internal, external
external,internal

Question # 3 of 10 (Start time: 07:27:07 PM) Total Marks: 1
The _____ of an m digit number x is xc'=bm -1- x
Select correct option:

Radix Compliment
Diminished Radix Compliment
Signed Magnitude Form
Biased Representation
Question # 4 of 10 (Start time: 07:28:02 PM) Total Marks: 1
Raid Level ____ is not a true member of the RAID family.
Select correct option:
0
2
3
4

Question # 5 of 10 (Start time: 07:28:16 PM) Total Marks: 1
In which one of the following methods for resolving the priority, the ACK is passed from device to device until it hits a device?
Select correct option:
Asynchronous
Daisy-Chaining Priority
Parallel
Semi-synchronous

Question # 6 of 10 (Start time: 07:29:42 PM) Total Marks: 1
Taking control of the system bus for a few bus cycles is known as _____.
Select correct option:
Bus Stealing
Cycle Stealing
Cycle Transfering
None of given

Question # 7 of 10 (Start time: 07:30:23 PM) Total Marks: 1
Identify the following type of serial communication error condition: “The prior character that was received was not still read by the CPU and is over written by a new received character.”
Select correct option:
Framing error
Parity error
Overrun error
Under-run error

Question # 8 of 10 (Start time: 07:31:50 PM) Total Marks: 1
The interrupts in which we write the address of the interrupt service routine (ISR) in the interrupt instruction itself are
Select correct option:
Maskable
Non-maskable
Non-maskable
Vectored

Question # 9 of 10 (Start time: 07:33:01 PM) Total Marks: 1

Given an m-digit base b number x, the _____ of x is xc = (bm– x) mod bm
Select correct option:
Radix Compliment
Diminished Radix Compliment
Signed Magnitude Form
Biased Representation

Question # 10 of 10 (Start time: 07:34:02 PM) Total Marks: 1
Which I/O technique will be used by a sound card that may need to access data stored in the computer's RAM?
Select correct option:
Programmed I/O
Interrupt driven I/O
Direct memory access(DMA)
Polling

==========

Set-19

How many types of instructions are available in SRC? Name them. What is the format of each of these instructions.....5marks

Answer:

Write the Structural RTL for the call instruction for uni-bus data path implementation. call ra, rb.....5 marks

Answer:

Write the Structural RTL for the mov instruction for uni-bus data path implementation. mov ra, rb.....3 marks

Answer:

How many stages are in the pipelined version of SRC? Name them.....3 marks

Answer:

How can you define microprogram?.....2 marks

Answer:

Write the Structural RTL for the 'not instruction'.....2 marks

Answer:

==========

Set-20

Question # 1
In which of the following addressing modes, the operand does not specify an address but it is the actual data to be used.
Direct
Indirect
Immediate
Relative
Question # 2
Which one of the following registers holds the address of the next instruction to be executed?
Accumulator
Address Mask
Instruction Register
Program Counter
Question # 3
In which of the following techniques, the time a process spends waiting for instructions to be fetched from memory is minimized?
Prefecting
Pipelining
Superscalar operation
Speedup

Question # 4
The external interface of FALCON-A consists of a address bus.
8-bit
16-bit
24-bit
32-bit
Question # 5
Which one of the following is the memory organization of EAGLE processor?
2^8*8 bits
2^16*8 bits
2^32*8 bits
2^64*8 bits

Question # 7
The External interface of FALCON-A consists of a address bus and a data bus.
8bit, 8bit
16-bit,16-bit
16-bit,24-bit

16-bit, 32-bit

Question # 8
Computer system performance is usually measured by the
Time to execute a program or program mix
The speed with which it executes programs
Processor's utilization in solving the problems
Instructions that can be carried out simultaneously

Question # 9
Which one of the following registers holds the instruction that is being executed?
Accumulator
Address Mask
Instruction Register
Program Counter

Question # 10
Matorola MC68000 is an example of microprocessor.
CISC
Risc
SRC
Identify the opcode, destination register (DR), source registers (SA and SB i/e source register A and source register **B)** from the following example. ADD R1, R2, R3
Select correct option:
Opcode= R1, DR=ADD, SA=R2, SB=R3
Opcode= ADD, DR=R1, SA=R2, SB=R3
Opcode= R2, DR=ADD, SA=R1, SB=R3
Opcode= ADD, DR=R3, SA=R2, SB=R1

Which type of instructions help in changing the flow of the program as and when required?
Select correct option:

Arithmetic
Control
Data transfer
Floating point

Almost every commercial computer has its own particular ---------- language
Select correct option:
3GL
English language

Higher level language
assembly language
Which one of the following is a binary cell capable of storing one bit of information?
Select correct option:

Decoder
Flip-flop
Multiplexer
Diplexer
Which statement(s)from the following is/are correct about Reduced Instruction Set Computer (RISC) architectures.
(i) The typical RISC machine instruction set is small, and is usually a subject of a CISC instruction set.
(ii) (ii) No arithmetic or logical instruction can refer to the memory directly.
(iii) (iii) A comparatively large number of user registers are available.
(iv) (iv) Instructions can be easily decoded through hard-wired control units.
Select correct option:

(i) and (iii) only
(i), (iii) and (iv)
(i), (ii) and (iii) only
(i),(ii),(iii) and (iv)

What is the instruction length of the FALCON-E processor?
Select correct option:

8 bits
16 bits
32 bits
64 bits

Which one of the following are the code size and the Number of memory bytes respectively for a 3-address instruction?
Select correct option:

0 bytes, 10 bytes
4 bytes, 7 bytes
7 bytes, 16 bytes
10 bytes, 19 bytes

The CPU includes three types of instructions, which have different operands and will need different representations. Which one of the instructions requires two source registers?

Select correct option:

Jump and branch format instructions
Immediate format instructions
Register format instructions
All of the above

Which one of the following are the code size and the Number of memory bytes respectively for a 2-address instruction?
Select correct option:

4 bytes, 7 bytes
7 bytes, 16 bytes
10 bytes, 19 bytes
13 bytes, 22 bytes

Nadia: P: R3 <- R5 MAR <- IR These two are instructions written using RTL .If these two operations is to occur simultaneously then which symbol will we use to separate them so that it becomes a correct statement with the condition that two operations occur simultaneously?
Select correct option:

Parentheses ()
Arrow <-
Colon :
Comma ,
In which of the following instructions the data move between a register in the processor and a memory location (or another register) and are also called data movement?
Select correct option:
Arithmetic/logic
Load/store
Test/branch
None of the given

In which one of the following addressing modes, the operand does not specify an address but it is the actual data to be used.
Select correct option:

Direct
Indirect
Immediate
Relative

Which one of the following portions of an instruction represents the operation to be performed?
Select correct option:

Address
Instruction code
Opcode
Operand

==========

Set-20

CS501_Short Questions

Q1- What is Reset operation describe it types

Answer:

Q2- Describe super scaler and VILW.

Answer:

Q3- Write RTL functions and there was a rb +rc instruction

Answer:

Q5-. Write the structural RTL for " in ra, rb"

Answer:

Write the Structural RTL description for un-conditional jump instruction for uni-bus data path implementation. (5 Marks)

Answer:

1. What function is performed by the reset operation of a processor and differentiate Hard reset and Soft reset? [5 marks]

Answer:

2. Write the Structural RTL for the mov instruction for uni-bus data path implementation. mov ra, rb 3 marks

Answer:

3. Write the Structural RTL for shift right instruction. 2 marks

Answer:

4. What is the use of "NOP" instruction in pipe lining? 3 marks vuzs

Answer:

Some MCQs are as follows
1). LPC: This control signal will enable write of the Program Counter, thus the new, incremented value can be written into the PC if it is made available on the "in" bus. Note that the ALSU is assumed to include an INC4 function.
2). Anything that interrupts the normal flow of execution of instructions in the processor is called an exception.
3).What is the size of the memory space that is available to FALCON-A processor?

2^8 bytes
2^16 bytes
2^32 bytes
2^64 bytes
4). What is the working of Processor Status Word (PSW)?
To hold the current status of the processor.
To hold the address of the current process
To hold the instruction that the computer is currently processing vuzs
To hold the address of the next instruction in memory that is to be executed

5). What is the instruction length of the FALCON-E processor?

8 bits
16 bits
32 bits
64 bits
6). Which one of the following portions of an instruction represents the operation to be performed?
Address
Instruction code
Opcode
Operand
7). Which instruction is used to store register to memory using relative address?
ld instruction
ldr instruction
lar instruction
str instruction
Helping topic: SRC instruction format.
8). Which type of instructions help in changing the flow of the program as and when required? vuzs.net
Arithmetic
Control
Data transfer
Floating point

9). A MCQ about **Power PC**

10). which one of the following is 0-address based machine.
11). There was a very long MCQ not remember now but the options are,
VCON
FCON
ACON
LCON
I already found all of them keywords on handouts but there is nothing like this.

FINALTERM EXAMINATION
Fall 2008

CS501- Advance Computer Architecture (Session - 1)

Shared by Eagle Eye (Tabish Ali Raza) & Strange_Stranger (Uzair Husnain)

M a r k s: 75

CS501 Question No: 1
Which one of the following is the memory organization of **SRC processor?**
- 28 * 8 bits
- 216 * 8 bits
- 232 * 8 bits
- 264 * 8 bits

CS501 Question No: 2
Type A format of SRC uses ----------instructions
- two
- three
- four
- five

CS501 Question No: 3
The instruction ----------will **load**
the register R3 with the contents of the memory
location M [PC+56]
- Add R3, 56
- lar R3, 56
- ldr R3, 56
- str R3, 56

CS501 Question No: 4
Which format of the instruction is called the accumulator?
- 3-address instructions
- 3-address instructions
- 2-address instructions
- 1-address instructions
- 0-address instructions

CS501 Question No: 5
Which one of the following are the **code size**
and the **Number of memory**
bytes respectively for a 2-address instruction?
- 4 bytes, 7 bytes
- 7 bytes, 16 bytes

- 10 bytes, 19 bytes
- 13 bytes, 22 bytes

CS501 Question No: 6

Which operator is used to name registers, or part of registers, in the Register Transfer Language?

- :=
- &
- %
- ©

CS501 Advance Computer Architecture - MCQS from Quiz #3

1. A collection of ----------is called a micro program.

A. large scale operations
B. Registers
C. DMA
D. Microinstructions

Microinstructions.

2. ____is the time needed by the CPU to recognize (not service) an interrupt request

A. Interrupt Latency
B. Response Deadline
C. Timer delay
D. Throughput

Interrupt Latency.

3. _____ controls the sequence of the flow of microinstructions.

A. Multiplexer
B. Micro program controller
C. DMA Controller
D. Virtual Memory

Micro program controller.

4. Which one of the following is NOT a technique used when the CPU wants to exchange data with a peripheral device?

A. Direct Memory Access (DMA)
B. Interrupt driven I/O
C. Programmed I/O
D. Virtual Memory

Virtual Memory .

5. Identify the following type of serial communication error condition: “The prior character that was received was not still read by the CPU and is over written by a new received character.”

A. Framing error
B. Parity error
C. Overrun error
D. Under-run error

Overrun error.

6. In which one of the following methods, does the CPU poll to identify the interrupting module and branches to an interrupt service routine on detecting an interrupt?
A. Daisy Chain
B. Software Poll
C. Multiple interrupt lines
D. All of the given options

Software Poll.

7. An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
A. Flip Flops
B. Memory
C. Peripheral devices
D. Multiplexers

Peripheral devices.

8. In _____, a separate address space of the CPU is reserved for I/O operations.
A. Isolated I/O
B. Memory Mapped I/O
C. All of above
D. None of above
Isolated I/O.

9. In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?
A. Asynchronous
B. Daisy-Chaining Priority
C. Parallel
D. Semi-synchronous

Parallel.

10. _____ is a technique in which some of the CPU's address lines forming an input to the address decoder are ignored.
A. Microprogramming
B. Instruction pre-fetching
C. Pipelining

D. Partial decoding

Partial decoding.

11. An interface that can be used to connect the microcomputer bus to _____is called an I/O Port.
A. Flip Flops
B. Memory
C. Peripheral devices
D. Multiplexers

Peripheral devices.

12. _____ is an electrical pathway through which the processor communicates with the internal and external devices attached to the computer.
A. Computer Bus
B. Hazard
C. Memory
D. Disk

Computer Bus.

13. Identify the type of serial communication error condition in which A 0 is received instead of a stop bit (which is always a 1)?
A. Framing error
B. Parity error
C. Overrun error
D. Under-run error

Framing error.

14. How can you define an interrupt?
A. A process where an external device can speedup the working of the microprocessor
B. A process where memory can speed up programs execution speed
C. A process where an external device can get the attention of the microprocessor
D. A process where input devices can takeover the working of the microprocessor

A process where an external device can get the attention of the microprocessor.

15. In which one of the following methods for resolving the priority, the device with the highest priority is placed in the first position, followed by lower-priority devices up to the device with the lowest priority, which is placed last in the series?
A. Asynchronous
B. Daisy-Chaining Priority
C. Parallel
D. Semi-synchronous

Parallel.

16. In which one of the following methods, does the CPU poll to identify the interrupting module and branches to an interrupt service routine on detecting an interrupt?
A. Daisy Chain
B. Software Poll
C. Multiple interrupt lines
D. All of the given options
Software Poll.

17. _____ controls the sequence of the flow of microinstructions.
A. Multiplexer
B. Micro program controller
C. DMA Controller
D. Virtual Memory
Micro program controller.

18. Identify the following type of serial communication error condition: "The prior character that was received was not still read by the CPU and is over written by a new received character."
A. Framing error
B. Parity error
C. Overrun error
D. Under-run error
Overrun error.

Quiz by SHabana Iqbal

Question # 2 of 10 (Start time: 07:19:55 PM) Total Marks: 1
Which operator is used to „name" registers, or part of registers, in the Register Transfer Language?
Select correct option:
:=
&
%
©

Question # 3 of 10 (Start time: 07:21:14 PM) Total Marks: 1
The data movement instructions _____ data within the machine and to or from input/output devices.
Select correct option:
Store
Load
Move
None of given

Question # 4 of 10 (Start time: 07:22:15 PM) Total Marks: 1
Which one of the following is the memory organization of EAGLE processor?
Select correct option:
2^8 * 8 bits
2^16 * 8 bits
2^32 * 8 bits
2^64 * 8 bits

Question # 5 of 10 (Start time: 07:23:33 PM) Total Marks: 1
Which field of the machine language instruction is the "type of operation" that is to be performed?
Select correct option:
Op-code (or the operation code)
CPU registers
Memory cells
I/O locations

Question # 6 of 10 (Start time: 07:24:42 PM) Total Marks: 1
Which one of the following circuit design levels is called the gate level?
Select correct option:
Logic Design Level
Circuit Level
Mask Level
None of the given

Question # 7 of 10 (Start time: 07:26:07 PM) Total Marks: 1
Which one of the following is the highest level of abstraction in digital design in which the computer architect views
the system for the description of system components and their interconnections?
Select correct option:
Processor-Memory-Switch level (PMS level)
Instruction Set Level
Register Transfer Level
None of the given

Question # 8 of 10 (Start time: 07:27:23 PM) Total Marks: 1
What functionality is performed by the instruction “lar R3, 36” of SRC?
Select correct option:
It will load the register R3 with the contents of the m
It will load the register R3 with the relative address i
It will store the register R3 contents to the memory
No operation

Question # 9 of 10 (Start time: 07:28:47 PM) Total Marks: 1
What is the working of Processor Status Word (PSW)?
Select correct option:
To hold the current status of the processor.
To hold the address of the current process
To hold the instruction that the computer is currently
To hold the address of the next instruction in memor

Question # 10 of 10 (Start time: 07:30:15 PM) Total Marks: 1
Which one of the following portions of an instruction represents the operation to be performed?
Select correct option:
Address
Instruction code
Opcode
Operand

~*23july 2011*~
4 question from DMA nad Interrupt I/O
what is pipelining ?with or without
Consider a LAN, using bus topology. If we replace the bus with a switch, what change
will occur in such a configuration?
floating poit numerical qs 5 marks
base 10 sai 2 question the

==========

Set-23

In Single-Precision Binary Floating Point Representation , the exponent is _____
8 bit
11 bit
1 bit
23 bit

The 32 floating-point registers can hold 32 single-precision (32 bits), 16 double-precision (64 bits), or 8 extended-precision (128 bits) floating- point numbers

Which of the following register(s) contain(s) the address of the place the CPU want to work with in the main memory and is/are directly connected to the RAM chips on the motherboard?

IR

MAR

MBR

Register A and C