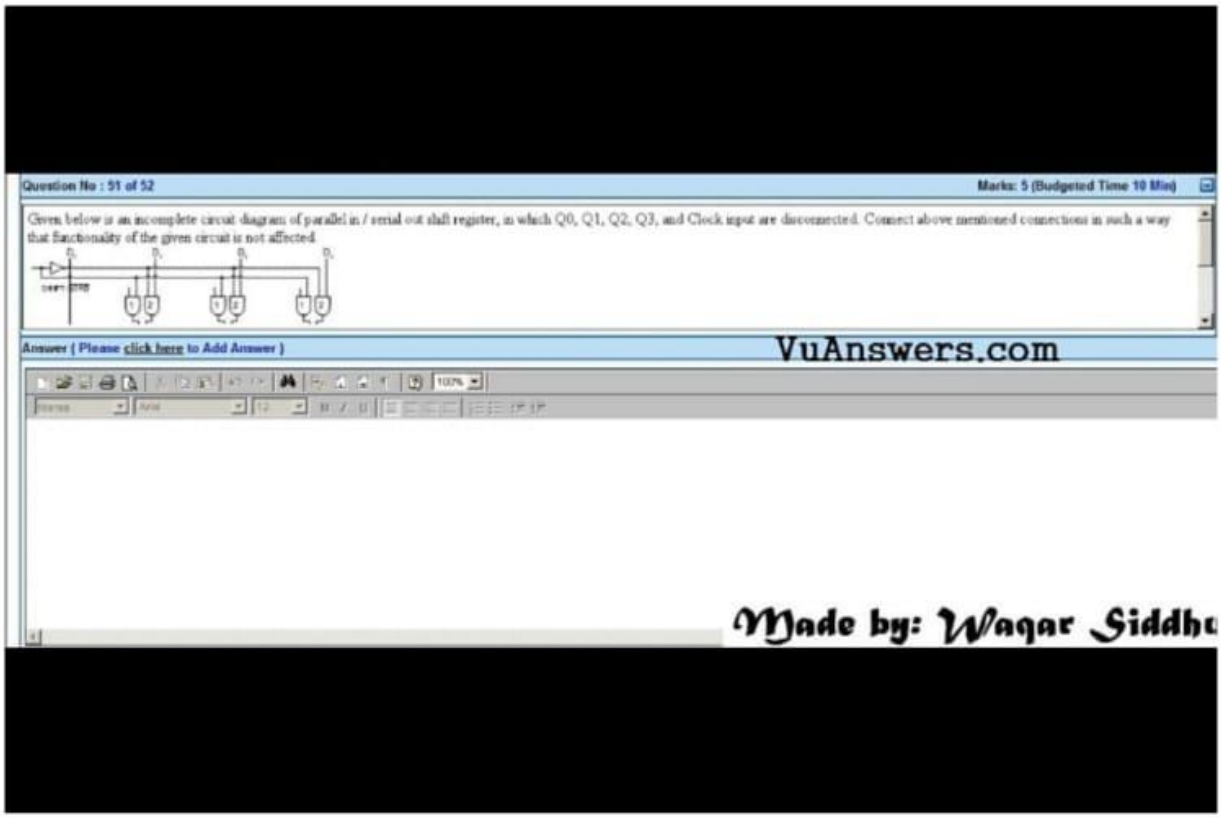
**Question No : 42 of 52**

What is meant by "excitation inputs"?

**Answer ( Please click here to Add Answer )**


A general Sequential circuit consists of a combinational circuit and a memory element. The memory element is made of a set of n flip-flops all connected to a a common clock. The n flip flops store 2n states. The flip-flops change their current state to the next state on each clock transition. The next state is determined by the current state and the external input. The output of the State Machine is determined by the current state and external input. The inputs to the memory which allow the memory to change its state on a clock transition are known as excitation inputs or excitation variables.



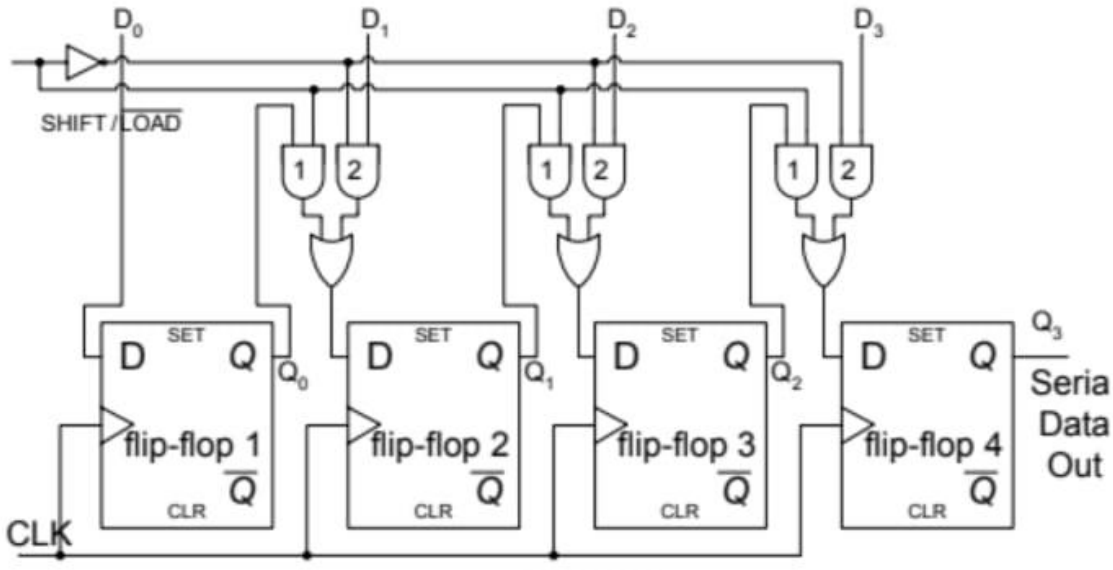



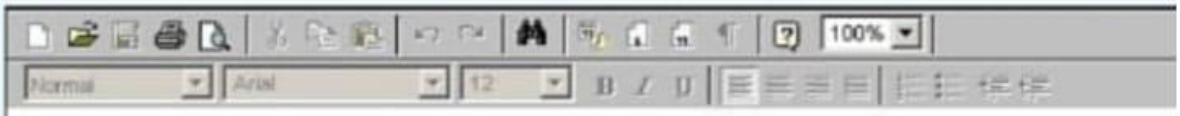

Figure 34.8 4-bit Parallel In/Serial Out Shift register

**Question No : 51 of 52**

Draw a complete test vector table for a 3-bit up/down counter using the following information.

- X is excitation input (if X=0, counter counts upward and vice versa).
- When the Clear input is 0 the output is cleared to 000 irrespective of the X.
- When the Clear input is set to 1 counter functions normally.
- Clear, Clock and X are inputs for up-down counter.

**Answer ( Please click here to Add Answer )**



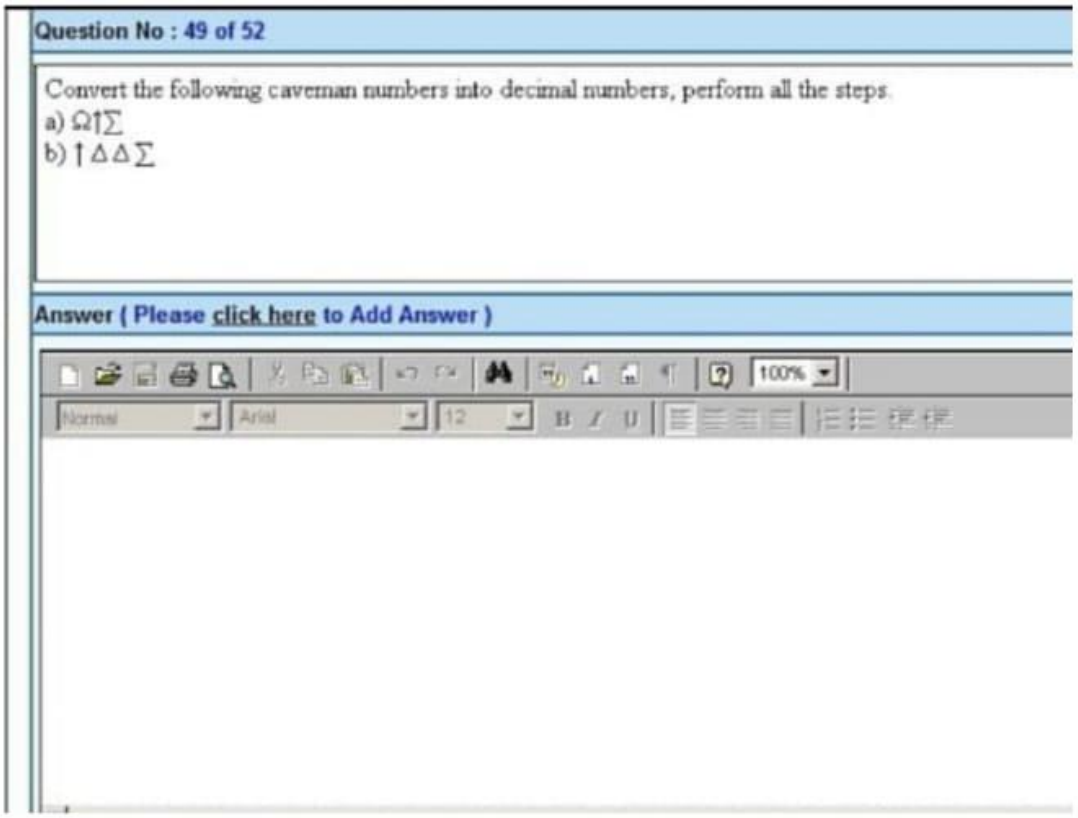

| Test Vector |
|---|
| ([Clock, Clear, X] -> [Q2, Q1, Q0]) |
| [ .c. , 0 ,x.] -> [0 , 0 , 0 ]; |
| [ .c. , 1 , 0 ] -> [0 , 0 , 1 ]; |
| [ .c. , 1 , 0 ] -> [0 , 1 , 0 ]; |
| [ .c. , 1 , 0 ] -> [0 , 1 , 1 ]; |
| [ .c. , 1 , 0 ] -> [1 , 0 , 0 ]; |
| [ .c. , 1 , 0 ] -> [1 , 0 , 1 ]; |
| [ .c. , 1 , 0 ] -> [1 , 1 , 0 ]; |
| [ .c. , 1 , 0 ] -> [1 , 1 , 1 ]; |
| [ .c. , 1 , 0 ] -> [0 , 0 , 0 ]; |
| [ .c. , 1 , 1 ] -> [1 , 1 , 1 ]; |
| [ .c. , 1 , 1 ] -> [1 , 1 , 0 ]; |
| [ .c. , 1 , 1 ] -> [1 , 0 , 1 ]; |
| [ .c. , 1 , 1 ] -> [1 , 0 , 0 ]; |



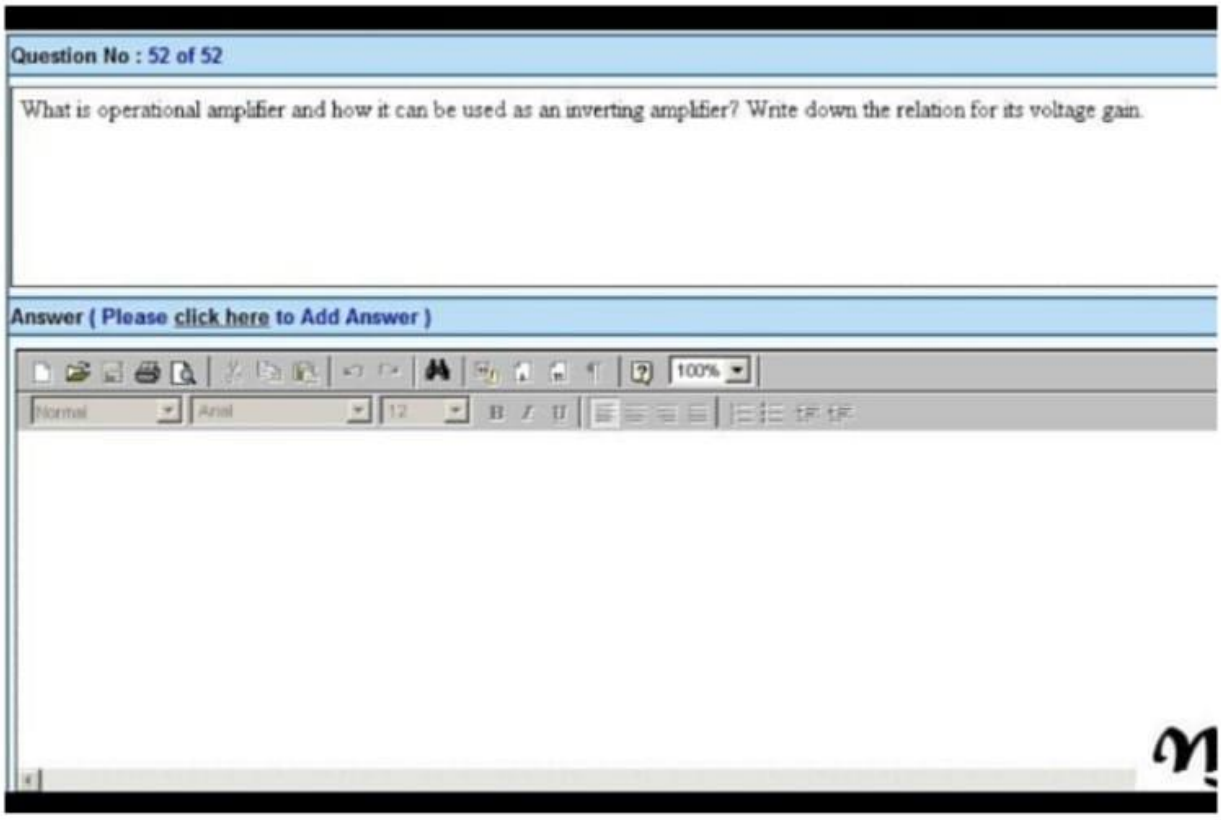
| |
|---|
| [ .c. , 1 , 1 ] -> [0 , 1 , 1 ]; |
| [ .c. , 1 , 1 ] -> [0 , 1 , 0 ]; |
| [ .c. , 1 , 1 ] -> [0 , 0 , 1 ]; |
| [ .c. , 1 , 1 ] -> [0 , 0 , 0 ]; |

Table 36.3c Test Vector Definition of 3-bit Up/Down Counter




| Decimal Number | Caveman Number | Decimal Number | Caveman Number |
|---|---|---|---|
| 0 | ∑ | 10 | >∑ |
| 1 | Δ | 11 | >Δ |
| 2 | > | 12 | >> |
| 3 | Ω | 13 | >Ω |
| 4 | ↑ | 14 | >↑ |
| 5 | Δ∑ | 15 | Ω∑ |
| 6 | ΔΔ | 16 | ΩΔ |
| 7 | Δ> | 17 | Ω> |
| 8 | ΔΩ | 18 | ΩΩ |
| 9 | Δ↑ | 19 | Ω↑ |
| | | 20 | ↑∑ |

Table 1.1 Decimal equivalents of the Caveman Numbers




Operational Amplifier is a linear amplifier which has two inputs (inverting and non-inverting) and one output. It has a high voltage gain, high input impedance and low output impedance. The Op-Amp amplifies the difference signal between its inverted and non-inverted inputs. Figure 44.6a

The Op-Amp is used as an inverting amplifier and as a comparator. When the Op-Amp is used as an inverting amplifier, the input signal is applied at its Inverted input through a series resistance $R_i$. The output of the Op-Amp is connected to the inverted input through a feedback resistance $R_f$. Figure 44.6b. The voltage gain of the Inverting Amplifier is given by the relation

$$V_{out}/V_{in} = - R_f/R_i$$

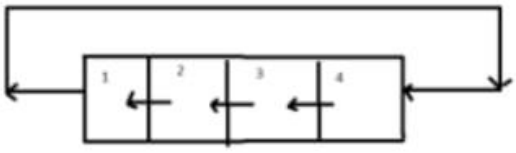
Question No : 51 of 52

Make block diagram of Rotate Left Operation of a shift register and explain its working.

Answer ( Please click here to Add Answer )

**Answer**:

The serial output of the register is connected to the serial input of the register. By applying clock pulses data is shifted left. The data shifted out of the serial out pin at the left hand side is re-circulated back into the shift register input at the right hand side. Thus the data is rotated left within the register.

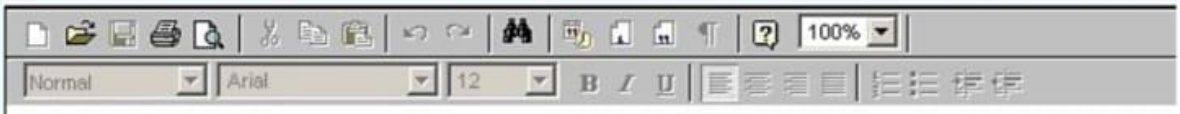



Rotate Left Operation

**Question No : 48 of 52**

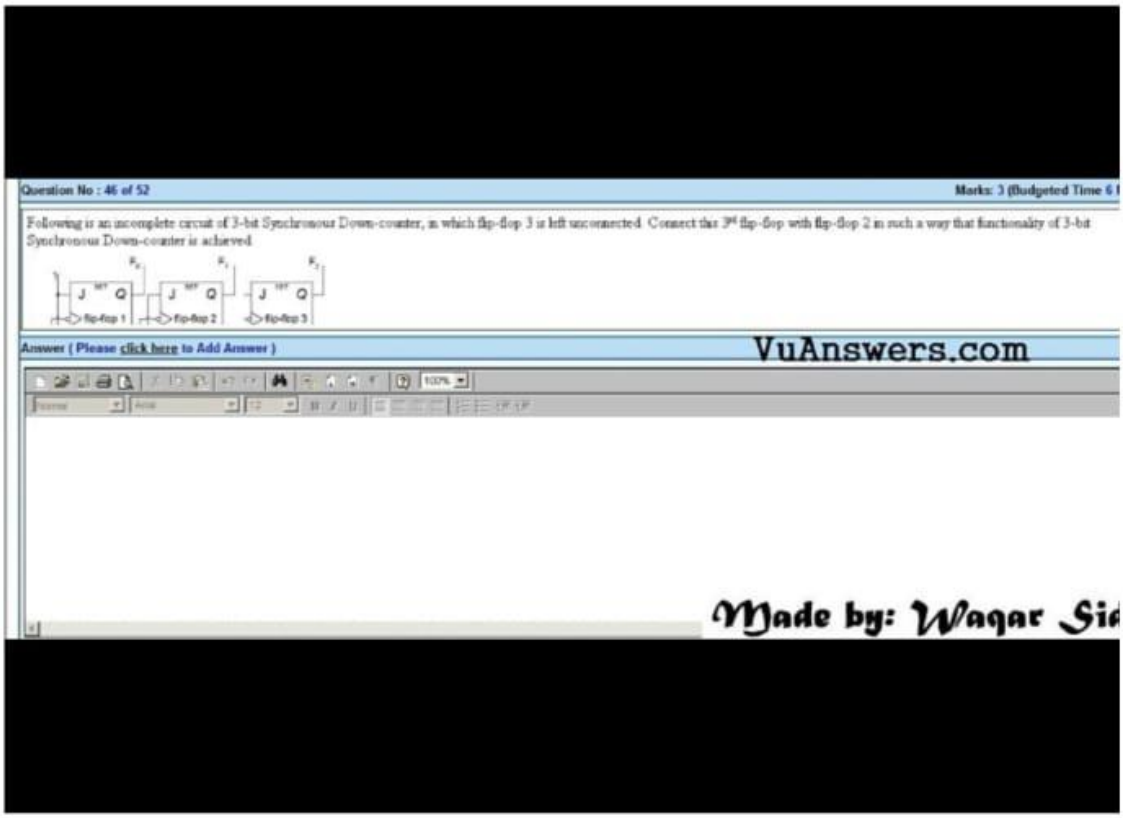
What is RAM Stack, which register stores the address of top of the stack?

**Answer ( Please click here to Add Answer )**




What is RAM Stack, which register stores the address of the top of the stack?

**Answer**:
Shift Register based stack implementation finds use in specialized digital systems. A practical way to implement the program stack which a program under execution uses to access variables is by means of the RAM memory. The stack is known as a RAM stack. A special purpose register known as the Stack Pointer Register stores the address of the top of the stack and a reserved area in the RAM memory.



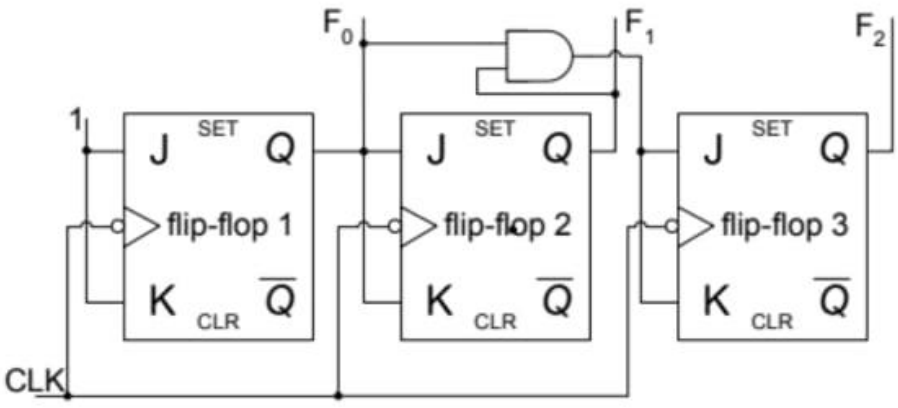
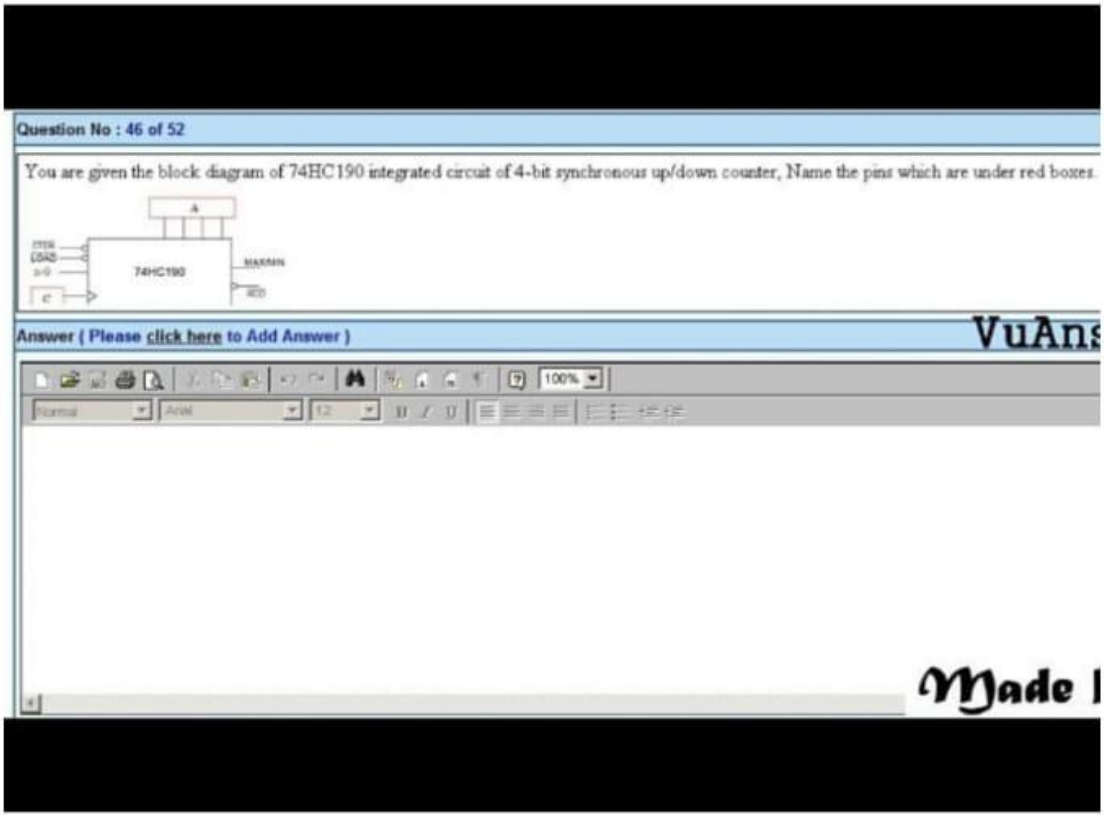




Figure 27.4a A 3-bit Synchronous Counter



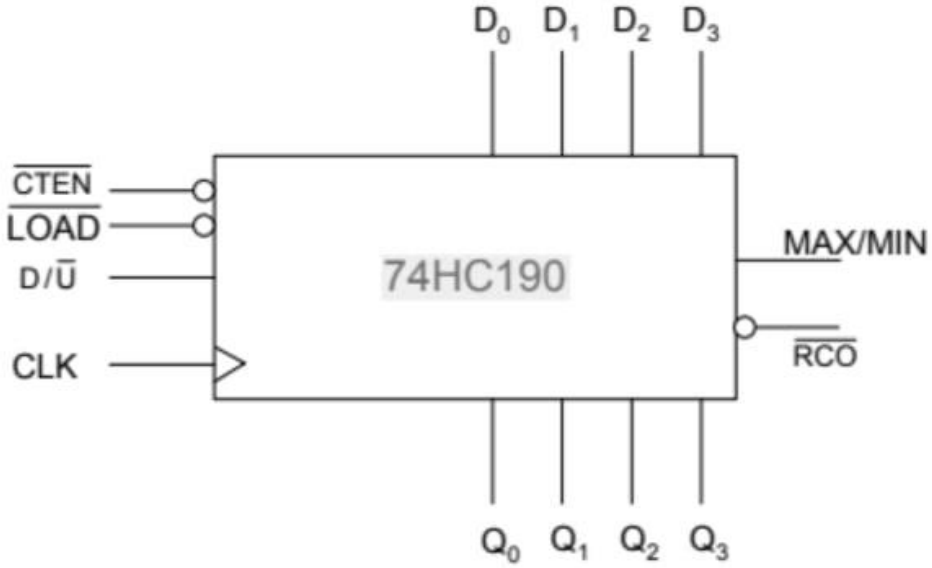
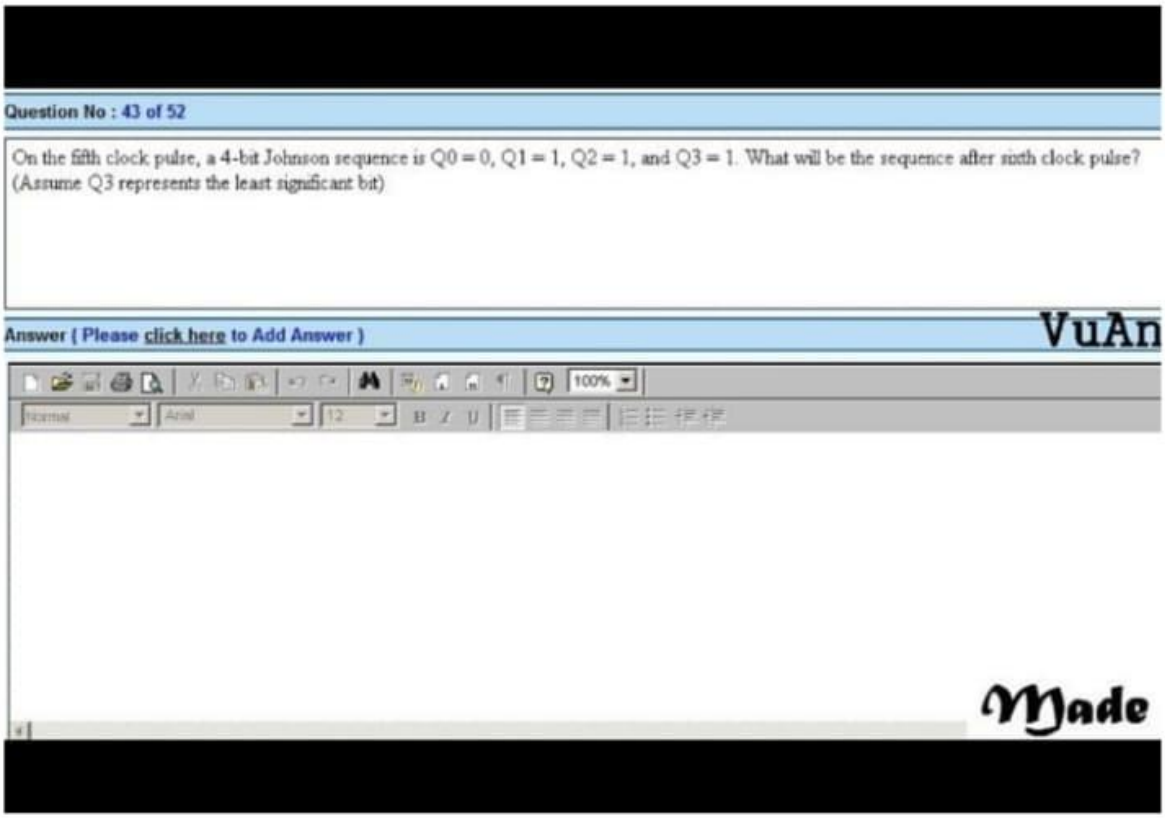
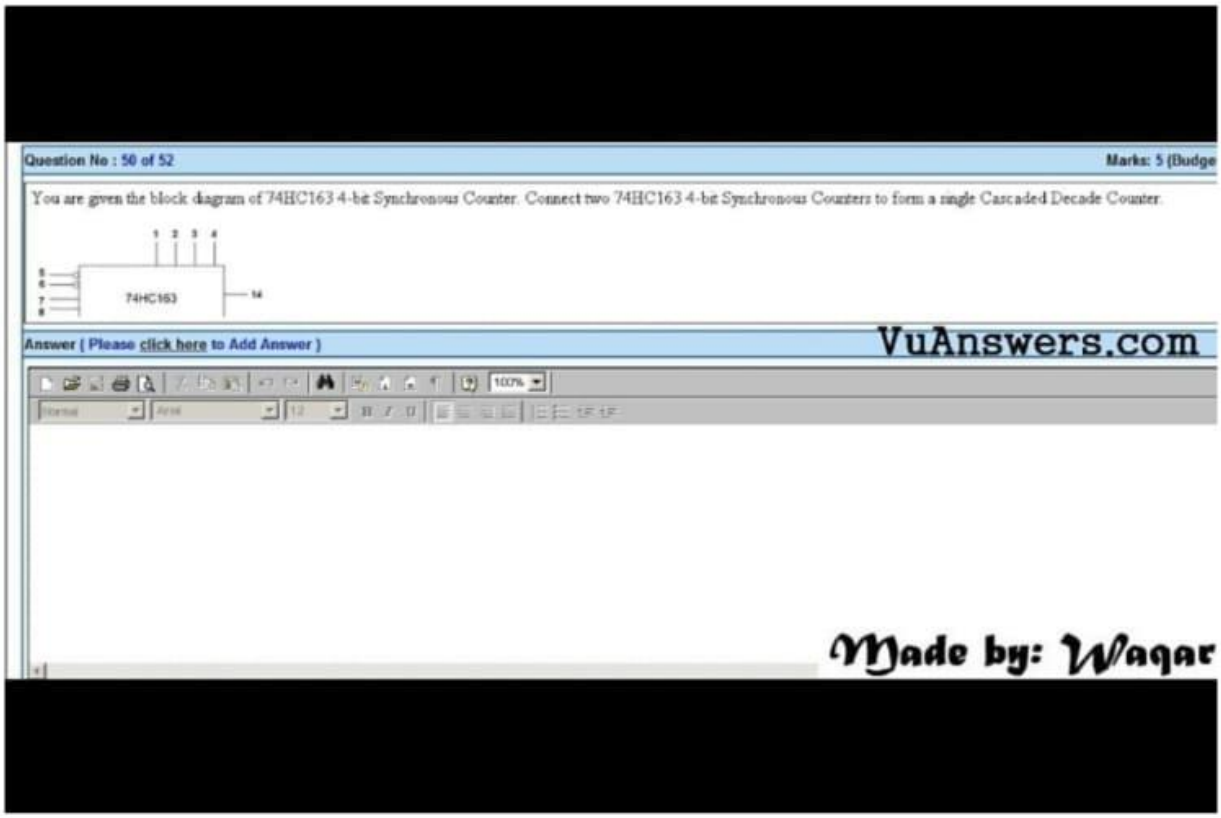




Figure 29.3 74HC190 4-bit Synchronous Up/Down Counter




| Clock Pulse | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 1 | 1 | 0 | 0 |
| 3 | 1 | 1 | 1 | 0 |
| 4 | 1 | 1 | 1 | 1 |
| 5 | 0 | 1 | 1 | 1 |
| 6 | 0 | 0 | 1 | 1 |
| 7 | 0 | 0 | 0 | 1 |

Table 34.1 Sequence of states of a 4-bit Johnson Counter



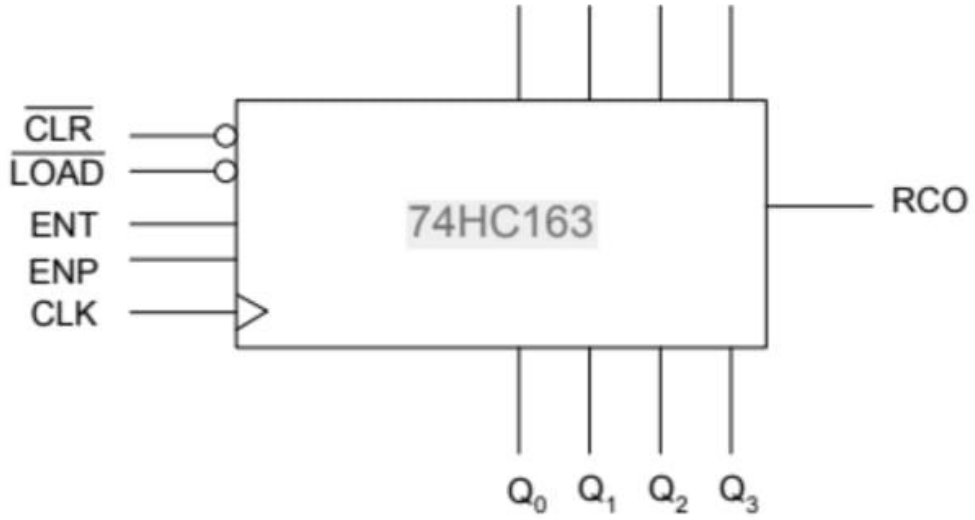
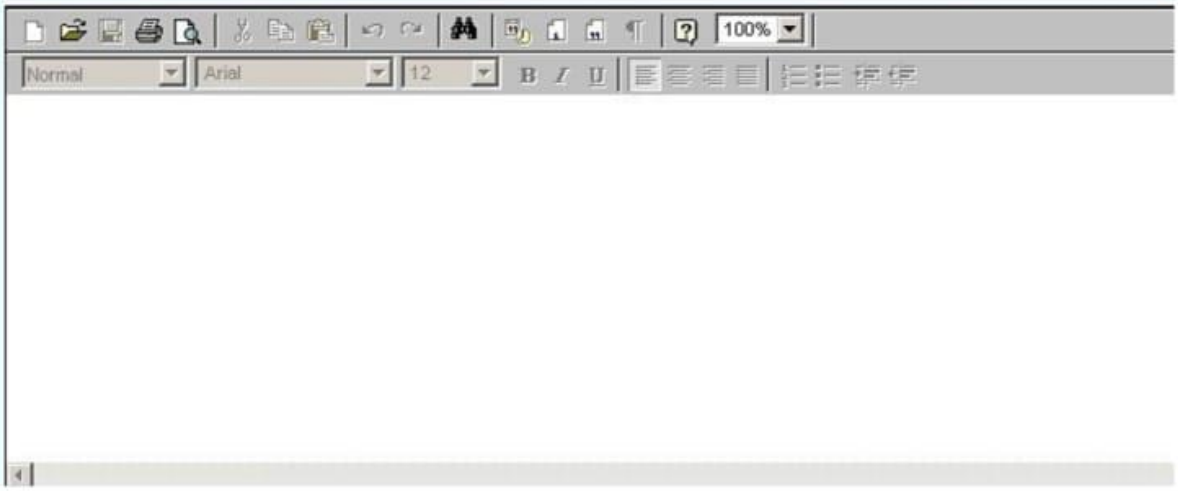




Figure 28.2a 74HC163 4-bit Synchronous Counter

**Question No : 43 of 52**

How many bytes will be there in 32 K x 4 memory?

**Answer ( Please click here to Add Answer )**




## HOW MANY BYTES WILL BE THERE IN 32 K X 4 MEMORY?

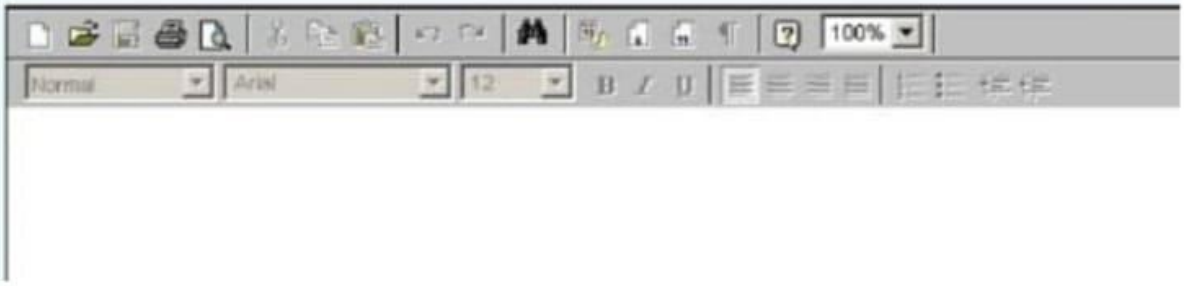
**Answer**:

32 X 1024BYTES X 4 = 131072 BYTES

**Question No : 48 of 52**

Draw the circuit diagram of operational amplifier used as an inverting amplifier.

**Answer ( Please click here to Add Answer )**



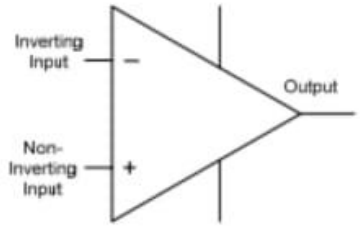




Figure 44.6a Op-Amp

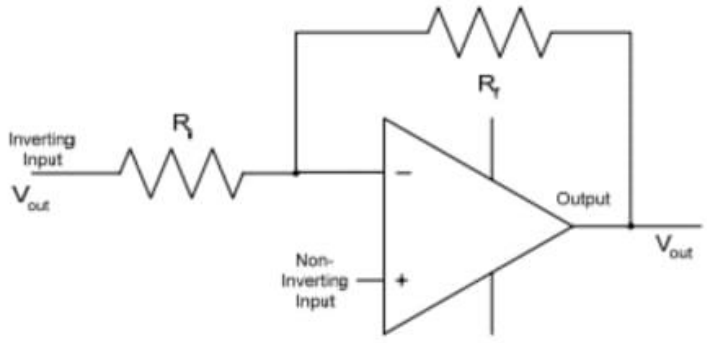



Figure 44.6b Op-Amp as an Inverting Amplifier

Question No : 42 of 52

What is meant by state assignment process?

Answer ( Please click here to Add Answer )


Explain state assignment process.

**Answer**:

Each state in a sequential circuit is identified by a unique combination of binary bits. Unless the output of the sequential is directly taken form the flip flop outputs such as counters, the states can be selected to allow minimum bit changes when changing from one state to the other.

Keeping the bits changes to minimum when changing from one state to the next which results in simpler combinational circuits that determine the next state. Generally, the selection of State Assignment is based on the following guidelines.

- Choose an initial coded state into which the state machine (sequential circuit) can easily be forced to reset (000 or 111)
- Minimize the State Variables that change on each transition
- Maximize the number of state variables that don't change in a group of related states
- If there are unused states, then choose the best state variable combinations to achieve the first three goals.

**Question No : 45 of 52**

Draw the function table of an Half adder circuit.

**Answer ( Please click here to Add Answer )**


**Half-Adder Function Table**

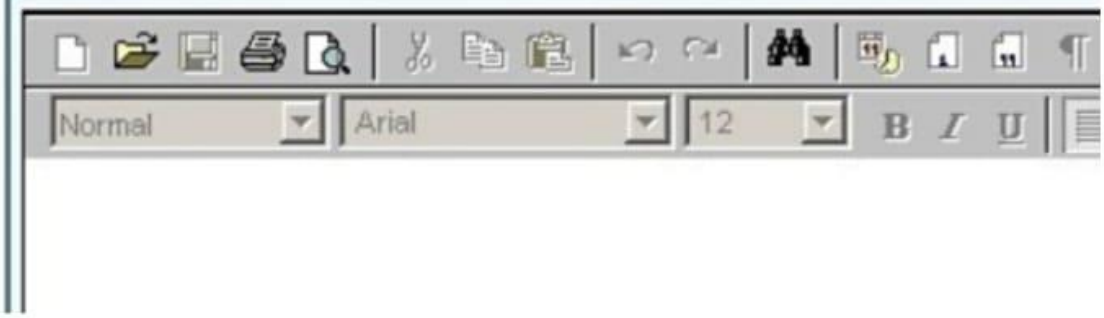
The Half-Adder has a 2-bit input and a 2-bit output. The function table of the Half-Adder has two input columns representing the two single bit numbers A and B. The function table also has two output columns representing the Sum bit and Carry Out bit. Table 14.3

| Input | | Output | |
|---|---|---|---|
| A | B | Sum | Carry Out |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

Table 14.3 Half-Adder Function Table

Draw the function table of Full adder circuit.

**Answer ( Please click here to Add Answer )**




**Full-Adder Function Table**

The Full-Adder has a 3-bit input and a 2-bit output. The function table of the Full-Adder has three input columns representing the two single bit numbers A, B and the Carry In bit. The function table also has two output columns representing the Sum bit and Carry Out bit. Table 14.4

| Input | | | Output | |
|---|---|---|---|---|
| A | B | Carry In(C) | Sum | Carry Out |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Table 14.4 Full-Adder Function Table

Draw the next-state table of a 3-bit Up Counter.

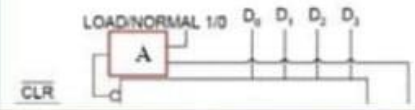
Answer ( Please click here to Add Answer )


| Present State | | | Next State | | |
|---|---|---|---|---|---|
| $Q_2$ | $Q_1$ | $Q_0$ | $Q_2$ | $Q_1$ | $Q_0$ |
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 |

**Table 28.1** Next-State Table for a 3-bit Up-Counter

Question No : 46 of 52

Following is an incomplete diagram. Name the gate which can be placed in red boxes A and B to configure 74HC161 as a Mod-9 counter.




Answer ( Please click here to Add Answer )



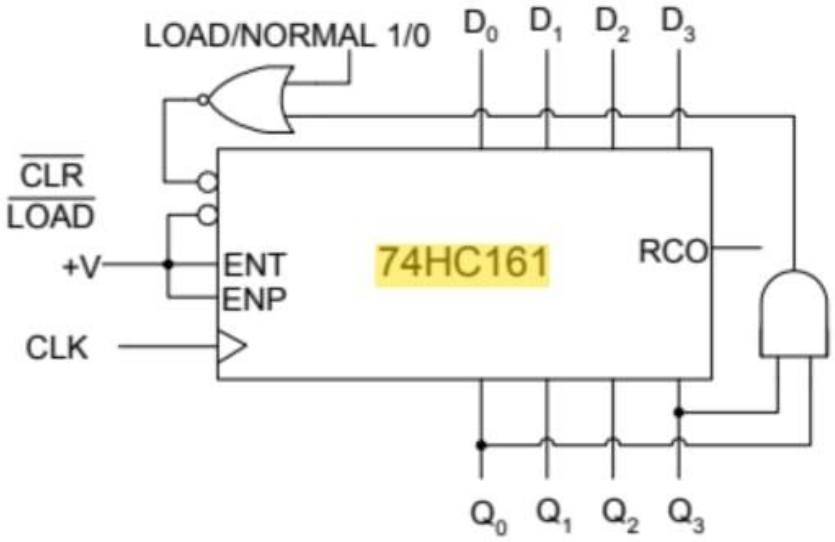


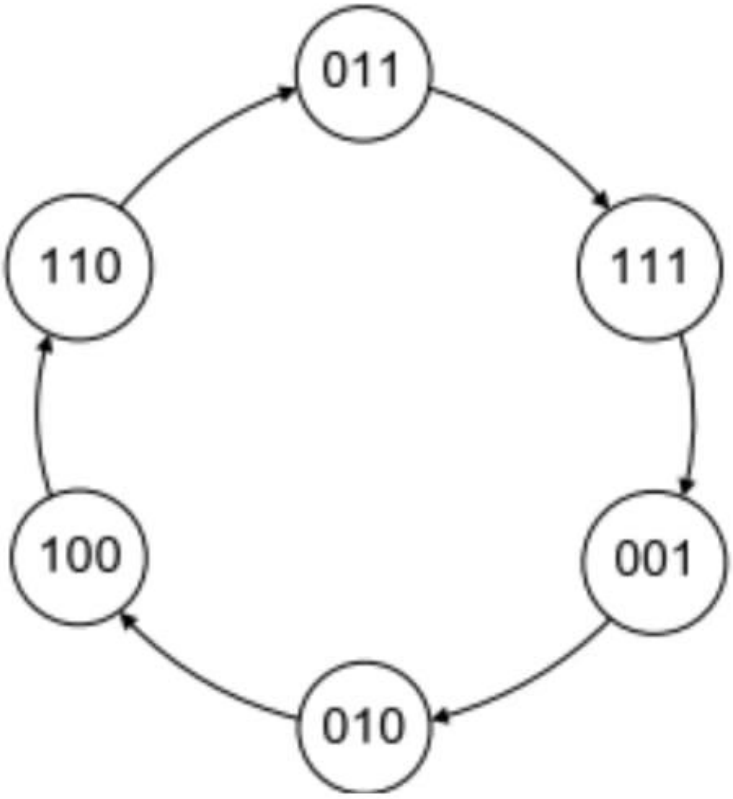

Figure 28.5a 74HC161 configured as Mod-9 counter

Question No : 50 of 52

You are given the Next-state table of a moor machine, using this information draw the state diagram of the machine.

| Present State | | | Next State | | |
|---|---|---|---|---|---|
| $Q_2$ | $Q_1$ | $Q_0$ | $Q_2$ | $Q_1$ | $Q_0$ |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 |

Answer ( Please click here to Add Answer )



**Question No : 51 of 52**

State table for a mealy machine is given below. Derive a state diagram for mealy machine from this state table.

| Present State | Next State | | | | Output Z | | | |
|---|---|---|---|---|---|---|---|---|
| | XY 00 | XY 01 | XY 10 | XY 11 | XY 00 | XY 01 | XY 10 | XY 11 |
| A | A | C | B | C | 0 | 1 | 0 | 1 |
| B | B | D | C | D | 0 | 0 | 0 | 0 |

**Answer ( Please click here to Add Answer )**

| Present State | Next State | | | | Output Z | | | |
|---|---|---|---|---|---|---|---|---|
| | XY 00 | XY 01 | XY 10 | XY 11 | XY 00 | XY 01 | XY 10 | XY 11 |
| A | A | C | B | C | 0 | 1 | 0 | 1 |
| B | B | D | C | D | 0 | 0 | 0 | 0 |
| C | C | A | D | A | 0 | 0 | 0 | 0 |
| D | D | C | A | C | 0 | 0 | 1 | 1 |

Table 38.13 State Table of a Mealy Machine

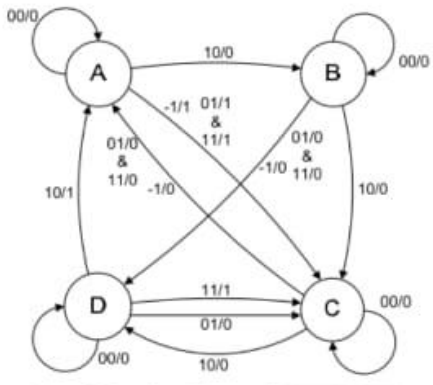
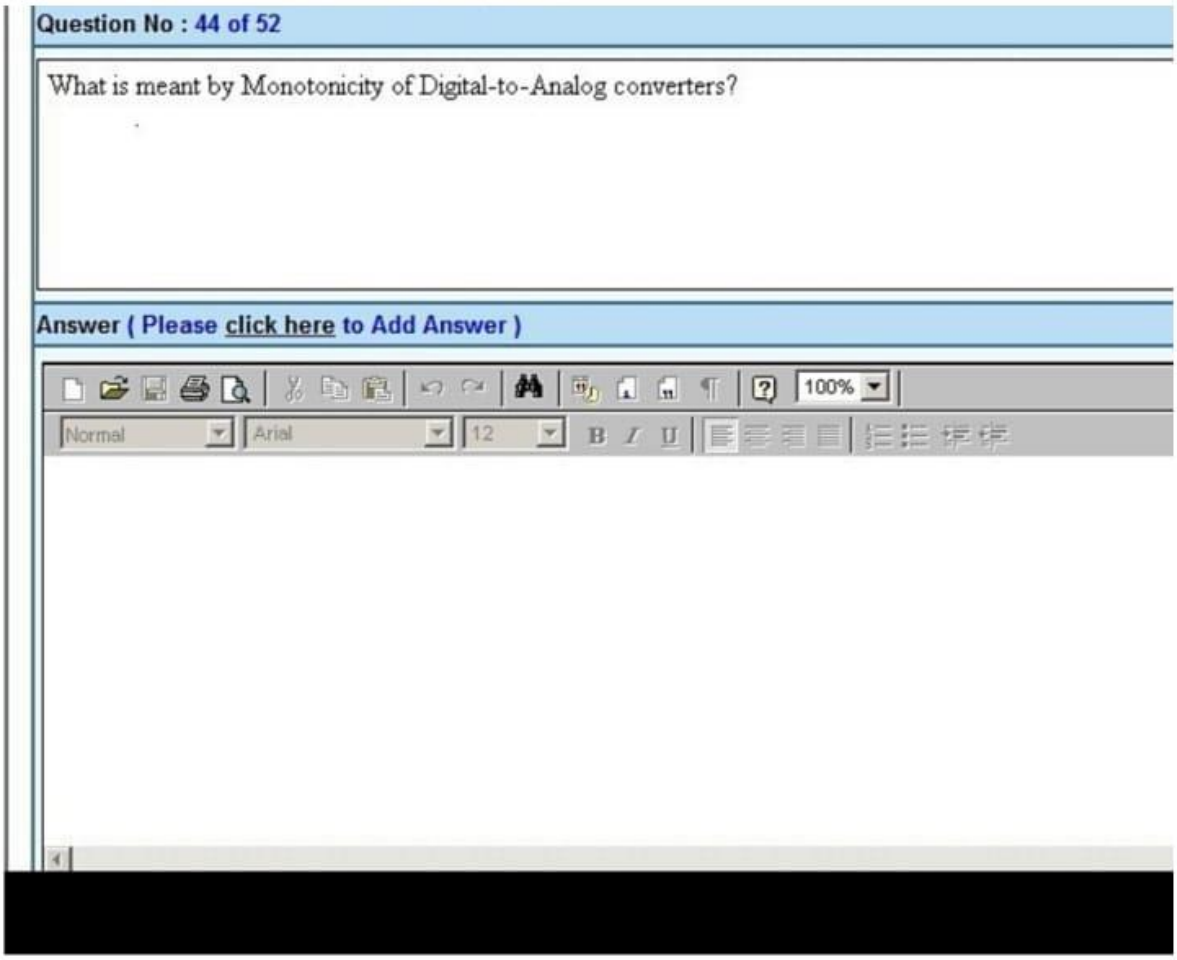



Figure 38.7 State Diagram of a Mealy Machine




**4: What is meant by Non-Monotonicity of Digital to Analog converter?**
**Answer:- (Page 460)**
if the D/A converter outputs a lower voltage than its preceding output voltage the converter is said to exhib
non-monotonic behavior.

Draw a circuit diagram of flip-flop based static memory cell.

**Answer ( Please click here to Add Answer )**

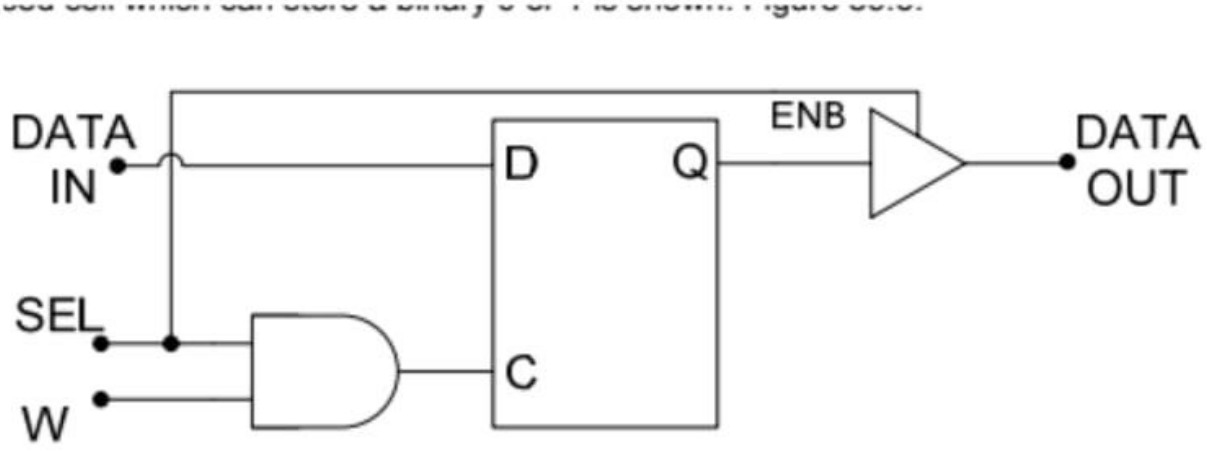
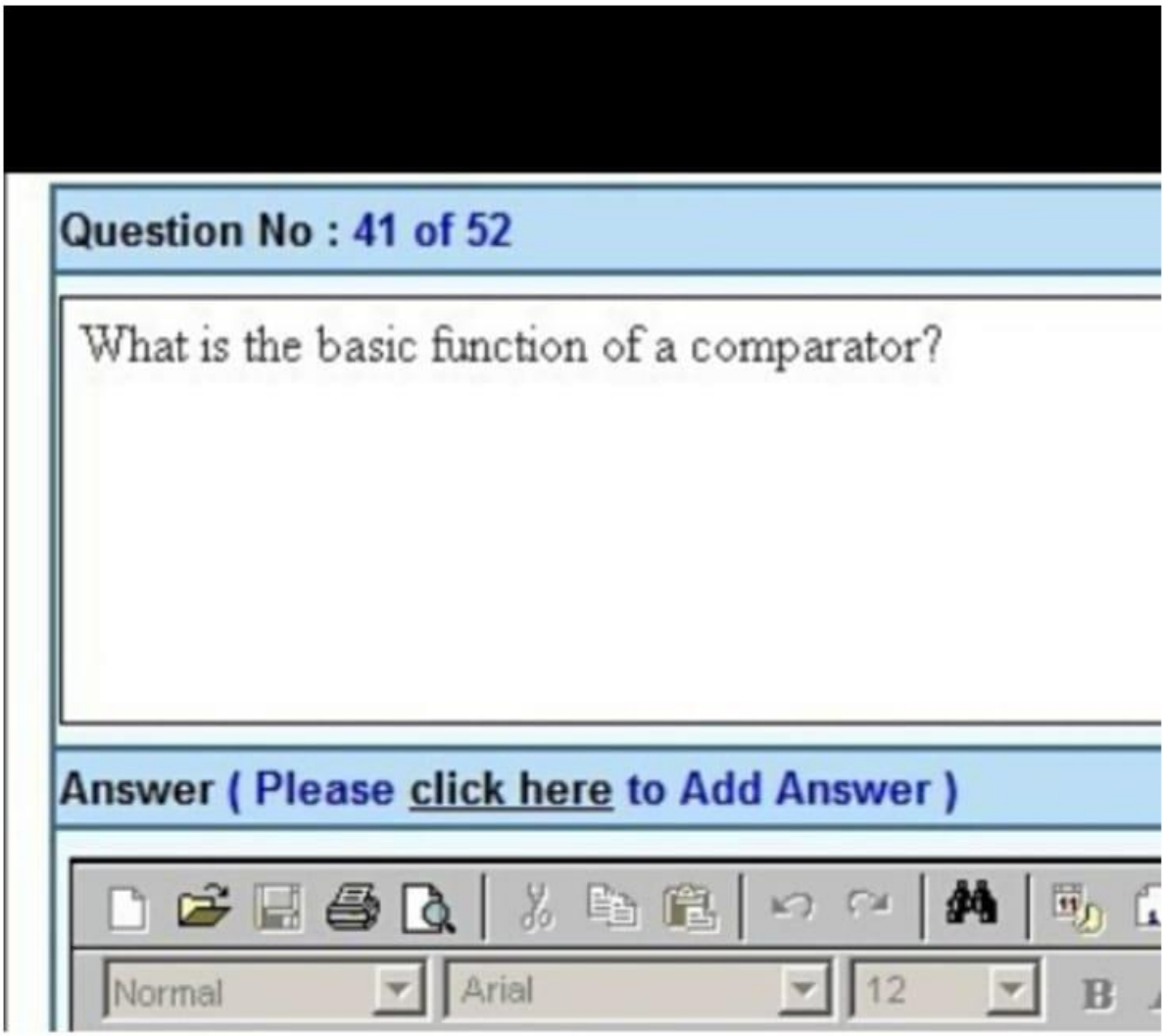
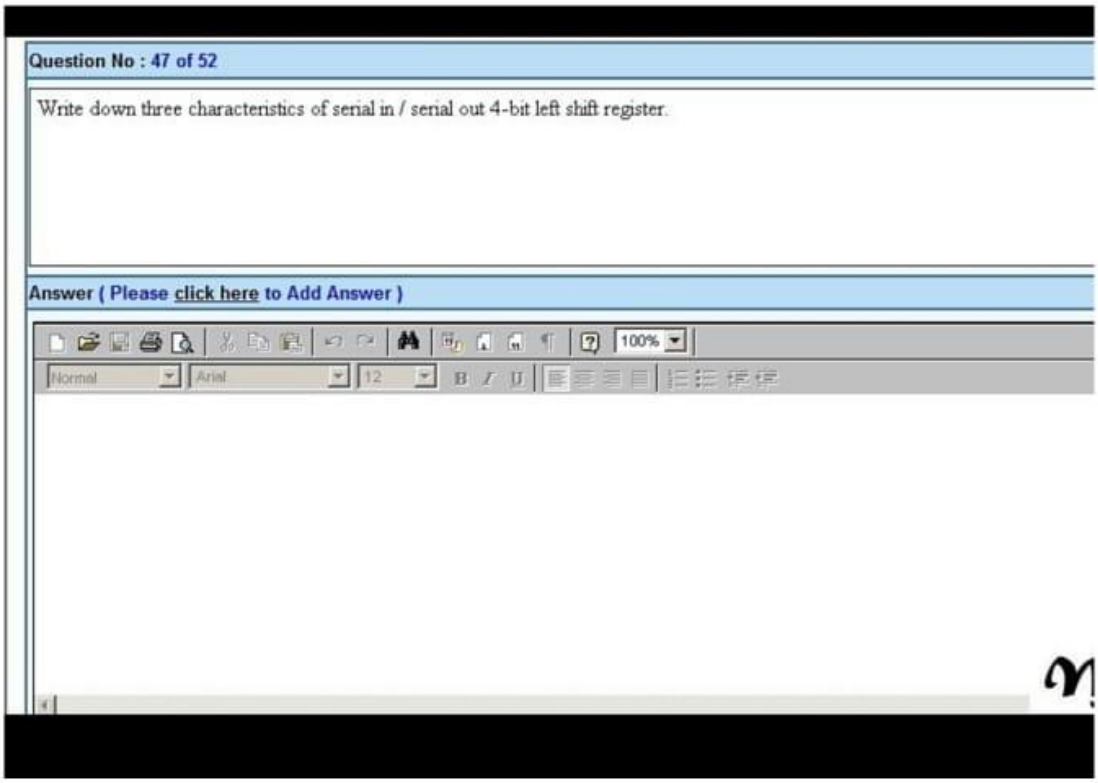



Figure 39.6 Circuit diagram of a Static Memory Cell based on a flip-flop




The basic function of a Comparator is to compare two binary quantities and to determine if the two quantities are equal. If the quantities are not equal then it has to determine which of the two quantities is greater than the other. Many Integrated Circuit Comparators have three outputs to indicate A=B, A>B and A<B.




**Question No: 37 ( Marks: 3 )**

Write down at least three characteristics of serial in / serial out 4-bit right shift register.

**Answer**:

A serial-in/serial-out shift register has a clock input, a data input, and a data output from the last stage. In general, the other stage outputs are not available Otherwise, it would be a serial-in, parallel-out shift register.

The waveforms below are applicable to either one of the preceding two versions of the serial-in, serial-out shift register. The three pairs of arrows show that a three stage shift register temporarily stores 3-bits of data and delays it by three clock periods from input to output.

Explain at least two advantages of the circuit having low power consumption 3 marks

**Answer**:

**Power Dissipation**

Logic Gates and Logic circuits consume varying amount of power during their operation. Ideally, logic gates and logic circuit should consume minimal power. Advantages of low power consumption are circuits that can be run from batteries instead of mains power supplies. Thus portable devices that run on batteries use Integrated circuits that have low power dissipation.

Secondly, low **Power consumption** means less heat is dissipated by the logic devices; this means that logic gates can be tightly packed to reduce the circuit size without having to worry about dissipating the access heat generated by the logic devices.